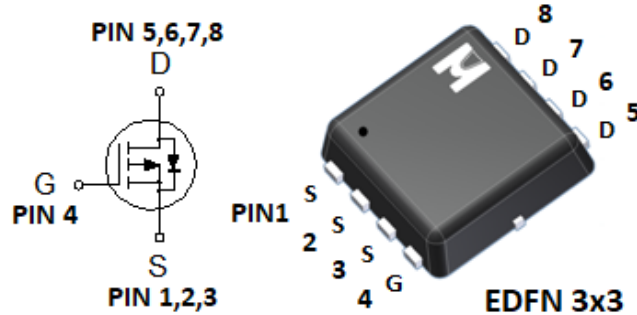


Single P-Channel Logic Level Enhancement Mode Field Effect Transistor

•Product Summary:

	P-CH
BV _{DSS}	-30V
R _{DSON (MAX.)} @V _{GS} =-10V	14mΩ
R _{DSON (MAX.)} @V _{GS} =-4.5V	22mΩ
I _D @T _C =25°C	-40A

• Pin Description:



Single P Channel MOSFET

UIS, Rg 100% Tested

RoHS & Halogen Free & TSCA Compliant

ESD level>2KV



▪ ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNIT
Gate-Source Voltage	V _{GS}	±25	V
Continuous Drain Current ¹	I _D	T _C = 25 °C	-40
		T _C = 100 °C	-35
		T _A = 25 °C	-10
		T _A = 70 °C	-8
Pulsed Drain Current ¹	I _{DM}	-105	A
Avalanche Current ^{1,4}	I _{AS}	-50	
Avalanche Energy ^{1,4}	E _{AS}	L = 0.1mH	125
Repetitive Avalanche Energy ^{2,4}		L = 0.05mH	62.5
Power Dissipation ¹	P _D	T _C = 25 °C	69
		T _C = 100 °C	28
Power Dissipation ¹	P _D	T _A = 25 °C	2.3
		T _A = 70 °C	1.5
Operating Junction & Storage Temperature Range	T _j , T _{stg}	-55 to 150	°C

▪ 100% UIS testing in condition of VD=25V, L=0.1mH, VG=10V, IL= 30A, RG=25Ω, Rated VDS=30V P-CH

•THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		1.8	°C / W
Junction-to-Ambient ³		t≤10s	23	
		Steady-State	55	

¹Pulse width limited by maximum junction temperature.

²Duty cycle < 1%

³The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C.

⁴Guarantee by Engineering test

▪ ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-30			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1.2	-1.5	-2.5	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±25V			±500	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = -30V, V _{GS} = 0V			-1	μA
		V _{DS} = -30V, V _{GS} = 0V, T _J = 125 °C			-25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = -10V, V _{GS} = -10V	-40			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = -10V, I _D = -12A		9	14	mΩ
		V _{GS} = -4.5V, I _D = -9A		13	22	
Forward Transconductance ¹	g _{fs}	V _{DS} = -5V, I _D = -9A		30		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = -15V, f = 1MHz		2345		pF
Output Capacitance ⁵	C _{oss}			315		
Reverse Transfer Capacitance ⁵	C _{rss}			260		
Gate Resistance ^{4,5}	R _g	f = 1MHz		3.0		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = -15V, V _{GS} = -10V, I _D = -12A		51		nC
	Q _g (V _{GS} =4.5V)			25		
Gate-Source Charge ^{1,2,5}	Q _{gs}			8.2		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			11		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = -15V, V _{GS} = -10V, I _D = -5A, R _g = 3Ω		6.8		nS
Rise Time ^{1,2,5}	t _r			10		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			55		
Fall Time ^{1,2,5}	t _f			33		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				-40	A
Pulsed Current ³	I _{SM}				-105	
Forward Voltage ^{1,4}	V _{SD}	I _F = -12A, V _{GS} = 0V			1.2	V
Reverse Recovery Time ⁵	t _{rr}	I _F = -12A, dI _F /dt = 100A / μS		15		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			1.5		A
Reverse Recovery Charge ⁵	Q _{rr}			8.4		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.



•TYPICAL CHARACTERISTICS

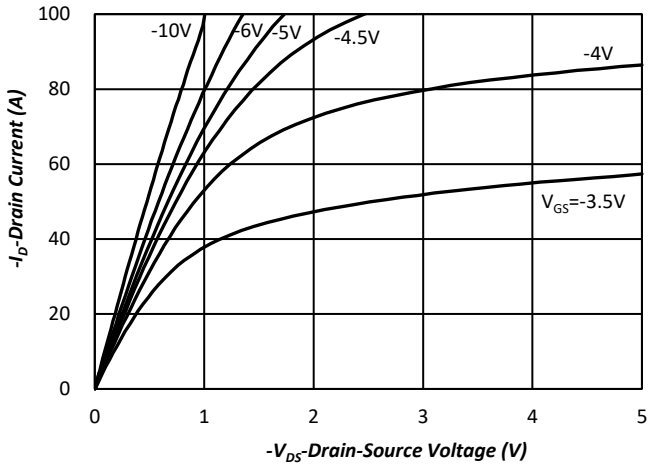


Fig.1 Typical Output Characteristics

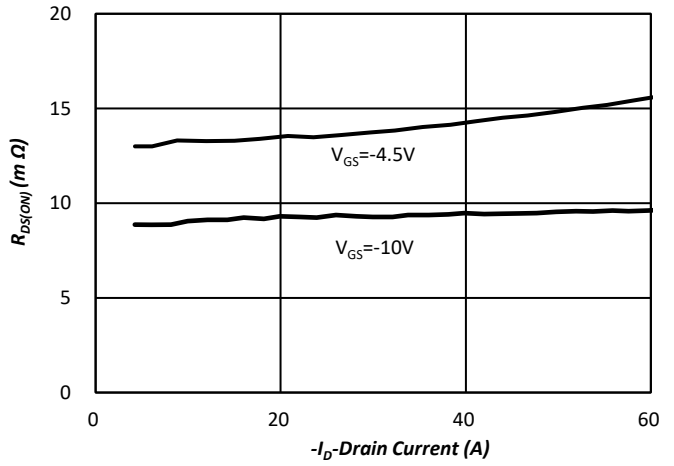


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

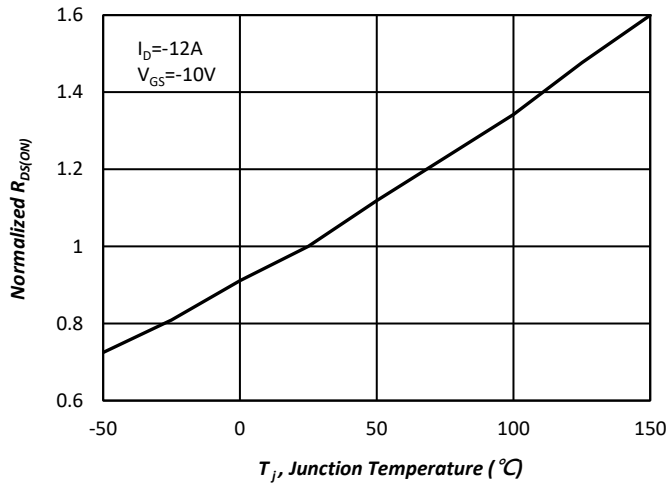


Fig.3 Normalized On-Resistance v.s. Junction Temperature

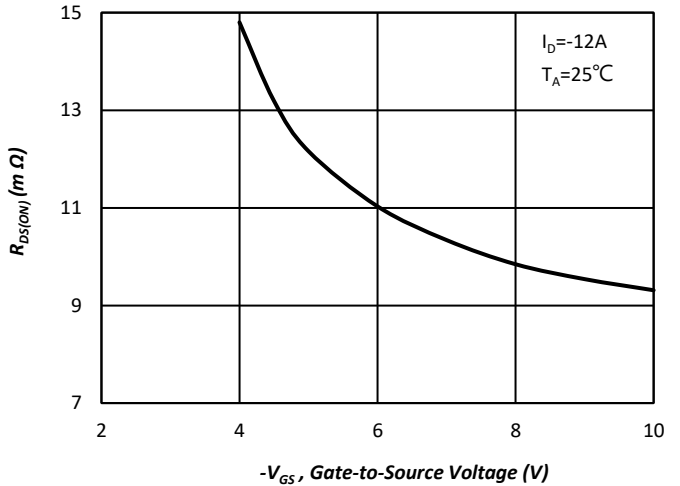


Fig.4 On-Resistance v.s. Gate Voltage

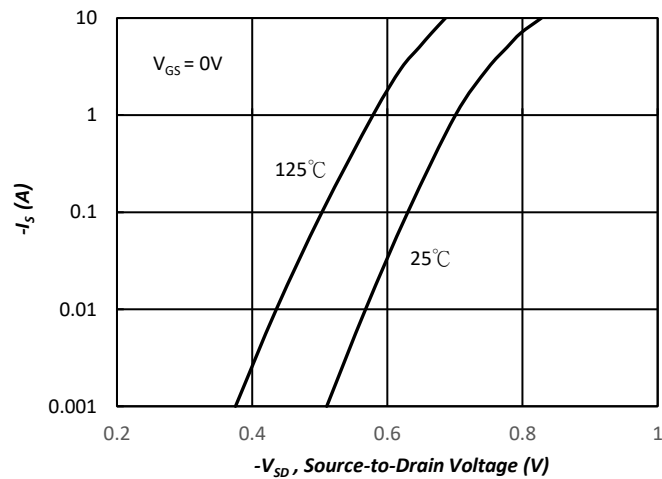


Fig.5 Forward Characteristic of Reverse Diode

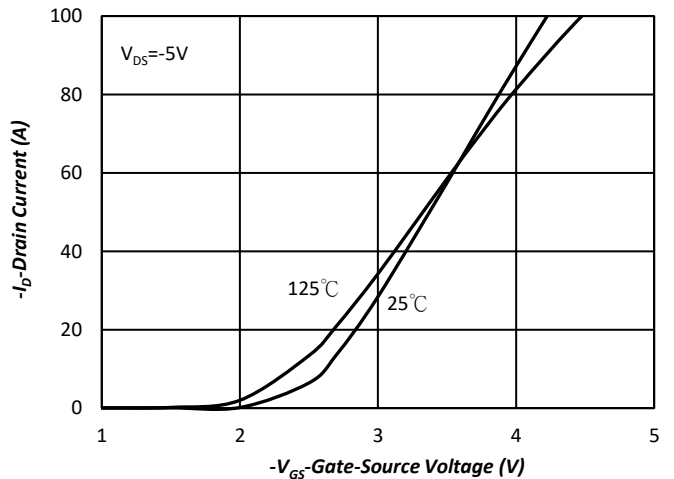


Fig.6 Transfer Characteristics

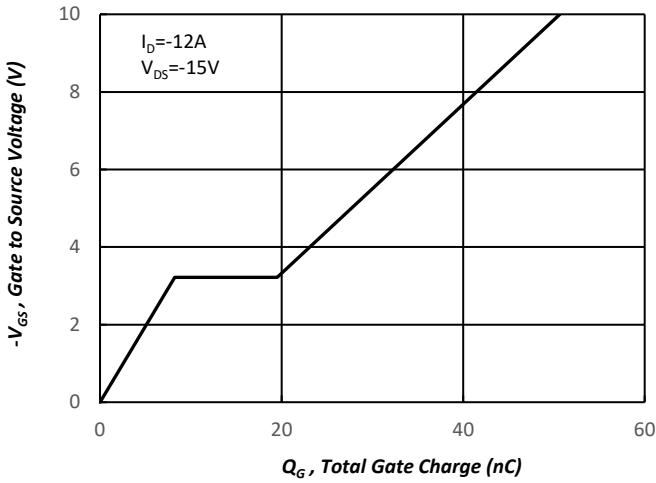


Fig.7 Gate Charge Characteristics

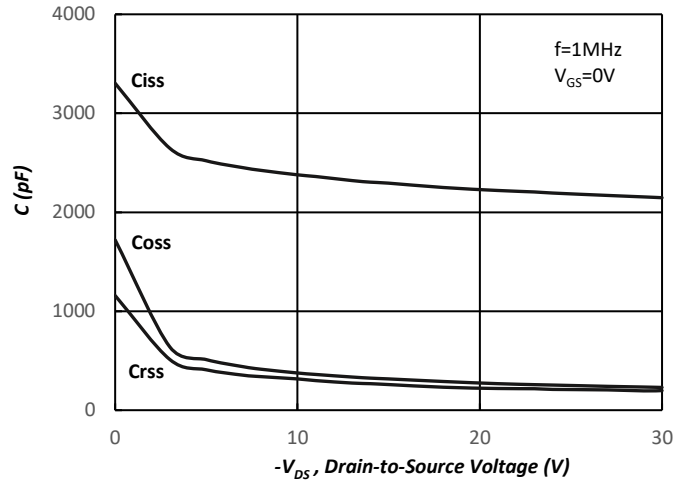


Fig.8 Typical Capacitance Characteristics

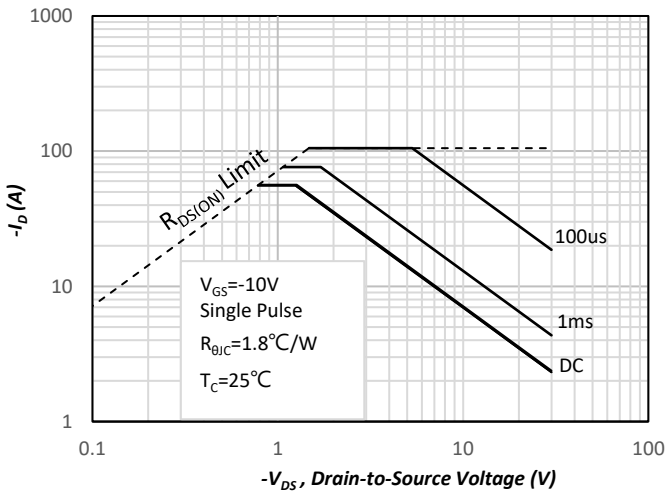


Fig.9. Maximum Safe Operating Area

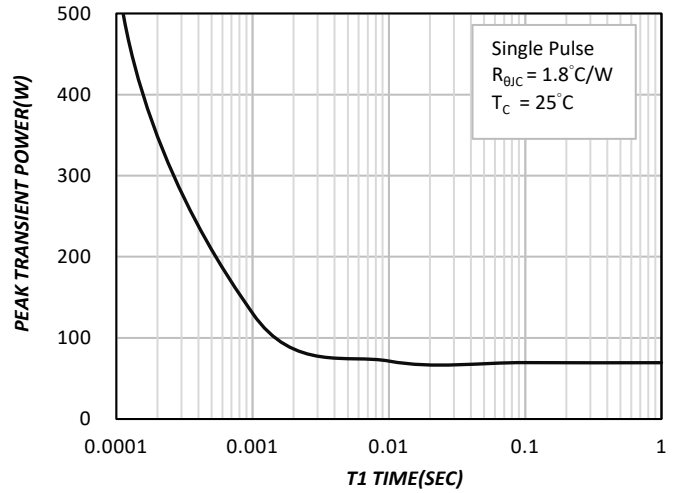


Fig.10. Single Pulse Maximum Power Dissipation

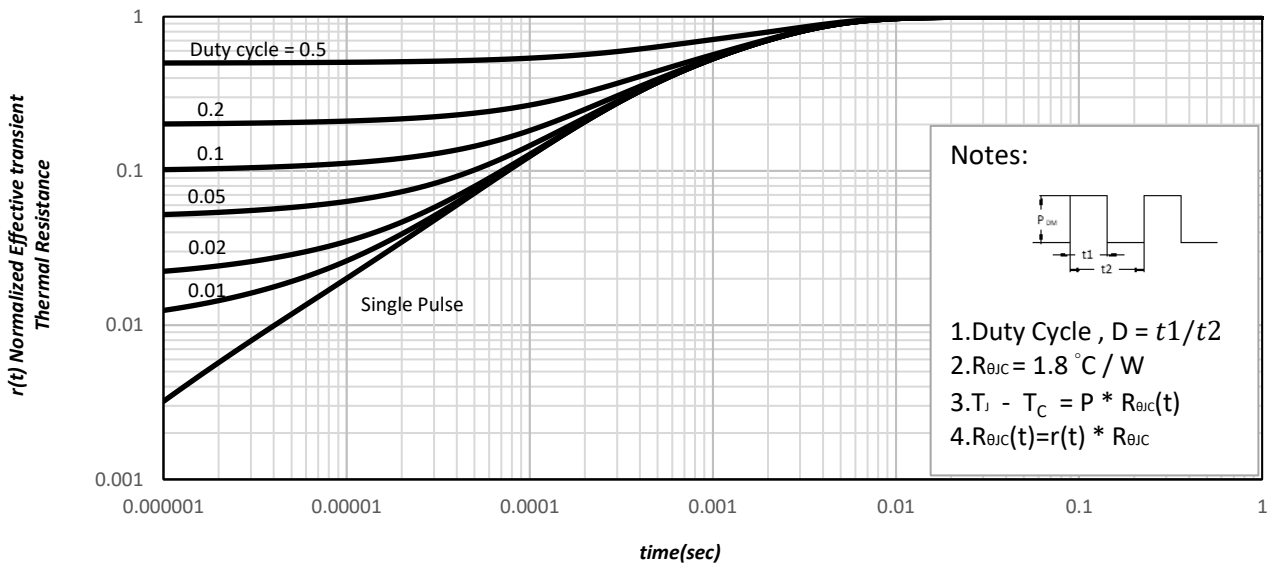
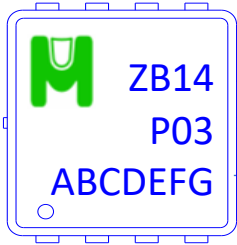


Fig.11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMZB14P03V for EDFN3X3



ZB14P03: Device Name

ABCDEFG: Date Code

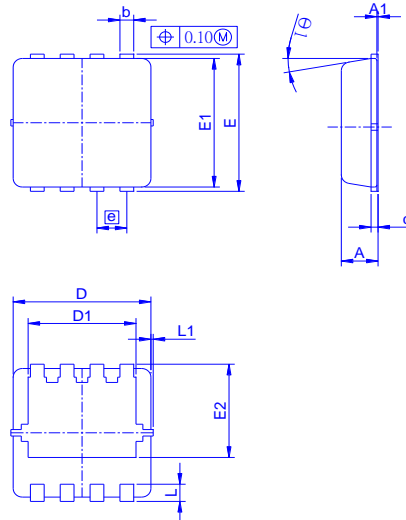
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

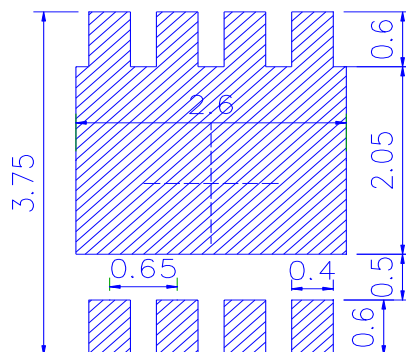
DEFG: Serial No.

Outline Drawing

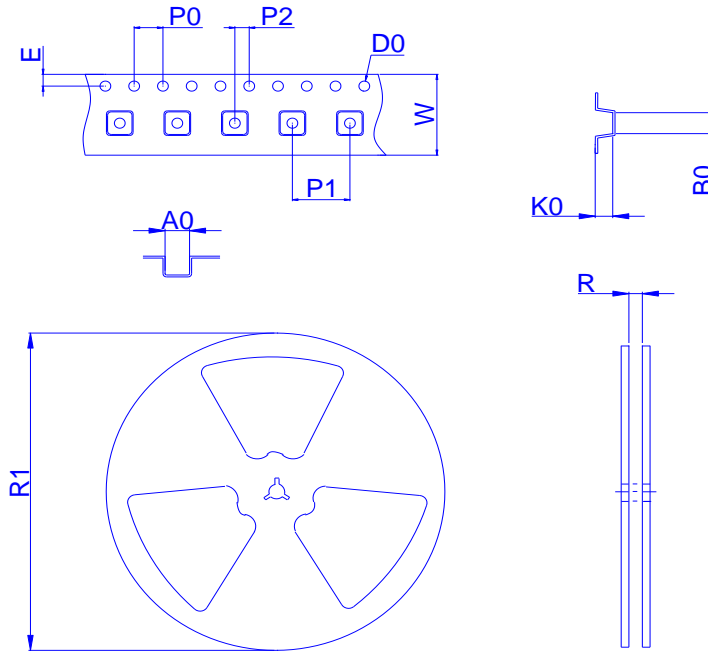


Dimension	A	A1	b	c	D	D1	E	E1	E2	e	L	L1	Θ1
Min.	0.65	0	0.2	0.1	2.9	2.15	3.1	2.9	1.53	0.55	0.25	-	0°
Typ.	0.75	-	0.3	0.15	3	2.45	3.2	3	1.97	0.65	0.4	0.075	10°
Max.	0.9	0.05	0.4	0.25	3.3	2.74	3.5	3.3	2.59	0.75	0.6	0.15	14°

Footprint



◆ **Tape&Reel Information: 5000pcs/Reel**



Package	EDFN3X3
Reel	13"
Device orientation	<p>FEED DIRECTION</p>

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	3.6	3.6	1.55	1.7	1.2	4	8	2	12	12.4	330
±	0.3	0.3	0.2	0.2	0.2	0.1	0.1	0.1	1	2	2