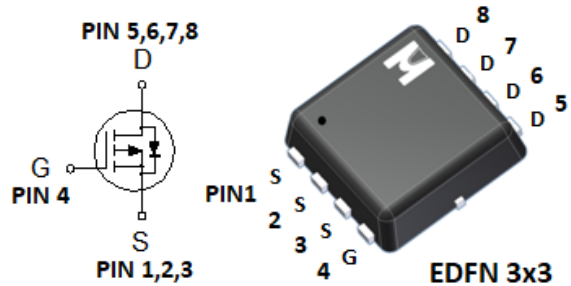


Single P-Channel Logic Level Enhancement Mode Field Effect Transistor

• Product Summary:

	P-CH
BV_{DSS}	-30 V
$R_{DS(on)} (MAX.) @ V_{GS} = -10V$	8.5 mΩ
$R_{DS(on)} (MAX.) @ V_{GS} = -4.5V$	15 mΩ
$I_D @ T_C = 25^\circ C$	-55 A
$I_D @ T_A = 25^\circ C$	-13 A

• Pin Description:



Single P Channel MOSFET

UIS, Rg 100% Tested

RoHS & Halogen Free & TSCA Compliant

ESD Protection



• ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 25	V
Continuous Drain Current	$T_C = 25^\circ C$	I_D	-55	A
	$T_C = 100^\circ C$		-36	
Continuous Drain Current	$T_A = 25^\circ C$	I_D	-13	
	$T_A = 70^\circ C$		-10	
Pulsed Drain Current ¹		I_{DM}	-144	mJ
Avalanche Current		I_{AS}	-25	
Avalanche Energy	$L = 0.1mH$	EAS	31.25	mJ
Repetitive Avalanche Energy ²	$L = 0.05mH$	EAR	15.625	
Power Dissipation	$T_C = 25^\circ C$	P_D	39	W
	$T_C = 100^\circ C$		16	
Power Dissipation	$T_A = 25^\circ C$	P_D	2.2	W
	$T_A = 70^\circ C$		1.4	
Operating Junction & Storage Temperature Range		$T_{j, T_{stg}}$	-55 to 150	$^\circ C$

* 100% UIS testing in condition of $V_D = 25V$, $L = 0.1mH$, $V_G = 10V$, $I_L = 20A$, $R_G = 25\Omega$, Rated $V_{DS} = -30V$ P-CH

• THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case		$R_{\theta JC}$		3.2	$^\circ C/W$
Junction-to-Ambient ³	$t \leq 10s$	$R_{\theta JA}$		26	
	Steady-State	$R_{\theta JA}$		58	

¹ Pulse width limited by maximum junction temperature.

² Duty cycle $< 1\%$

³ The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ C$.

⁴ Guarantee by Engineering test

▪ ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-30			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1.2	-1.5	-2.5	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±25V			±10	μA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = -30V, V _{GS} = 0V			-1	μA
		V _{DS} = -30V, V _{GS} =0V, T _J = 125 °C			-25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = -5V, V _{GS} = -10V	-55			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = -10V, I _D = -12A		7.5	8.5	mΩ
		V _{GS} = -4.5V, I _D = -9A		10	15	
Forward Transconductance ¹	g _{fs}	V _{DS} = -5V, I _D = -16A		44		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = -15V, f = 1MHz		2830		pF
Output Capacitance ⁵	C _{oss}			455		
Reverse Transfer Capacitance ⁵	C _{rss}			355		
Gate Resistance ^{4,5}	R _g	f = 1MHz		3.2		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =-10V)	V _{DS} = -15V, V _{GS} = -10V, I _D = -12A		55		nC
	Q _g (V _{GS} =-4.5V)			27		
Gate-Source Charge ^{1,2,5}	Q _{gs}			9.1		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			13		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = -15V, V _{GS} = -10V, I _D = -5A , R _g = 3Ω		7.5		nS
Rise Time ^{1,2,5}	t _r			12		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			65		
Fall Time ^{1,2,5}	t _f			48		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				-33	A
Pulsed Current ³	I _{SM}				-144	
Forward Voltage ^{1,4}	V _{SD}	I _F = -12A, V _{GS} = 0V			-1.2	V
Reverse Recovery Time ⁵	t _{rr}	I _F = -12A, dI _F /dt = 100A / μS		11		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			0.5		A
Reverse Recovery Charge ⁵	Q _{rr}			2.6		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.



•TYPICAL CHARACTERISTICS

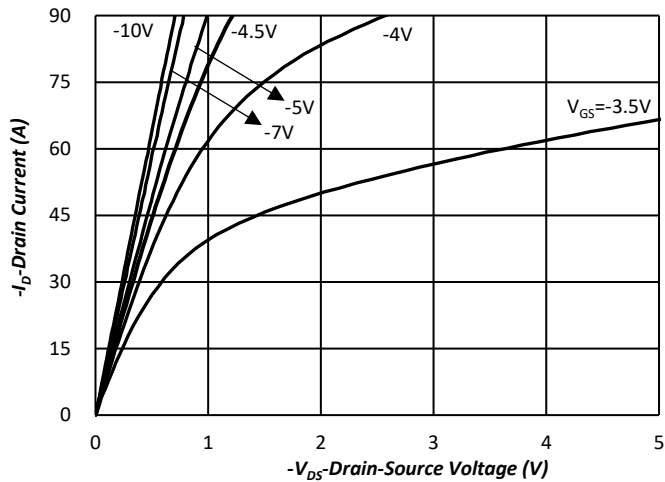


Fig.1 Typical Output Characteristics

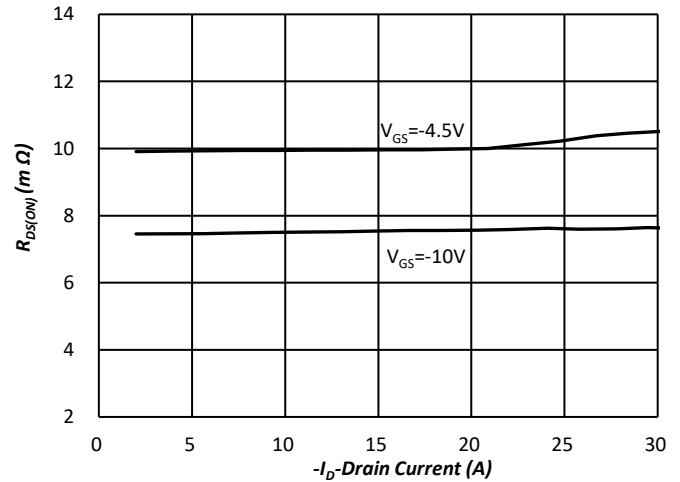


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

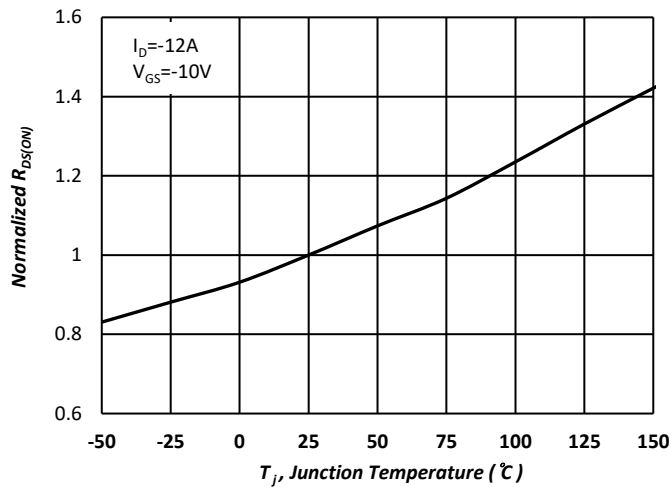


Fig.3 Normalized On-Resistance v.s. Junction Temperature

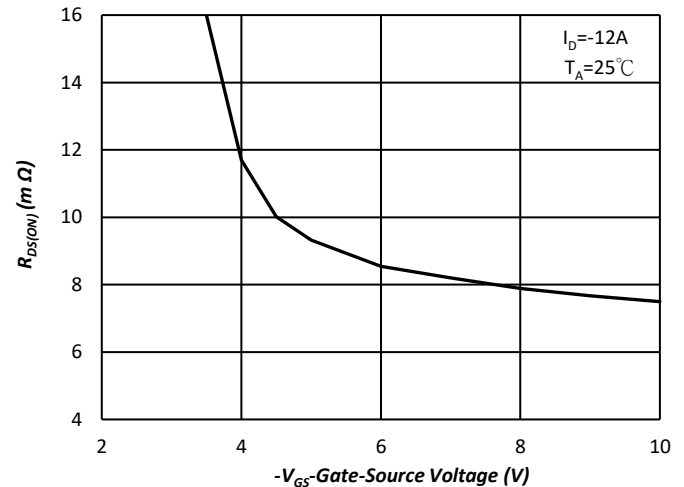


Fig.4 On-Resistance v.s. Gate Voltage

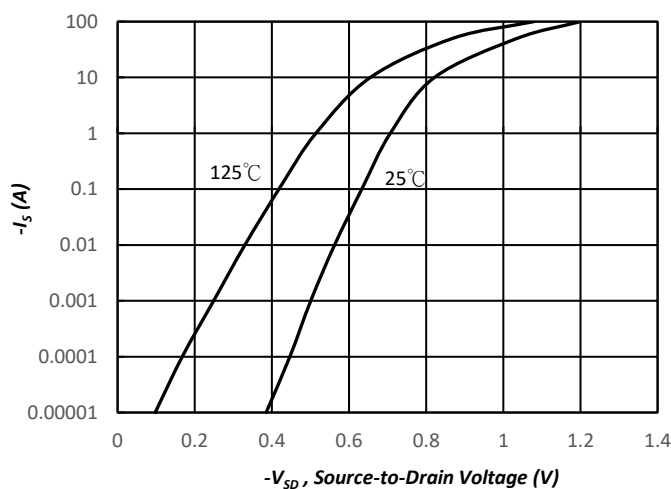


Fig.5 Forward Characteristic of Reverse Diode

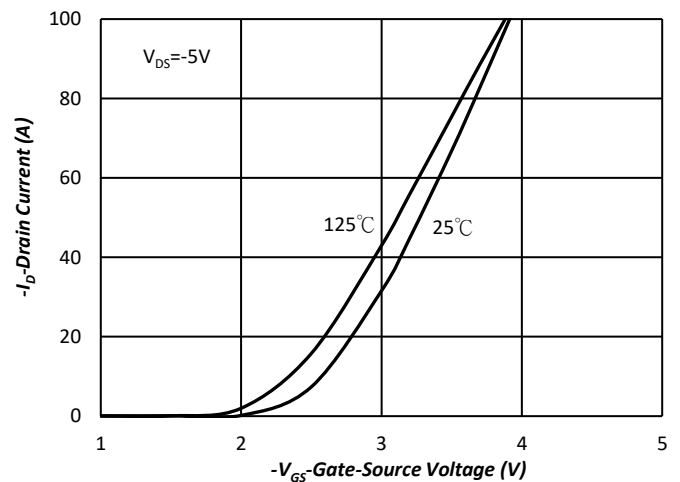


Fig.6 Transfer Characteristics

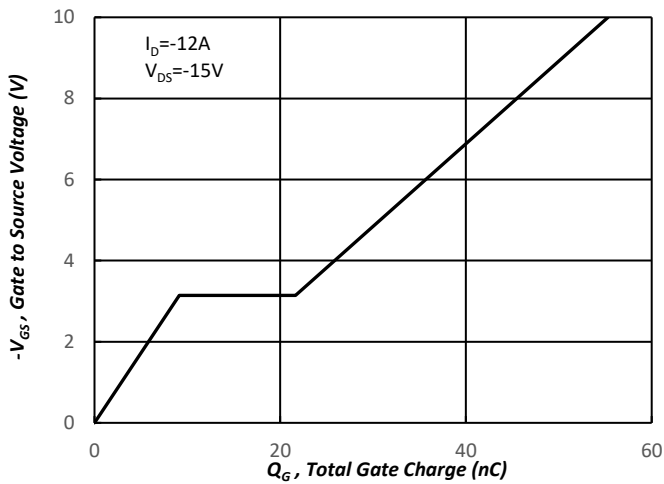


Fig.7 Gate Charge Characteristics

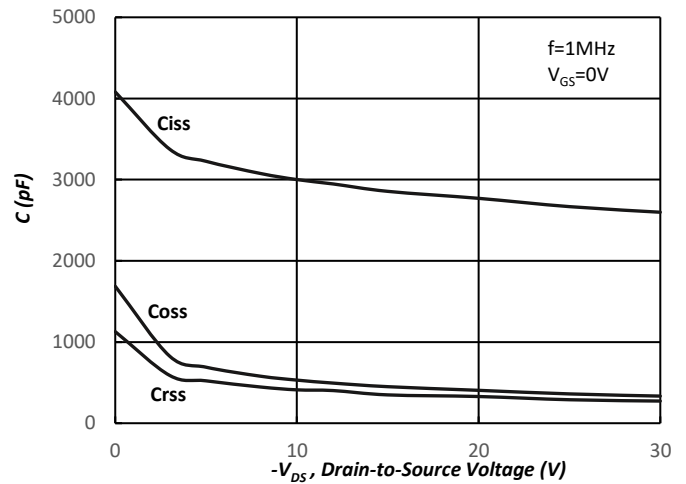


Fig.8 Typical Capacitance Characteristics

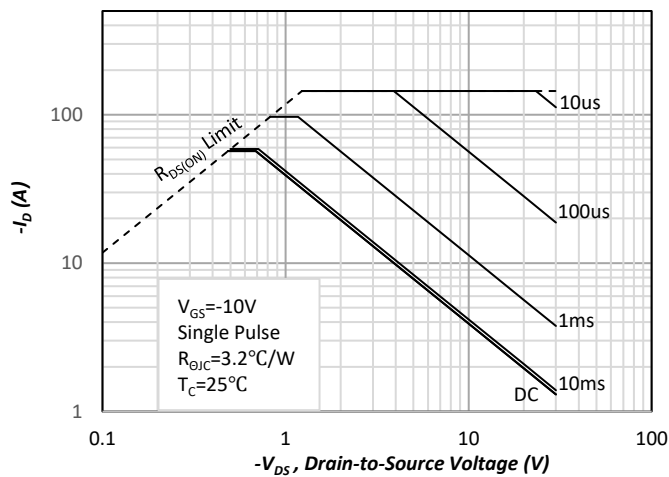


Fig.9. Maximum Safe Operating Area

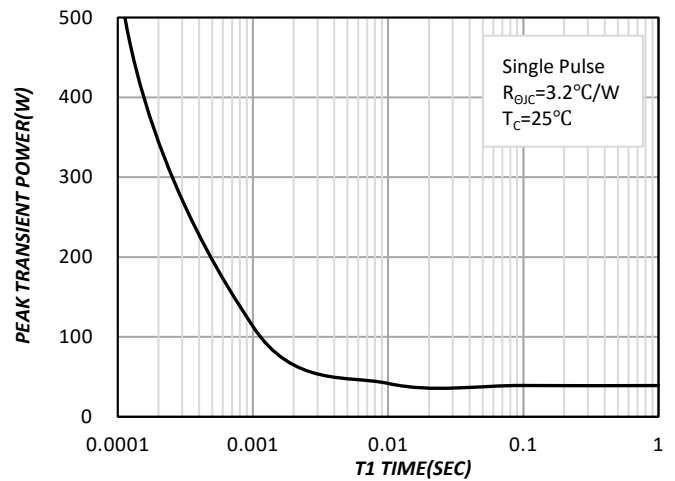


Fig.10. Single Pulse Maximum Power Dissipation

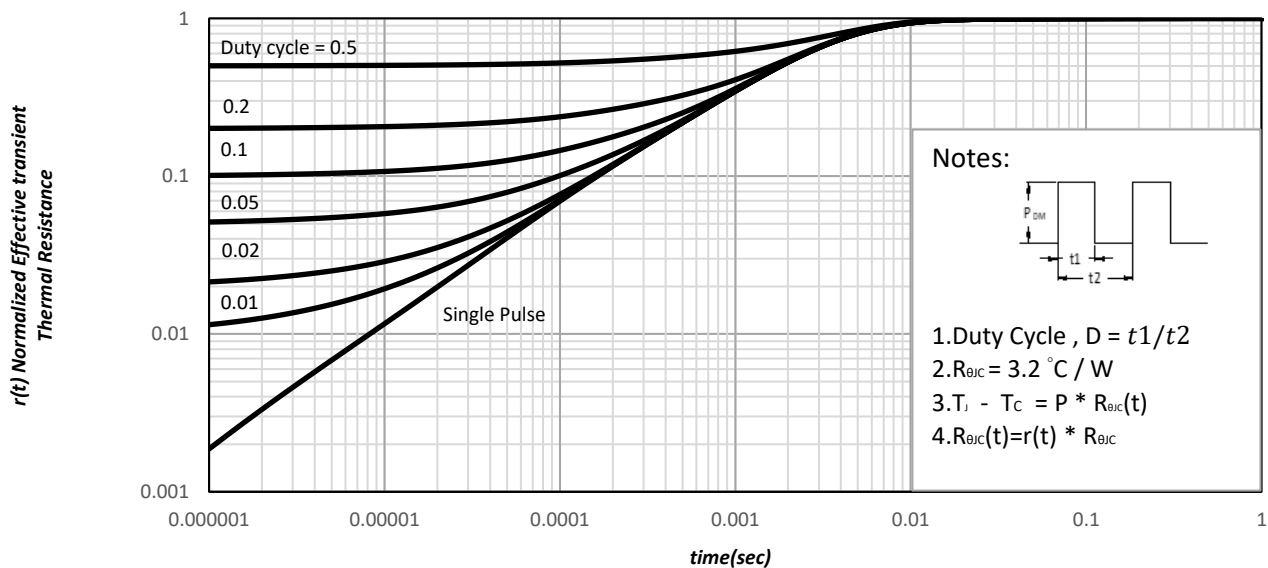
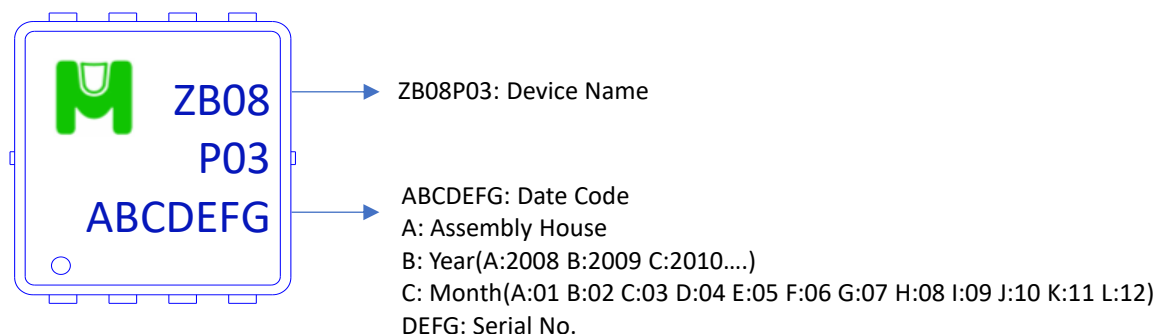


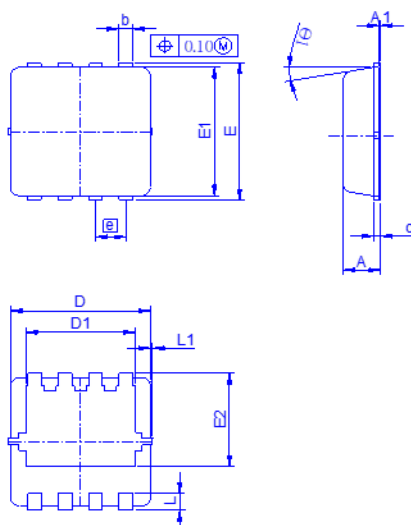
Fig.11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMZB08P03V for EDFN 3x3

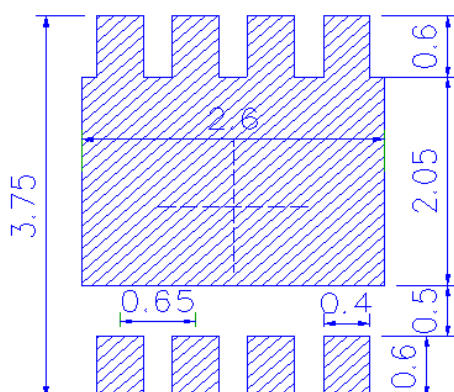


Outline Drawing

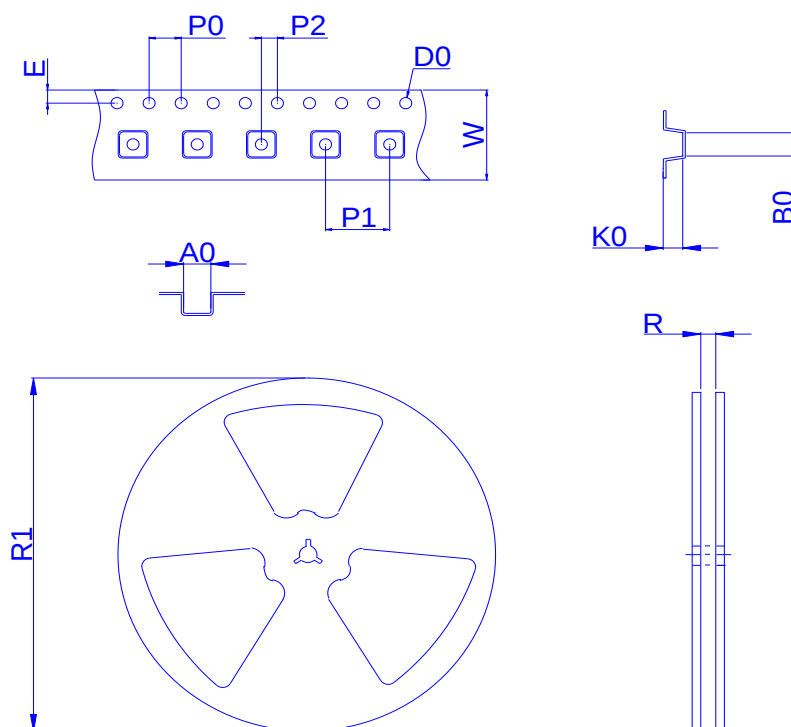


Dimension	A	A1	b	c	D	D1	E	E1	E2	e	L	L1	θ1
Min.	0.650	0.000	0.200	0.100	2.900	2.150	3.100	2.900	1.530	0.550	0.250	-	0°
Typ.	0.750	-	0.300	0.150	3.000	2.450	3.200	3.000	1.970	0.650	0.400	0.075	10°
Max.	0.900	0.050	0.400	0.250	3.300	2.740	3.500	3.300	2.590	0.750	0.600	0.150	14°

Footprint



◆ Tape&Reel Information:5000pcs/Reel



Package	EDFN3X3
Reel	13"
Device orientation	FEED DIRECTION

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	3.6	3.6	1.55	1.7	1.2	4	8	2	12	12.4	330
±	0.3	0.3	0.2	0.2	0.2	0.1	0.1	0.1	1	2	2