杰力科技股份有限公司
Excelliance MOS Corporation

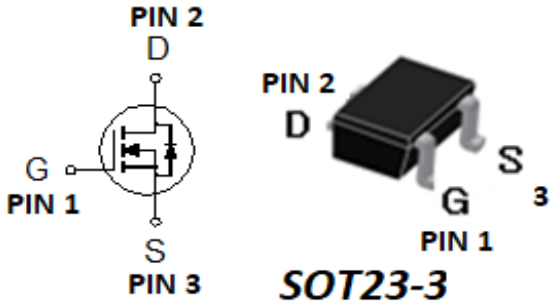
EMVB70N06JS

Single N-Channel Logic Level Enhancement Mode Field Effect Transistor

▪Product Summary:

	N-CH
BV_{DSS}	60V
$R_{DSON\ (MAX.)}$@V_{GS}=10V	75mΩ
$R_{DSON\ (MAX.)}$@V_{GS}=4.5V	83mΩ
I_D @T_C=25°C	10A
I_D @T_A=25°C	2.8A

▪ Pin Description:



Single N Channel MOSFET
UIS, Rg 100% Tested
RoHS & Halogen Free & TSCA Compliant
AEC-Q101 Qualified

▪ ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	10	A
	T_C = 100 °C		7	
Continuous Drain Current	T_A = 25 °C	I_D	2.8	
	T_A = 70 °C		2	
Pulsed Drain Current[1]		I_{DM}	11	
Avalanche Current		I_{AS}	8	
Avalanche Energy	L = 1mH	EAS	32	mJ
Repetitive Avalanche Energy[2]	L = 0.5mH	EAR	16	
Power Dissipation	T_C = 25 °C	P_D	17.6	W
	T_C = 100 °C		8.8	
Power Dissipation	T_A = 25 °C	P_D	1.3	W
	T_A = 70 °C		0.9	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 175	°C

▪ 100% UIS testing in condition of VD=40V, L=1mH, VG=10V, IL=5A, Rated VDS=60V N-CH

▪THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	UNIT
Junction-to-Lead		$R_{\theta JC}$	8.5	°C/W
Junction-to-Ambient[3]	t≦10s	$R_{\theta JA}$	77	
	Steady-State	$R_{\theta JA}$	114	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle < 1%

[3]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C.

[4]Guarantee by Engineering test

▪ ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage[4]	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	60			V
Gate Threshold Voltage[4]	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	0.9	1.5	2.0	
Gate-Body Leakage[4]	I_{GSS}	V_{DS} = 0V, V_{GS} = ±16V			±100	nA
Zero Gate Voltage Drain Current[4]	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V			1	μA
		V_{DS} =60V, V_{GS} =0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	10			A
Drain-Source On-State Resistance[1,4]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 5A		63	75	mΩ
		V_{GS} = 4.5V, I_D = 3A		69	83	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 5A		15		S
DYNAMIC						
Input Capacitance[5]	C_{iss}	V_{GS} = 0V, V_{DS} = 30V, f = 1MHz		544		pF
Output Capacitance[5]	C_{oss}			39		
Reverse Transfer Capacitance[5]	C_{rss}			32		
Gate Resistance[4,5]	R_g	f = 1MHz		1.3		Ω
Total Gate Charge[1,2,5]	Q_g(V_{GS}=10V)	V_{DS} = 30V, V_{GS} = 10V, I_D = 5A		16		nC
	Q_g(V_{GS}=4.5V)			8		
Gate-Source Charge[1,2,5]	Q_{gs}			2		
Gate-Drain Charge[1,2,5]	Q_{gd}			3		
Turn-On Delay Time[1,2,5]	$t_{d(on)}$	V_{DS} = 30V, V_{GS} = 10V, I_D = 5A , Rg = 6Ω		5		nS
Rise Time[1,2,5]	t_r			7		
Turn-Off Delay Time[1,2,5]	$t_{d(off)}$			24		
Fall Time[1,2,5]	t_f			15		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				10	A
Pulsed Current[3]	I_{SM}				11	
Forward Voltage[1,4]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.2	V
Reverse Recovery Time[5]	t_{rr}	I_F = I_S, dI_F/dt = 100A / μS		16		nS
Peak Reverse Recovery Current[5]	$I_{RM(REC)}$			2.2		A
Reverse Recovery Charge[5]	Q_{rr}			12		nC

[1]Pulse test : Pulse Width ≦ 300 usec, Duty Cycle ≦ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

[4]Guarantee by FT test Item

[5]Guarantee by Engineering test

▪TYPICAL CHARACTERISTICS

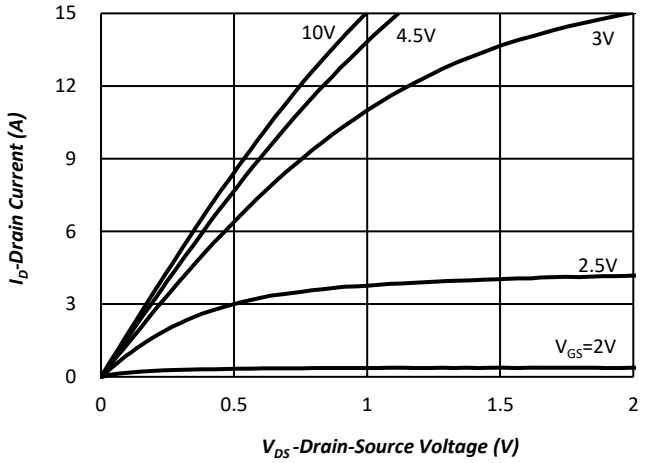


Fig.1 Typical Output Characteristics

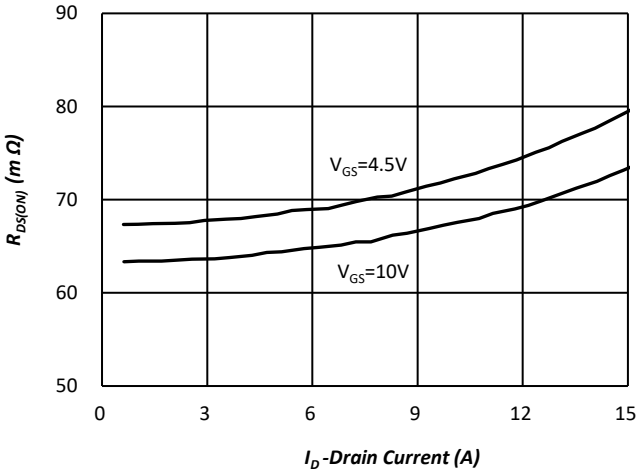


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

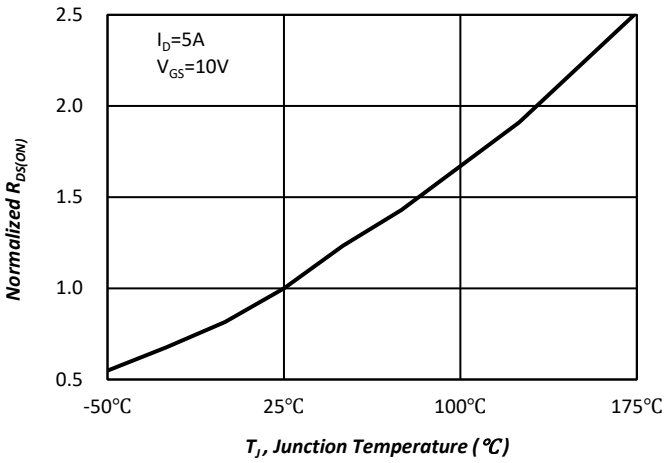


Fig.3 Normalized On-Resistance v.s. Junction Temperature

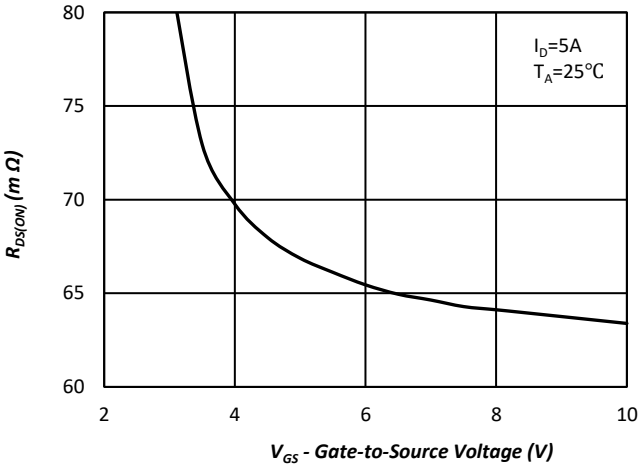


Fig.4 On-Resistance v.s. Gate Voltage

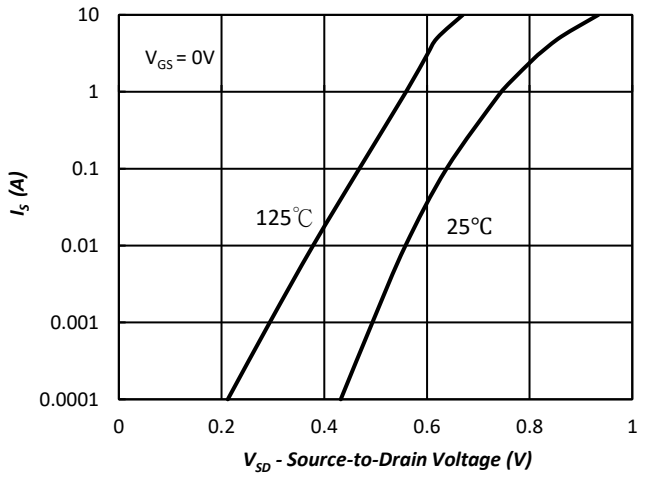


Fig.5 Forward Characteristic of Reverse Diode

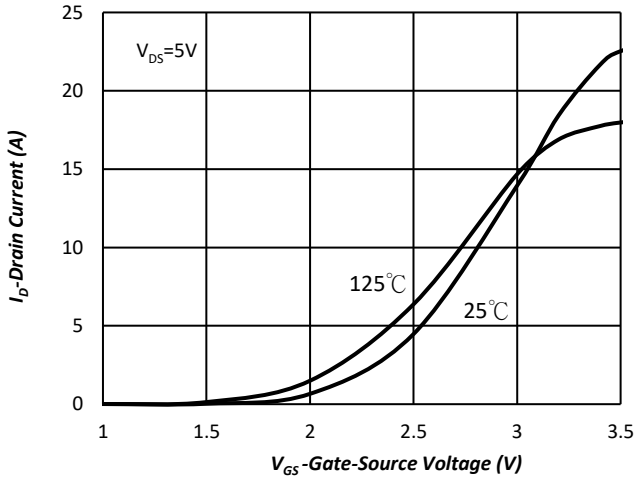


Fig.6 Transfer Characteristics

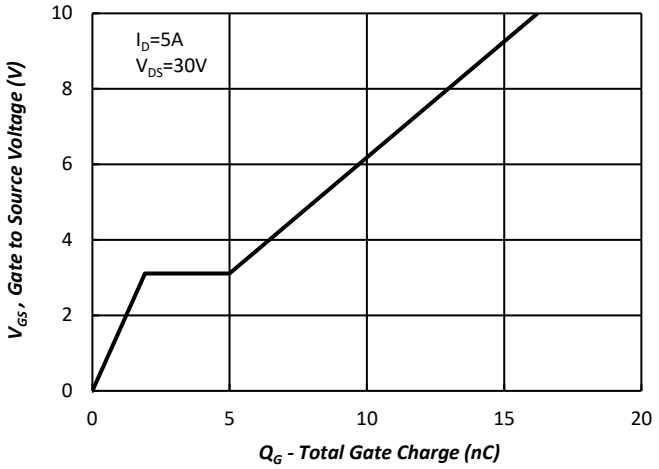


Fig.7 Gate Charge Characteristics

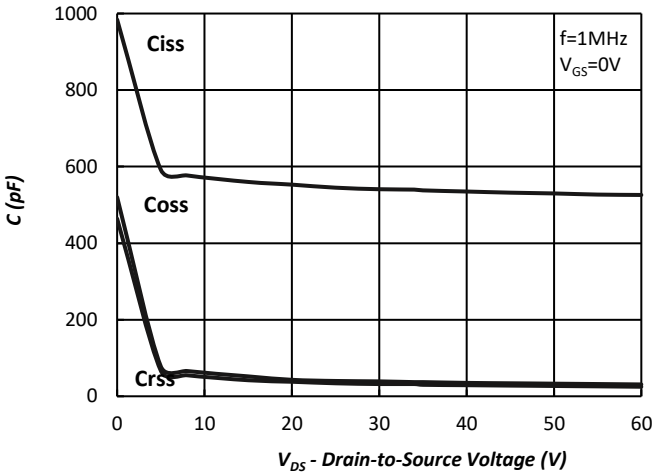


Fig.8 Typical Capacitance Characteristics

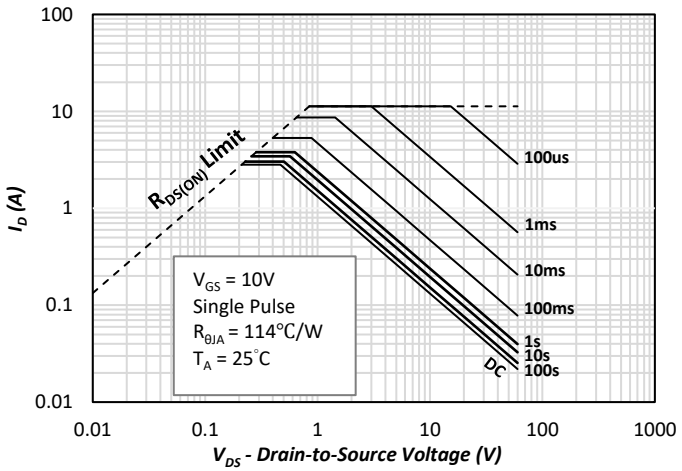


Fig 9. Maximum Safe Operating Area

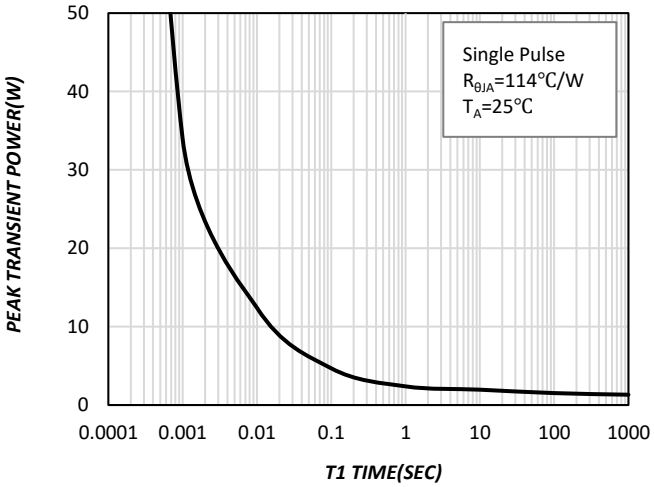


Fig 10. Single Pulse Maximum Power Dissipation

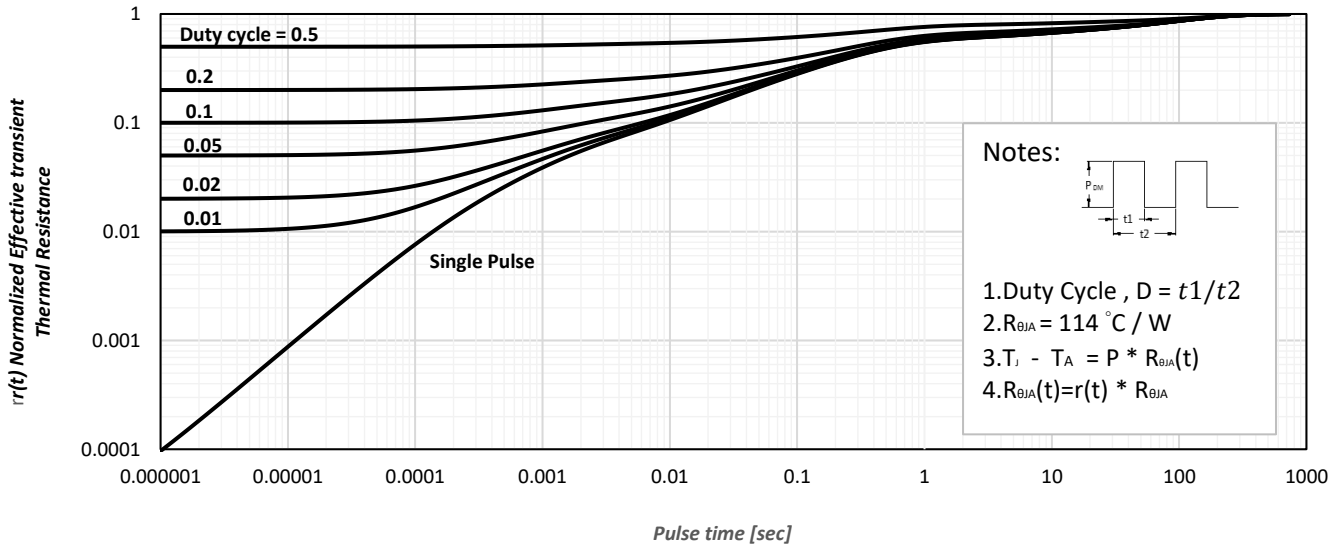


Fig 11. Effective Transient Thermal Impedance

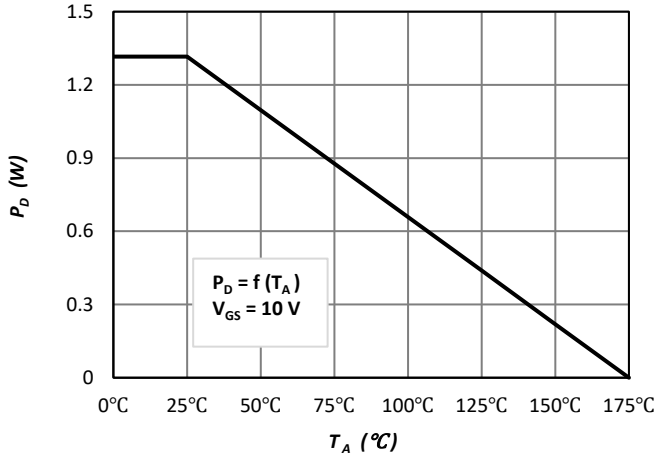


Fig.12 Power dissipation

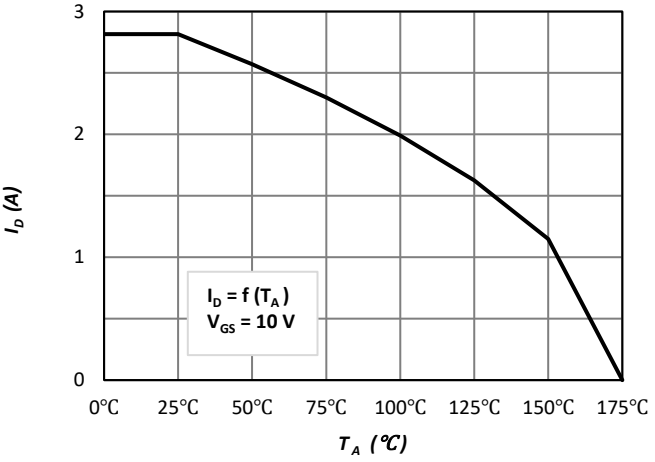
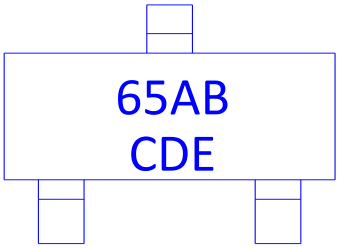


Fig.13 Drain current

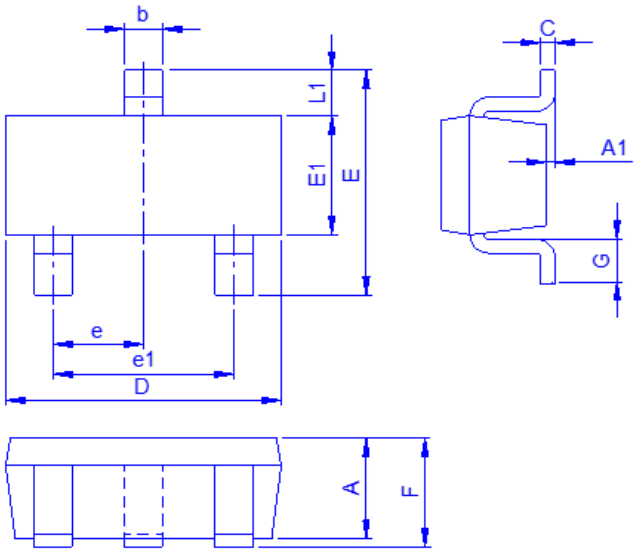
Ordering & Marking Information:

Device Name: EMVB70N06JS for SOT23-3



65 for EMVB70N06JS
A: Year(A:2008 B:2009 C:2010….)
B: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)
CDE: Serial No.

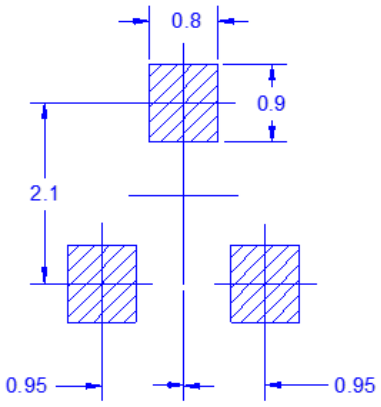
Outline Drawing



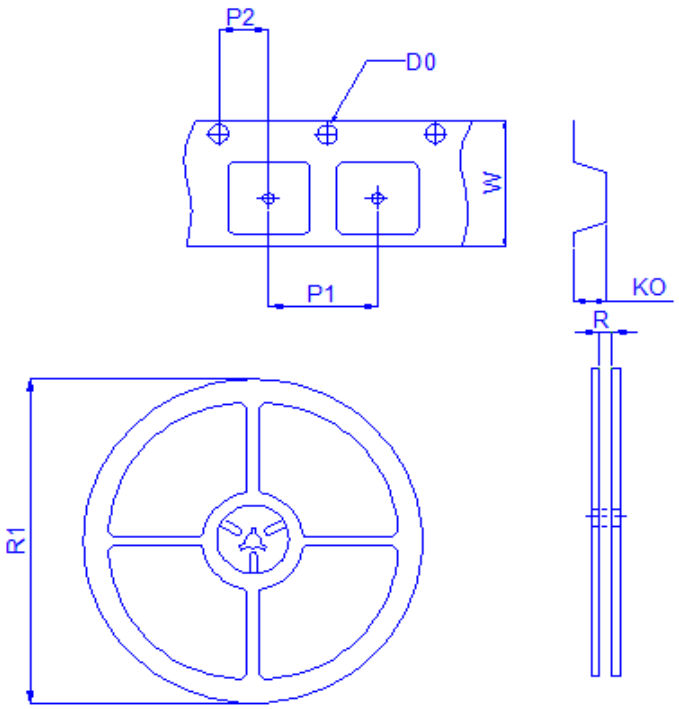
Dimension in mm

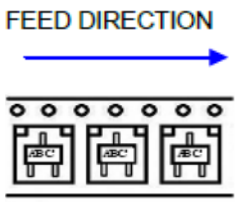
Dimension	A	A1	b	C	D	E	E1	e	e1	F	G	L1
Min.	0.88	-	0.3	0.13	2.8	2.25	1.2	0.9	1.8	0.89	0.3	
Typ.	0.95	-	0.4	0.17	2.9	2.5	1.3	0.95	1.9		0.45	0.55
Max.	1.1	0.1	0.5	0.2	3	2.64	1.4	1	2	1.15	0.6	

Footprint



◆ **Tape&Reel Information:3000pcs/Reel**



Package	SOT23-3
Reel	7”
Device orientation	

Dimension in mm

Dimension	Carrier tape					Reel	
	D0	K0	P1	P2	W	R	R1
Typ.	1.53	1.45	4	2	8	8.5	178
±	0.2	0.5	0.2	0.2	0.5	REF	REF