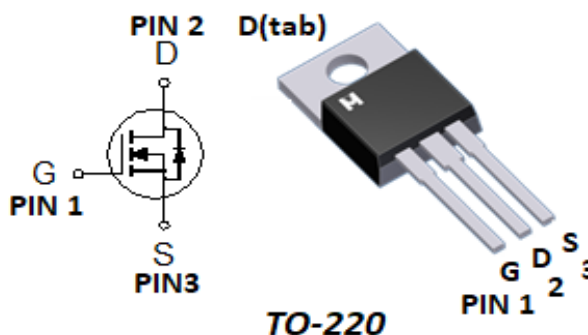


Single N-Channel Logic Level Enhancement Mode Field Effect Transistor

•Product Summary:

	N-CH
BVDSS	100V
$R_{DS(on)}(MAX.)@V_{GS}=10V$	8.5mΩ
$R_{DS(on)}(MAX.)@V_{GS}=4.5V$	10.5mΩ
$I_D @T_C=25^{\circ}C$	100A
$I_D @T_A=25^{\circ}C$	12A

• Pin Description:



Single N Channel MOSFET

UIS, Rg 100% Tested

RoHS & Halogen Free & TSCA Compliant



•ABSOLUTE MAXIMUM RATINGS ($T_C = 25^{\circ}C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^{\circ}C$	I_D	100	A
	$T_C = 100^{\circ}C$		63	
Continuous Drain Current	$T_A = 25^{\circ}C$	I_D	12	
	$T_A = 70^{\circ}C$		9	
Pulsed Drain Current ¹		I_{DM}	165	
Avalanche Current		I_{AS}	30	mJ
Avalanche Energy	$L = 0.1mH$	EAS	45	
Repetitive Avalanche Energy ²	$L = 0.05mH$	EAR	22.5	
Power Dissipation	$T_C = 25^{\circ}C$	P_D	139	W
	$T_C = 100^{\circ}C$		56	
Power Dissipation	$T_A = 25^{\circ}C$	P_D	2.0	W
	$T_A = 70^{\circ}C$		1.3	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^{\circ}C$

•THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		0.9	$^{\circ}C/W$
Junction-to-Ambient ³	$R_{\theta JA}$		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle < 1%

³The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^{\circ}C$.

⁴Guarantee by Engineering test



▪ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250uA	100			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	1.5	2	2.5	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} =80V, V _{GS} = 0V			1	uA
		V _{DS} =70V, V _{GS} =0V, T _J = 125°C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 5V, V _{GS} = 10V	100			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 24A		6.5	8.5	mΩ
		V _{GS} = 4.5V, I _D = 20A		8	10.5	
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 50V, f = 1MHz		2975		pF
Output Capacitance ⁵	C _{oss}			503		
Reverse Transfer Capacitance ⁵	C _{rss}			28		
Gate Resistance ^{4,5}	R _g	f = 1MHz		1.0		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 50V, V _{GS} = 10V, I _D = 24A		46.9		nC
	Q _g (V _{GS} =4.5V)			25.1		
Gate-Source Charge ^{1,2,5}	Q _{gs}			7.8		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			10.9		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 50V, V _{GS} = 10V, I _D = 5A , R _g = 6Ω		14.0		nS
Rise Time ^{1,2,5}	t _r			16.3		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			52.4		
Fall Time ^{1,2,5}	t _f			46.5		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				100	A
Pulsed Current ³	I _{SM}				165	
Forward Voltage ^{1,4}	V _{SD}	I _F = 24A, V _{GS} = 0V			1.2	V
Reverse Recovery Time ⁵	t _{rr}	I _F = 40A, dI _F /dt = 100A / uS		52.4		nS
Reverse Recovery Charge ⁵	Q _{rr}			64.8		nC

¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.



•TYPICAL CHARACTERISTICS

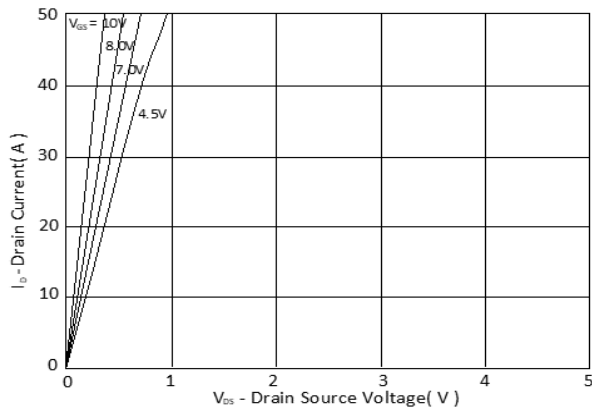


Fig.1 Typical Output Characteristics

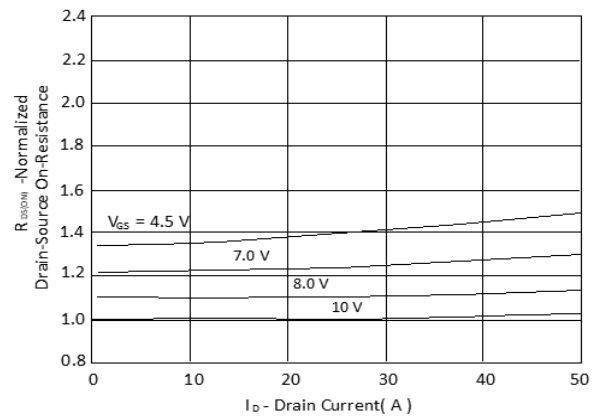


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

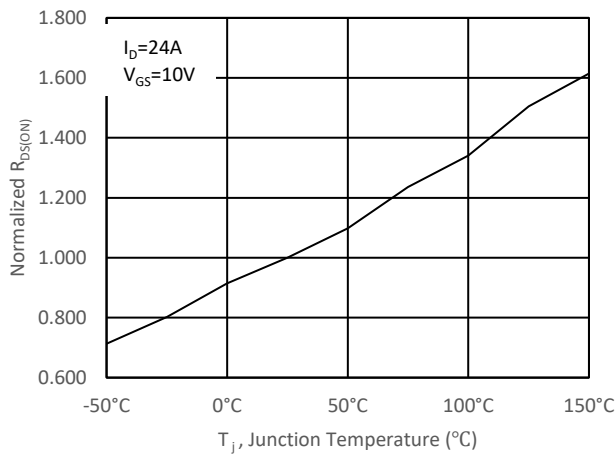


Fig.3 Normalized On-Resistance v.s. Junction Temperature

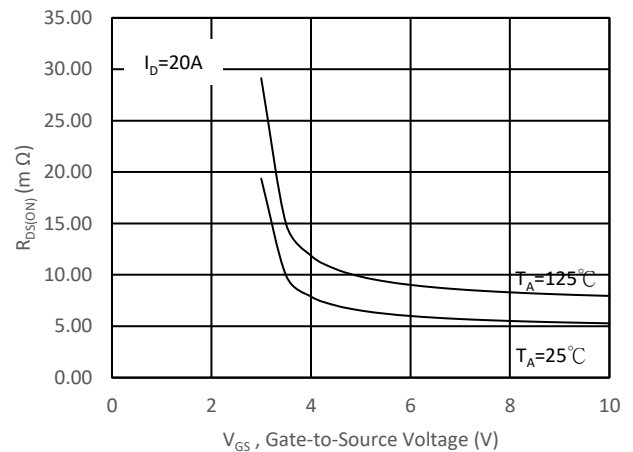


Fig.4 On-Resistance v.s. Gate Voltage

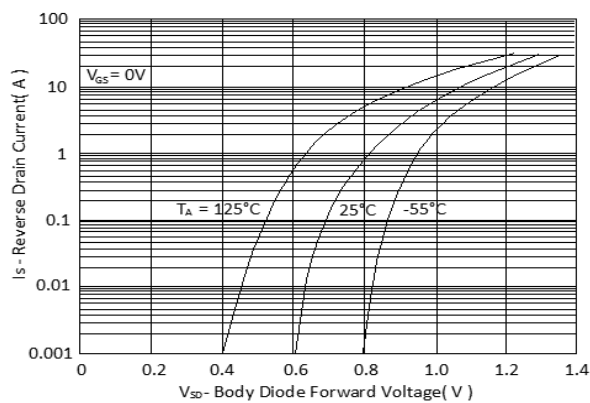


Fig.5 Forward Characteristic of Reverse Diode

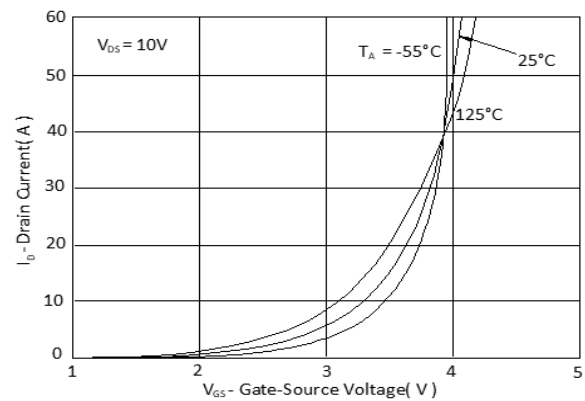


Fig.6 Transfer Characteristics

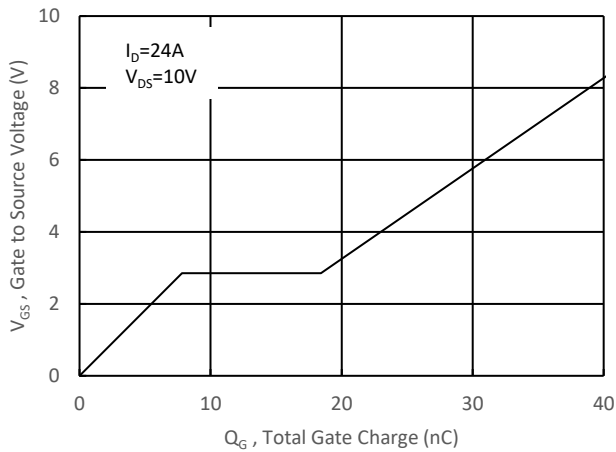


Fig.7 Gate Charge Characteristics

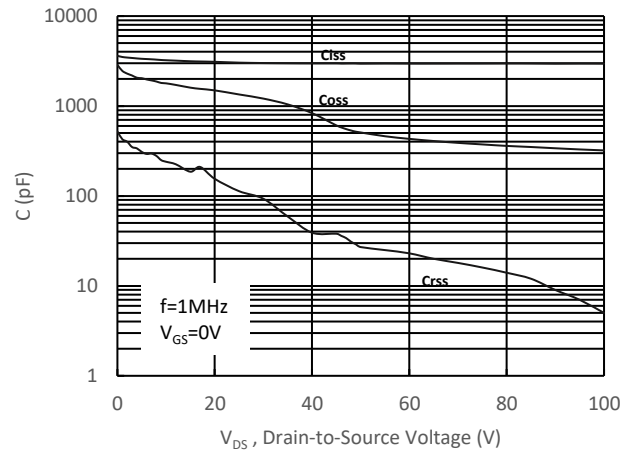


Fig.8 Typical Capacitance Characteristics

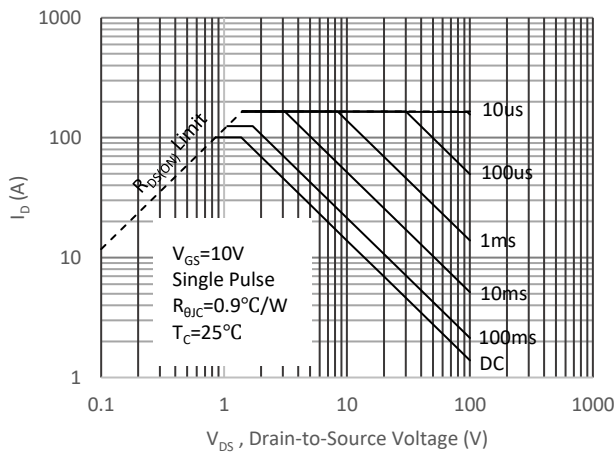


Fig.9. Maximum Safe Operating Area

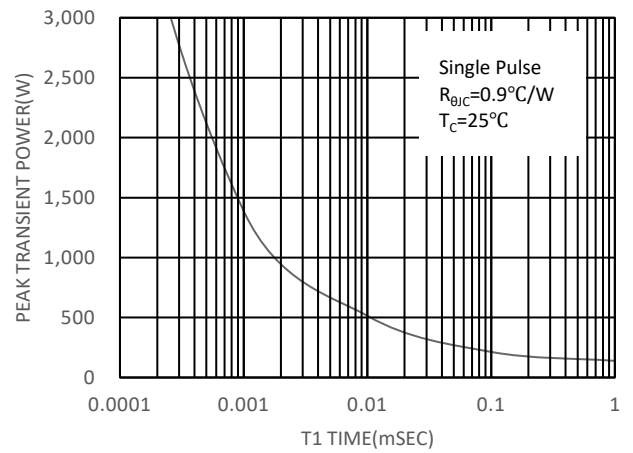


Fig.10. Single Pulse Maximum Power Dissipation

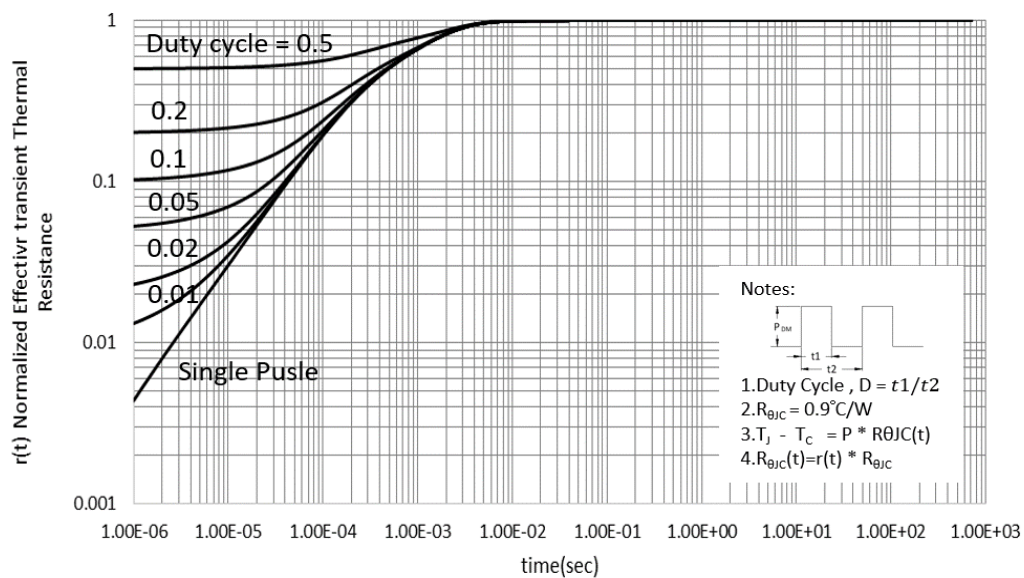
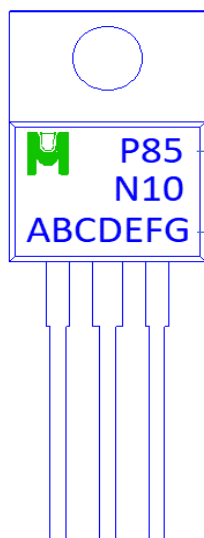


Fig.11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMP85N10E for TO-220



P85N10: Device Name

ABCDEFGH: Date Code

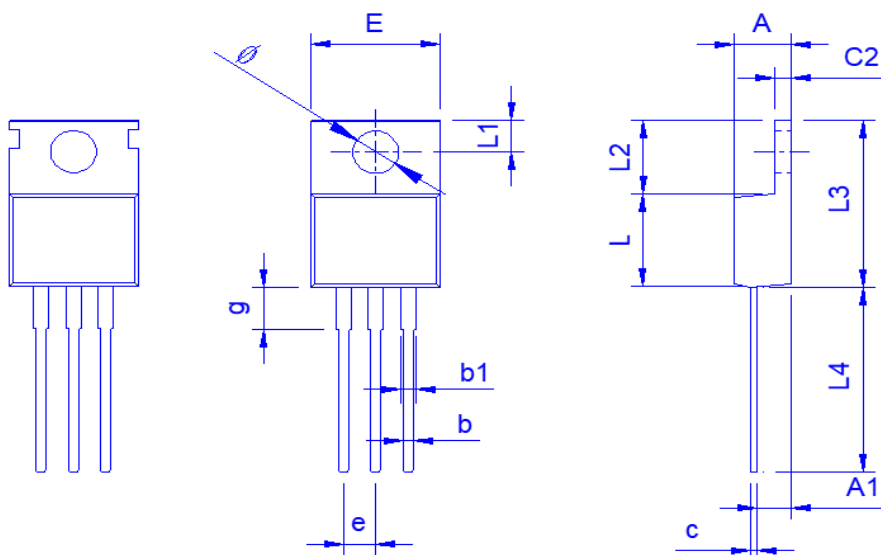
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

Outline Drawing



Dimension	A	A1	b	b1	c	c2	E	L	L1	L2	L3	L4	Ø
Min.	4.240	2.250	0.700	1.170	0.310	1.150	9.910	8.500	2.590	6.100	14.700	12.700	3.400
Typ.	4.440	2.400	0.800	1.550	0.500	1.270	10.160	8.920	2.800	6.300	15.370	13.720	3.840
Max.	4.700	2.820	0.910	1.750	0.650	1.400	10.360	9.750	3.250	6.800	16.900	13.970	3.935

Dimension	e	g
Min.	2.440	2.850
Typ.	2.540	3.800
Max.	2.640	4.000

◆ Tube Information: 50pcs/Tube (1000pcs/Box)

