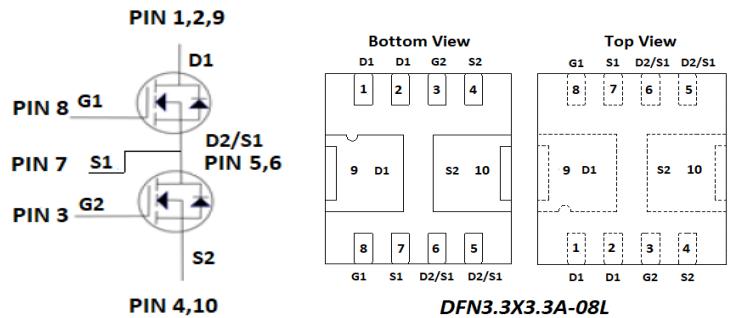


Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

•Product Summary:

	Q1	Q2
BV_{DSS}	30V	30V
$R_{DSON (MAX.)}@V_{GS}=10V$	5.2m Ω	6.4m Ω
$R_{DSON (MAX.)}@V_{GS}=4.5V$	6.2m Ω	7.8m Ω
$I_D @T_C=25^\circ C$	57A	48A
$I_D @T_A=25^\circ C$	21A	17A

• Pin Description:



Dual N Channel MOSFET

UIS, Rg 100% Tested

RoHS & Halogen Free & TSCA Compliant

•ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ C$ Unless Otherwise Noted)



PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS		UNIT	
		Q1	Q2		
Gate-Source Voltage	V_{GS}	± 12	± 12	V	
Continuous Drain Current	I_D	$T_C = 25^\circ C$	57	48	A
		$T_C = 100^\circ C$	36	30	
Continuous Drain Current	I_D	$T_A = 25^\circ C$	21	17	
		$T_A = 70^\circ C$	17	13	
Pulsed Drain Current ¹	I_{DM}	182	128		
Avalanche Current	I_{AS}	60	45		
Avalanche Energy	EAS	L = 0.1mH	180	101	mJ
		L = 0.01mH	18	10	
Repetitive Avalanche Energy ²	EAR	90	51		
Power Dissipation	P_D	$T_C = 25^\circ C$	28	25	W
		$T_C = 100^\circ C$	11	10	
Power Dissipation	P_D	$T_A = 25^\circ C$	3.1	3.1	W
		$T_A = 70^\circ C$	2	2	
Operating Junction & Storage Temperature Range	T_j, T_{stg}	-55 to 150		$^\circ C$	

• 100% UIS testing in condition of $V_D=25V, L=0.01mH, V_G=10V, I_L=36A, R_G=25\Omega$, Rated $V_{DS}=30V$ N-CH_Q1

• 100% UIS testing in condition of $V_D=25V, L=0.01mH, V_G=10V, I_L=27A, R_G=25\Omega$, Rated $V_{DS}=30V$ N-CH_Q2

•THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM		UNIT
			Q1	Q2	
Junction-to-Case	$R_{\theta JC}$		4.55	5	$^\circ C/W$
Junction-to-Ambient ³	$R_{\theta JA}$	$t \leq 10s$	40	40	
		Steady-State	60	60	

¹Pulse width limited by maximum junction temperature.

²Duty cycle < 1%

³The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ C$.

⁴Guarantee by Engineering test



▪ Q1_ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	30			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.2	1.6	2.2	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 30V, V _{GS} = 0V			1	μA
		V _{DS} = 30V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	57			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A		4.2	5.2	mΩ
		V _{GS} = 4.5V, I _D = 20A		5.2	6.2	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 20A		100		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		1000		pF
Output Capacitance ⁵	C _{oss}			370		
Reverse Transfer Capacitance ⁵	C _{rss}			30		
Gate Resistance ^{4,5}	R _g	f = 1MHz		0.8		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 15V, V _{GS} = 10V, I _D = 20A		20		nC
	Q _g (V _{GS} =4.5V)			9		
Gate-Source Charge ^{1,2,5}	Q _{gs}			3.9		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			2		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}			6.8		
Rise Time ^{1,2,5}	t _r		12			
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}		18.3			
Fall Time ^{1,2,5}	t _f		3			
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				57	A
Pulsed Current ³	I _{SM}				182	
Forward Voltage ^{1,4}	V _{SD}	I _F = I _S , V _{GS} = 0V			1.2	V
Reverse Recovery Time ⁵	t _{rr}	I _F = I _S , dI _F /dt = 400A / μS		15.3		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			2.3		A
Reverse Recovery Charge ⁵	Q _{rr}			17.8		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

•Q1_TYPICAL CHARACTERISTICS

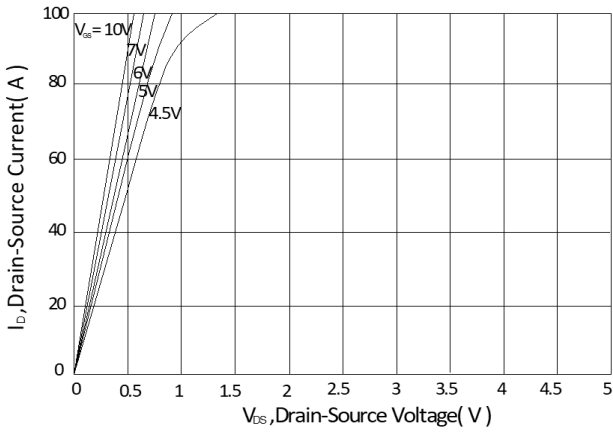


Fig.1 Typical Output Characteristics

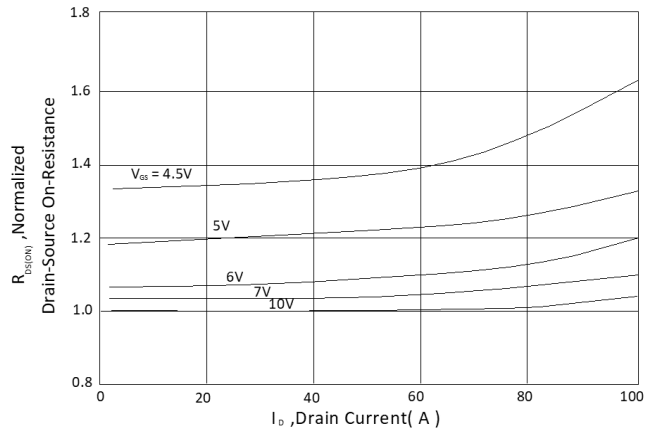


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

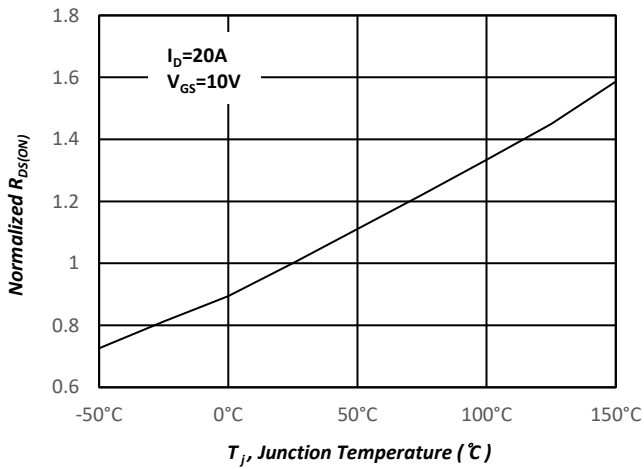


Fig.3 Normalized On-Resistance v.s. Junction Temperature

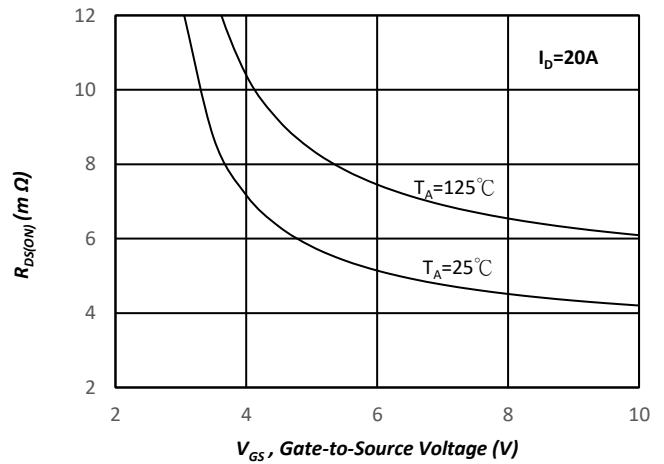


Fig.4 On-Resistance v.s. Gate Voltage

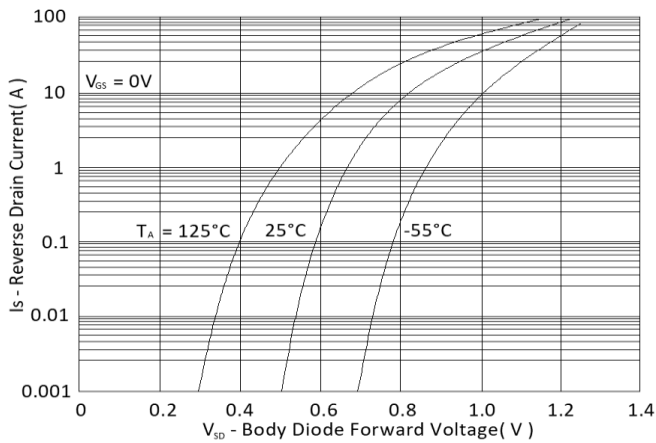


Fig.5 Forward Characteristic of Reverse Diode

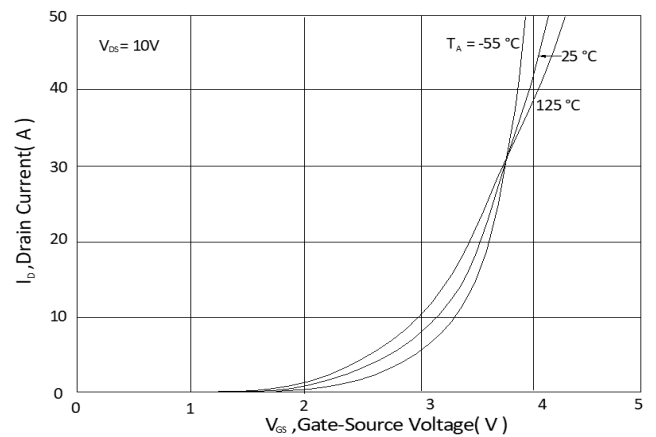


Fig.6 Transfer Characteristics

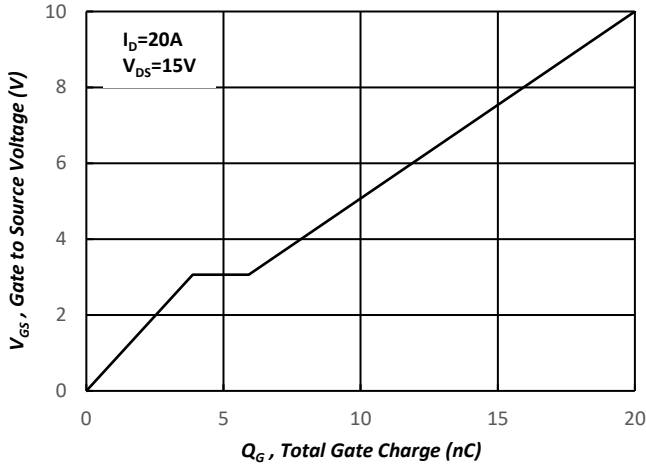


Fig.7 Gate Charge Characteristics

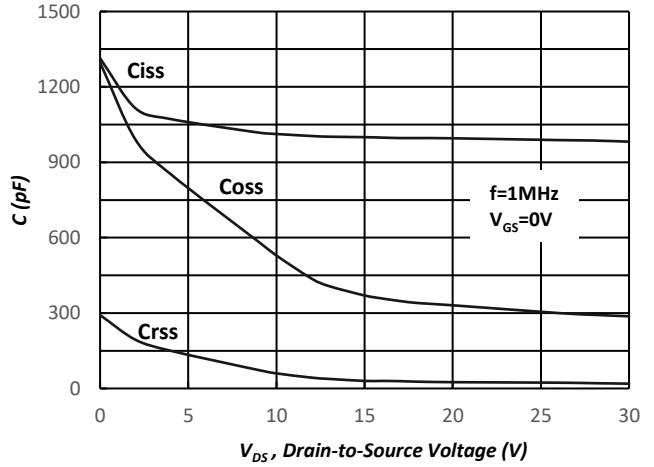


Fig.8 Typical Capacitance Characteristics

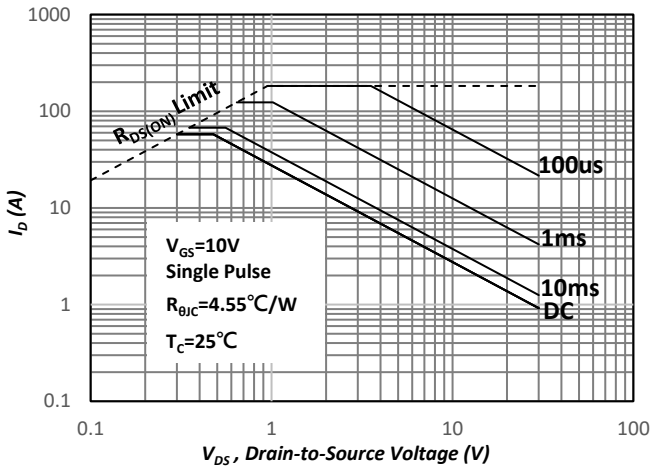


Fig.9. Maximum Safe Operating Area

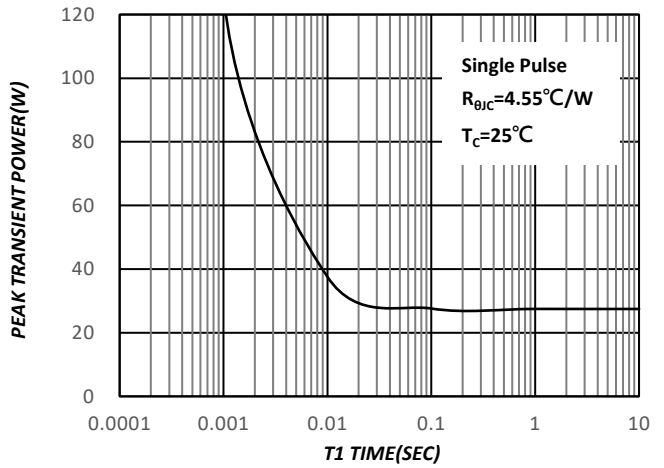


Fig.10. Single Pulse Maximum Power Dissipation

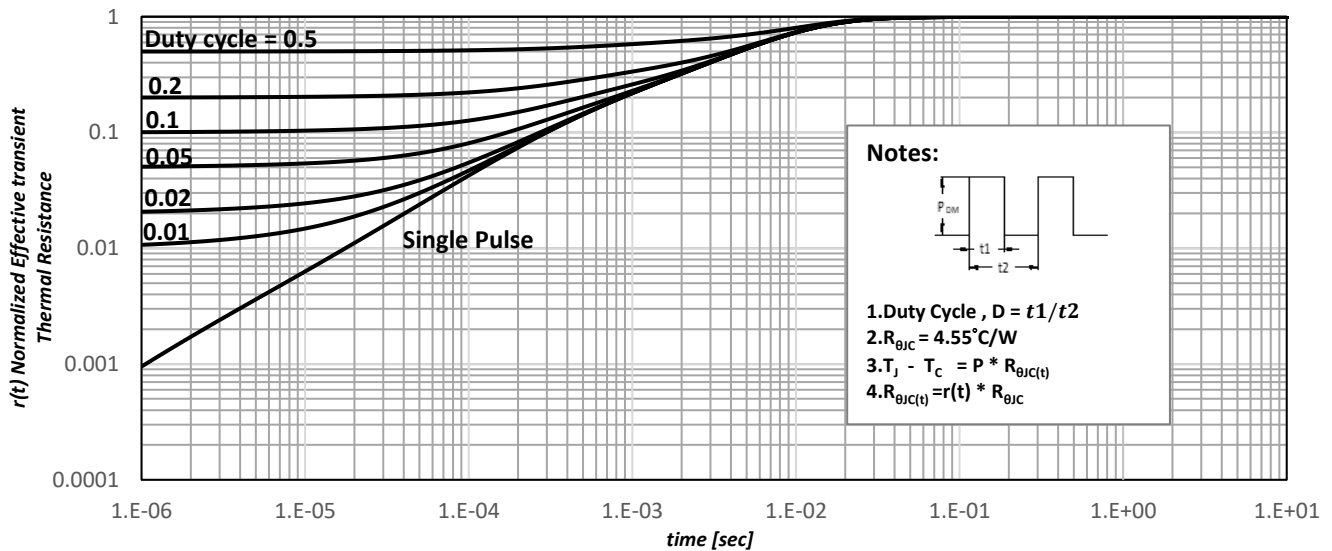


Fig.11. Effective Transient Thermal Impedance



▪ Q2_ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	30			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.2	1.6	2.2	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 30V, V _{GS} = 0V			1	μA
		V _{DS} = 30V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	48			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 18A		4.9	6.4	mΩ
		V _{GS} = 4.5V, I _D = 18A		6.0	7.8	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 18A		100		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		990		pF
Output Capacitance ⁵	C _{oss}			400		
Reverse Transfer Capacitance ⁵	C _{rss}			38		
Gate Resistance ^{4,5}	R _g	f = 1MHz		1.7		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 15V, V _{GS} = 10V, I _D = 18A		18		nC
	Q _g (V _{GS} =4.5V)			8.5		
Gate-Source Charge ^{1,2,5}	Q _{gs}			3.9		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			2		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}			7.2		
Rise Time ^{1,2,5}	t _r		12.4			
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}		18.6			
Fall Time ^{1,2,5}	t _f		2.9			
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				48	A
Pulsed Current ³	I _{SM}				128	
Forward Voltage ^{1,4}	V _{SD}	I _F = I _S , V _{GS} = 0V			1.2	V
Reverse Recovery Time ⁵	t _{rr}	I _F = I _S , dI _F /dt = 400A / μS		16.2		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			2.3		A
Reverse Recovery Charge ⁵	Q _{rr}			18.9		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

Q2_TYPICAL CHARACTERISTICS

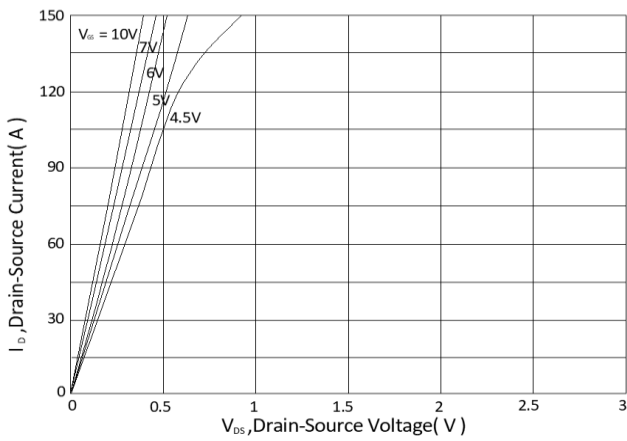


Fig.1 Typical Output Characteristics

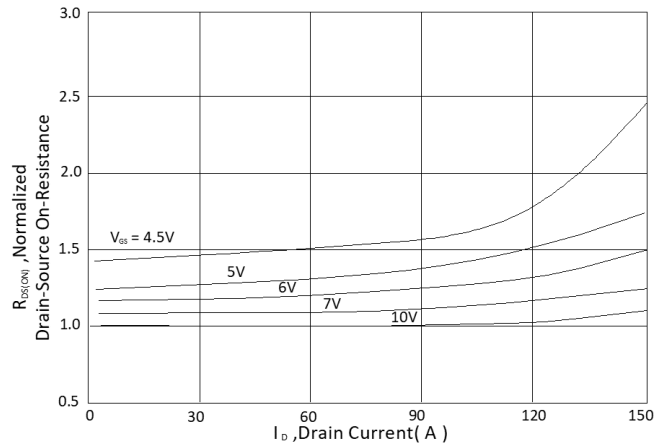


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

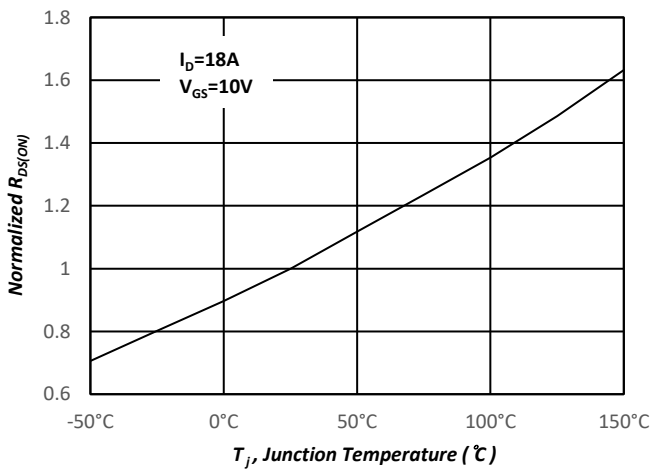


Fig.3 Normalized On-Resistance v.s. Junction Temperature

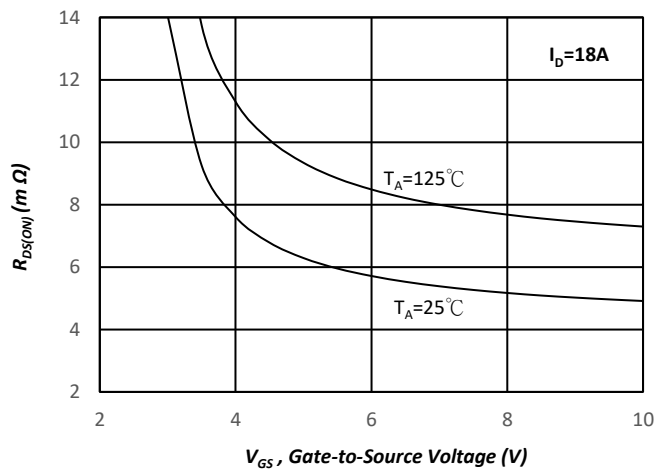


Fig.4 On-Resistance v.s. Gate Voltage

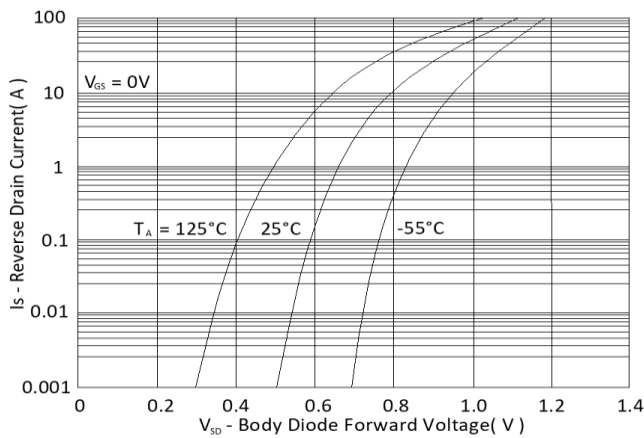


Fig.5 Forward Characteristic of Reverse Diode

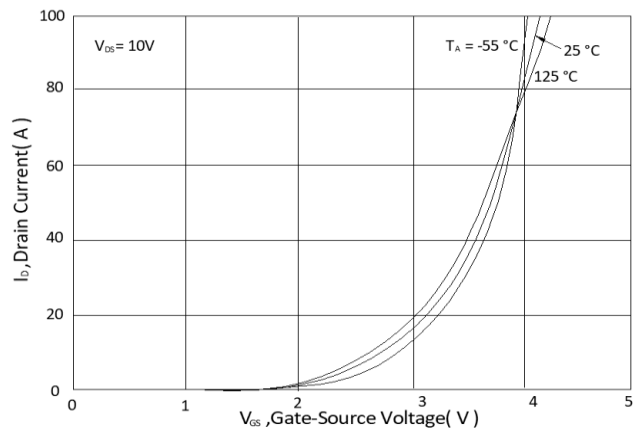
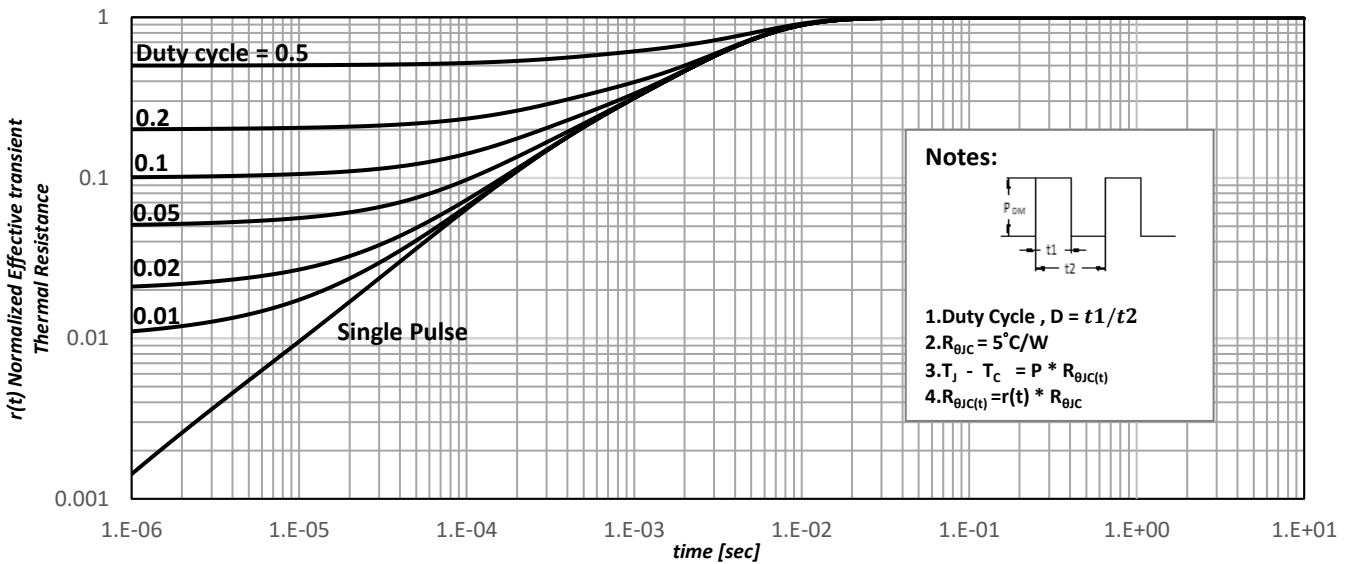
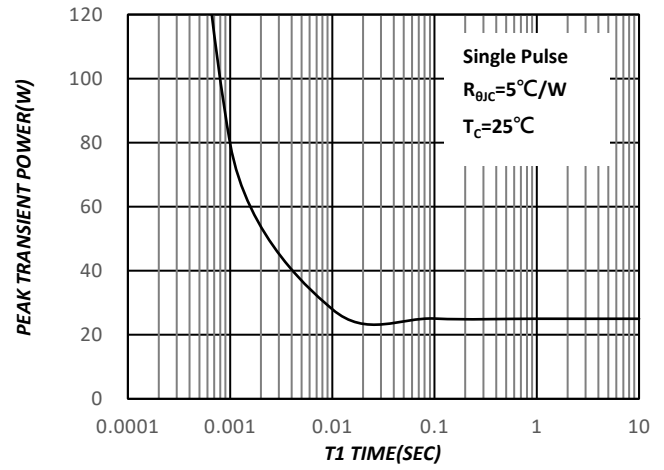
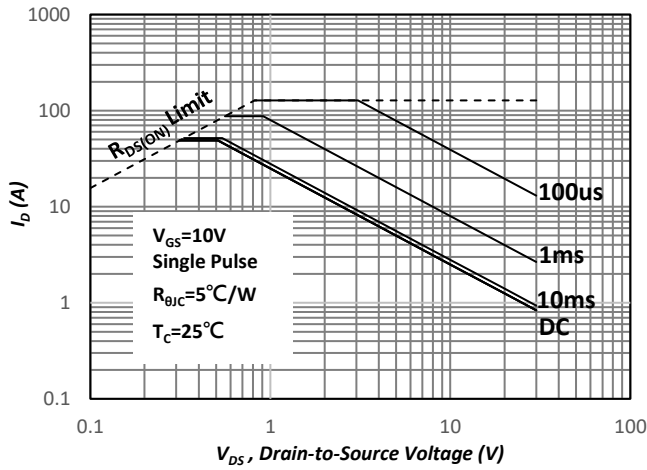
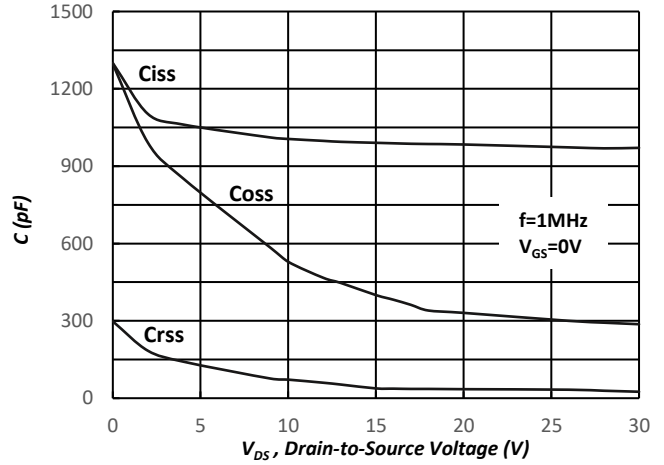
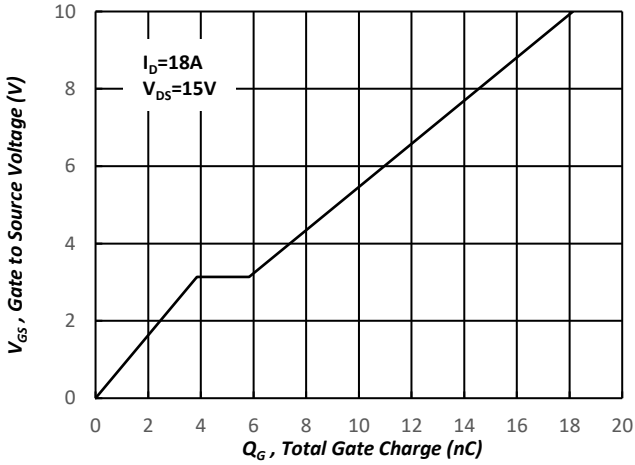


Fig.6 Transfer Characteristics



Ordering & Marking Information:

Device Name: EMP65Q03VSCS for DFN3.3X3.3A-08L



→ P65Q03S: Device Name

→ ABCDEFG: Date Code

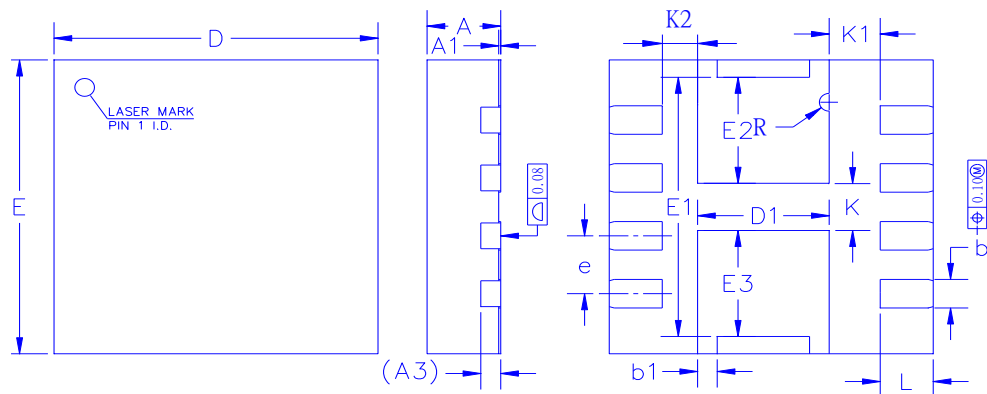
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

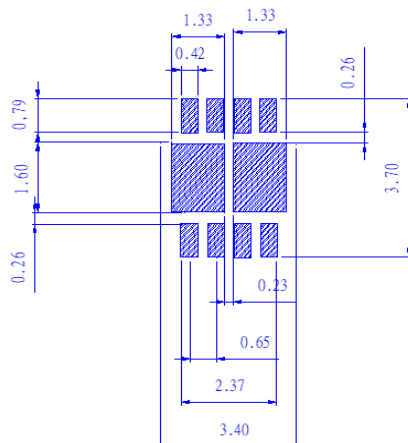
Outline Drawing



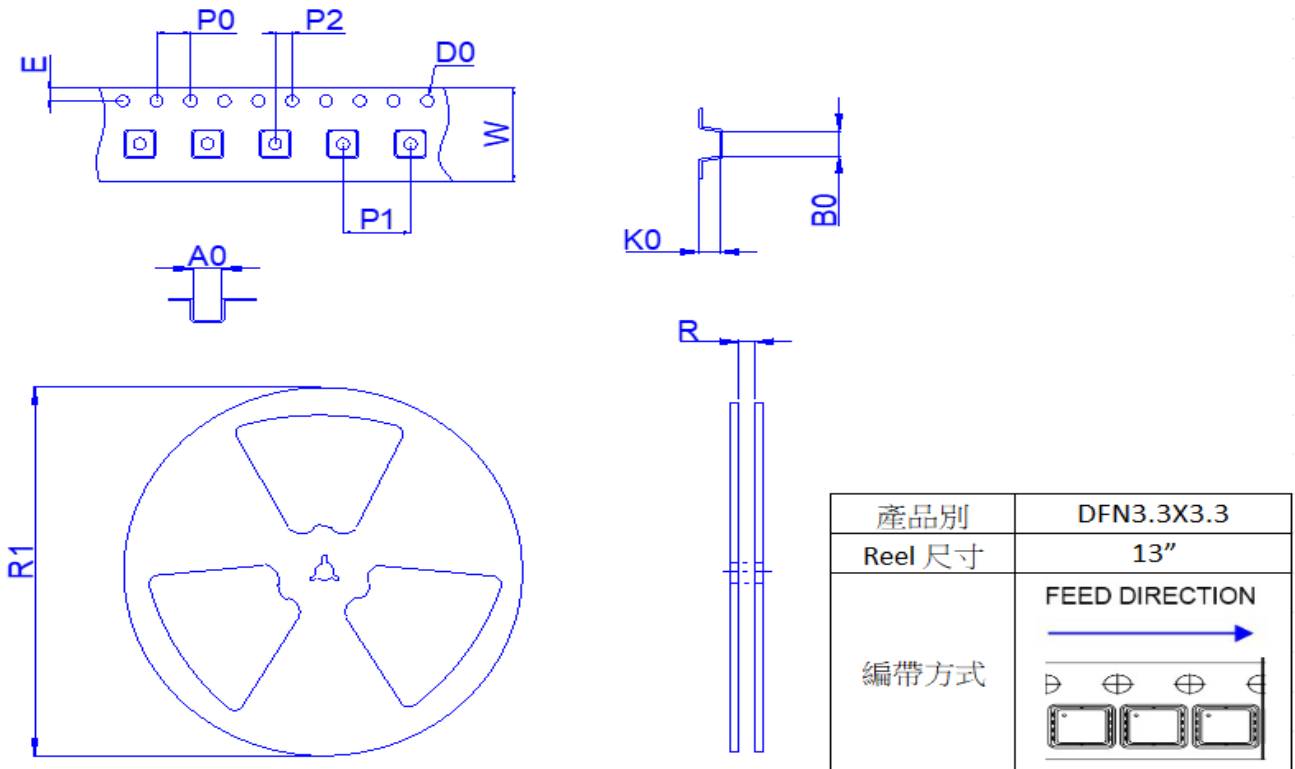
Dimension	A	A1	A3	b	b1	D	E	D1	E1	E2	E3	e
Min.	0.7	-	-	0.27	0.15	3.2	3.2	1.24	2.8	1.09	1.09	0.55
Typ.	0.75	0.02	0.203	0.32	0.2	3.3	3.3	1.34	2.91	1.19	1.19	0.65
Max.	0.8	0.05	-	0.37	0.25	3.4	3.4	1.44	3	1.29	1.29	0.75

Dimension	K	K1	K2	L	R
Min.	0.43	0.42	0.26	0.44	-
Typ.	0.53	0.52	0.36	0.54	0.1
Max.	0.63	0.62	0.46	0.64	-

Footprint



◆ Tape&Reel Information: 5000pcs/Reel



Dimension in mm

Dimension	Carrier tape								Reel		
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	3.6	3.6	1.55	1.7	1.2	4	8	2	12	12.4	330
±	0.3	0.3	0.2	0.2	0.2	0.1	0.1	0.1	1	2	2