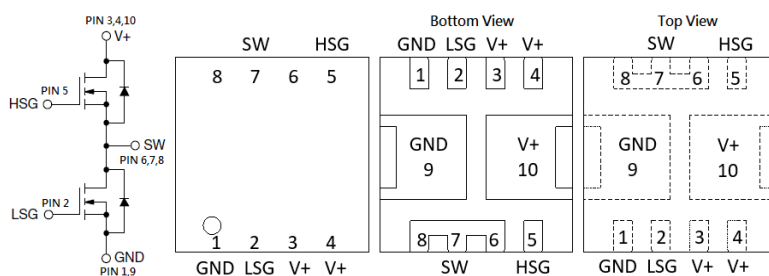


**Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor**
**•Product Summary:**

	Q1	Q2
$BV_{DSS}$	30V	30V
$R_{DS(on) (MAX.)}@V_{GS}=10V$	2.7m $\Omega$	2.4m $\Omega$
$R_{DS(on) (MAX.)}@V_{GS}=4.5V$	3.7m $\Omega$	3.5m $\Omega$
$I_D @T_C=25^\circ C$	68A	91A
$I_D @T_A=25^\circ C$	17A	18A

**• Pin Description:**

**DFN3.3X3.3E-08(Dual)**

Dual N Channel MOSFET

UIS, Rg 100% Tested

RoHS &amp; Halogen Free &amp; TSCA Compliant

**•ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ C$  Unless Otherwise Noted)**


PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS		UNIT	
		Q1	Q2		
Gate-Source Voltage	$V_{GS}$	$\pm 12$	$\pm 12$	V	
Continuous Drain Current	$I_D$	$T_C = 25^\circ C$	68	91	A
		$T_C = 100^\circ C$	43	57	
Continuous Drain Current	$I_D$	$T_A = 25^\circ C$	17	18	
		$T_A = 70^\circ C$	13	14	
Pulsed Drain Current <sup>1</sup>	$I_{DM}$	162	244		
Avalanche Current	$I_{AS}$	75	66		
Avalanche Energy	$EAS$	28	22	mJ	
Repetitive Avalanche Energy <sup>2</sup>	$EAR$	141	109		
Power Dissipation	$P_D$	$T_C = 25^\circ C$	24	36	W
		$T_C = 100^\circ C$	9	14	
Power Dissipation	$P_D$	$T_A = 25^\circ C$	1.5	1.5	W
		$T_A = 70^\circ C$	0.9	0.9	
Operating Junction & Storage Temperature Range	$T_j, T_{stg}$	-55 to 150		$^\circ C$	

<sup>1</sup> 100% UIS testing in condition of  $V_D=25V, L=0.01mH, V_G=10V, I_L=45A, R_G=25\Omega$ , Rated  $V_{DS}=30V$  N-CH\_Q1

<sup>2</sup> 100% UIS testing in condition of  $V_D=25V, L=0.01mH, V_G=10V, I_L=40A, R_G=25\Omega$ , Rated  $V_{DS}=30V$  N-CH\_Q2

**•THERMAL RESISTANCE RATINGS**

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM		UNIT
			Q1	Q2	
Junction-to-Case	$R_{\theta JC}$		5.3	3.5	$^\circ C/W$
Junction-to-Ambient <sup>3</sup>	$R_{\theta JA}$	$t \leq 10s$	44	44	
		Steady-State	86	86	

<sup>1</sup> Pulse width limited by maximum junction temperature.

<sup>2</sup> Duty cycle < 1%

<sup>3</sup> The value of  $R_{\theta JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A = 25^\circ C$ .

<sup>4</sup> Guarantee by Engineering test



▪ Q1\_ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage <sup>4</sup>	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	30			V
Gate Threshold Voltage <sup>4</sup>	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1.2	1.5	2.0	
Gate-Body Leakage <sup>4</sup>	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±12V			±100	nA
Zero Gate Voltage Drain Current <sup>4</sup>	I <sub>DSS</sub>	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V			1	μA
		V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125 °C			25	
On-State Drain Current <sup>1</sup>	I <sub>D(ON)</sub>	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 10V	68			A
Drain-Source On-State Resistance <sup>1,4</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 10A		2.1	2.7	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 7A		3.1	3.7	
Forward Transconductance <sup>1</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 5V, I <sub>D</sub> = 5A		70		S
<b>DYNAMIC</b>						
Input Capacitance <sup>5</sup>	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 15V, f = 1MHz		1570		pF
Output Capacitance <sup>5</sup>	C <sub>oss</sub>			690		
Reverse Transfer Capacitance <sup>5</sup>	C <sub>rss</sub>			55		
Gate Resistance <sup>4,5</sup>	R <sub>g</sub>	f = 1MHz		1.3		Ω
Total Gate Charge <sup>1,2,5</sup>	Q <sub>g</sub> (V <sub>GS</sub> =10V)	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 10A		27		nC
	Q <sub>g</sub> (V <sub>GS</sub> =4.5V)			12		
Gate-Source Charge <sup>1,2,5</sup>	Q <sub>gs</sub>			6.0		
Gate-Drain Charge <sup>1,2,5</sup>	Q <sub>gd</sub>			2.4		
Turn-On Delay Time <sup>1,2,5</sup>	t <sub>d(on)</sub>			8.6		
Rise Time <sup>1,2,5</sup>	t <sub>r</sub>	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 5A, R <sub>g</sub> = 3Ω		17		
Turn-Off Delay Time <sup>1,2,5</sup>	t <sub>d(off)</sub>			25		
Fall Time <sup>1,2,5</sup>	t <sub>f</sub>			6.8		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Continuous Current	I <sub>S</sub>				20	A
Pulsed Current <sup>3</sup>	I <sub>SM</sub>				162	
Forward Voltage <sup>1,4</sup>	V <sub>SD</sub>	I <sub>F</sub> = I <sub>S</sub> , V <sub>GS</sub> = 0V			1.2	V
Reverse Recovery Time <sup>5</sup>	t <sub>rr</sub>	I <sub>F</sub> = I <sub>S</sub> , dI <sub>F</sub> /dt = 100A / μS		17		nS
Peak Reverse Recovery Current <sup>5</sup>	I <sub>RM(REC)</sub>			0.4		A
Reverse Recovery Charge <sup>5</sup>	Q <sub>rr</sub>			3.7		nC

<sup>1</sup>Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

<sup>2</sup>Independent of operating temperature.

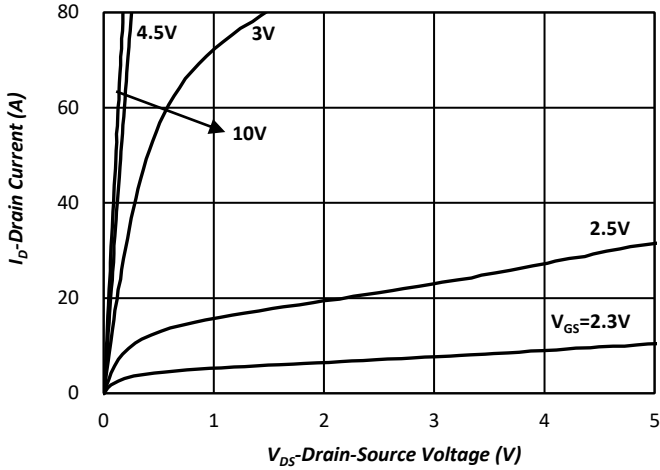
<sup>3</sup>Pulse width limited by maximum junction temperature.

<sup>4</sup>Guarantee by FT test Item

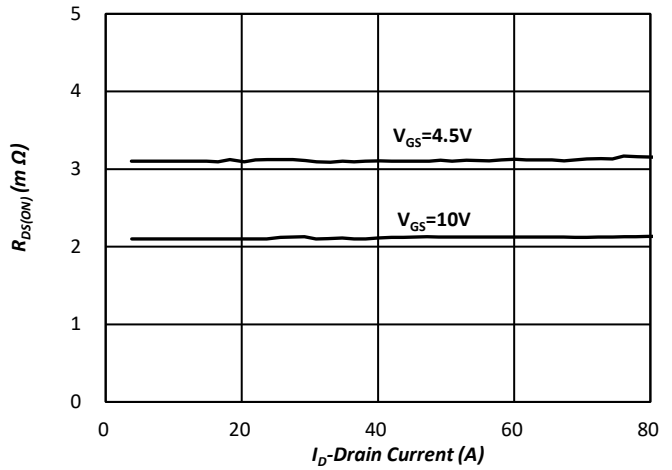
<sup>5</sup>Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

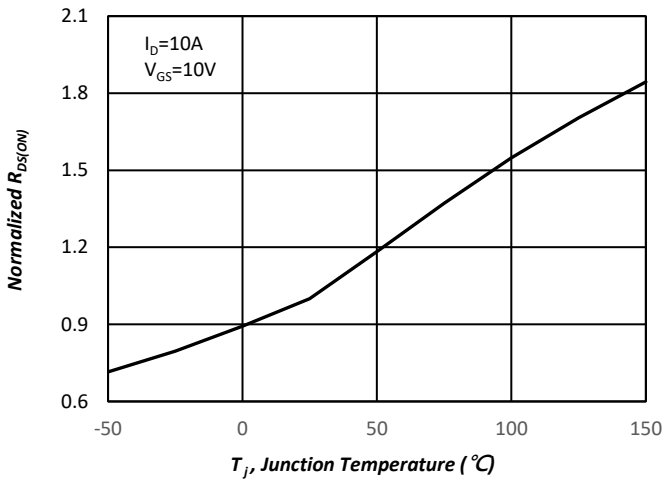
**-Q1\_TYPICAL CHARACTERISTICS**



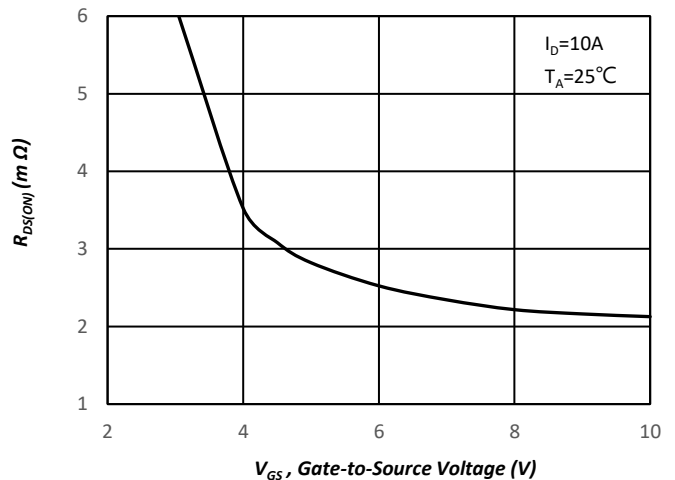
**Fig.1 Typical Output Characteristics**



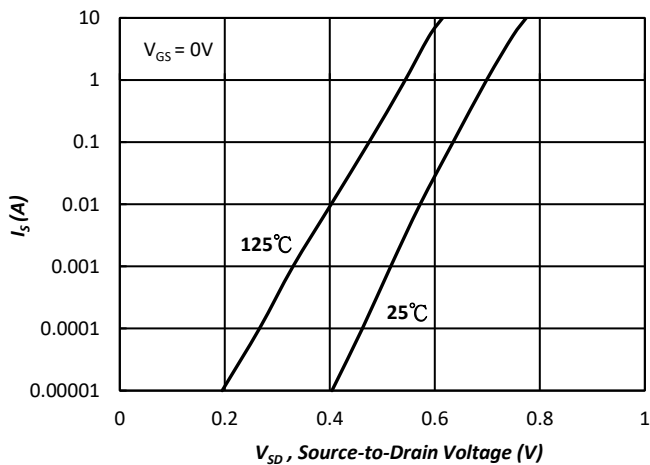
**Fig.2 On-Resistance Variation with Drain Current and Gate Voltage**



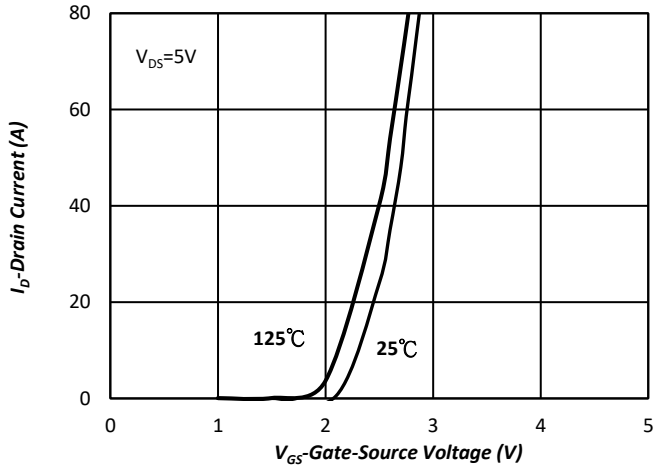
**Fig.3 Normalized On-Resistance v.s. Junction Temperature**



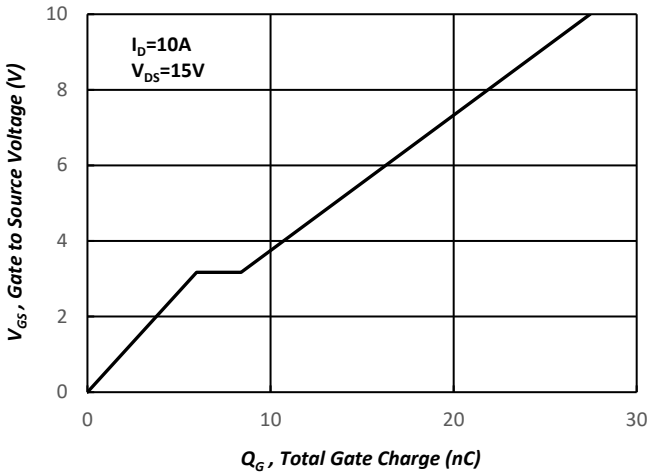
**Fig.4 On-Resistance v.s. Gate Voltage**



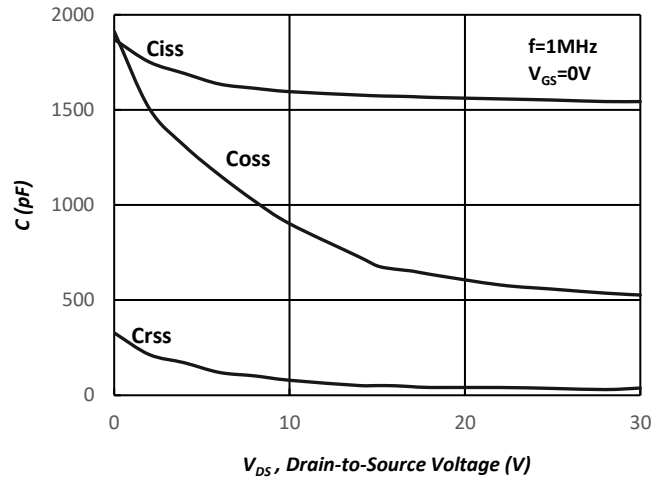
**Fig.5 Forward Characteristic of Reverse Diode**



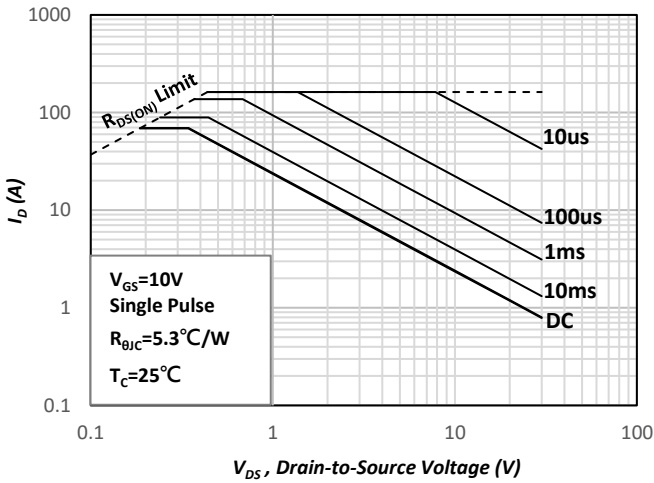
**Fig.6 Transfer Characteristics**



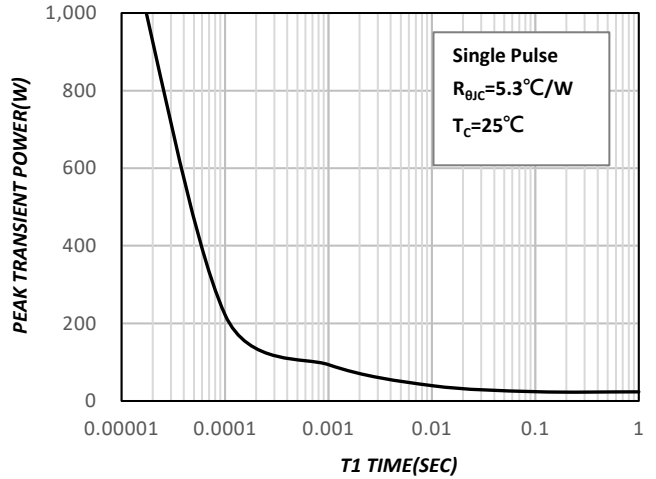
**Fig.7 Gate Charge Characteristics**



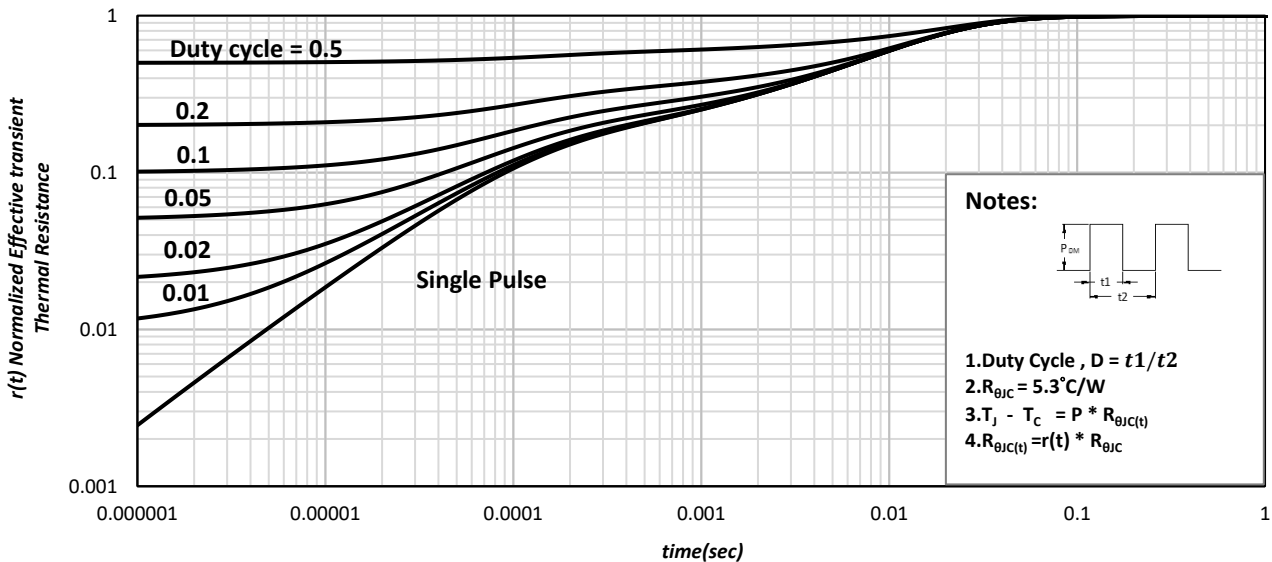
**Fig.8 Typical Capacitance Characteristics**



**Fig.9. Maximum Safe Operating Area**



**Fig.10. Single Pulse Maximum Power Dissipation**



**Fig.11. Effective Transient Thermal Impedance**

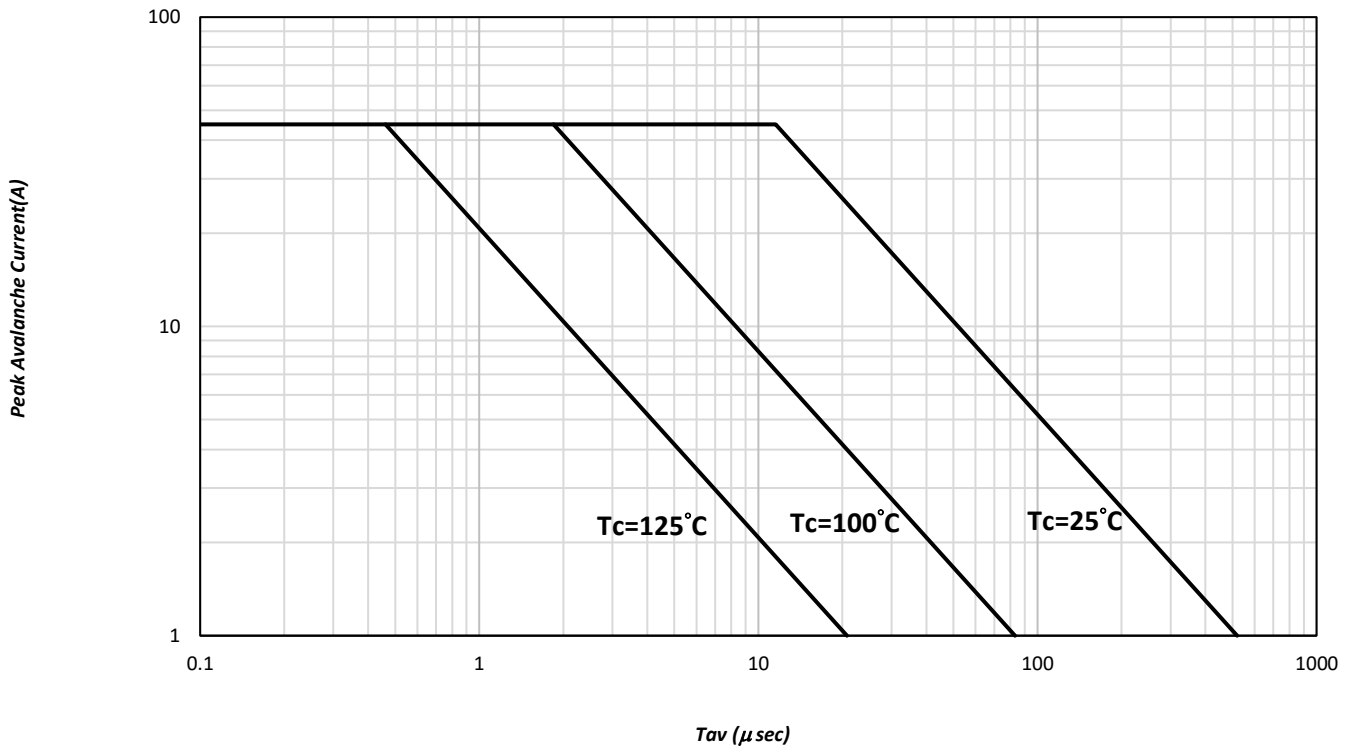


Fig 12. Single Pulse Avalanche Capability Curve

▪ Q2\_ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage <sup>4</sup>	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	30			V
Gate Threshold Voltage <sup>4</sup>	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1.2	1.5	2.0	
Gate-Body Leakage <sup>4</sup>	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±12V			±100	nA
Zero Gate Voltage Drain Current <sup>4</sup>	I <sub>DSS</sub>	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V			1	μA
		V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125 °C			25	
On-State Drain Current <sup>1</sup>	I <sub>D(ON)</sub>	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 10V	91			A
Drain-Source On-State Resistance <sup>1,4</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 10A		2.0	2.4	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 7A		2.9	3.5	
Forward Transconductance <sup>1</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 5V, I <sub>D</sub> = 5A		72		S
<b>DYNAMIC</b>						
Input Capacitance <sup>5</sup>	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 15V, f = 1MHz		1570		pF
Output Capacitance <sup>5</sup>	C <sub>oss</sub>			680		
Reverse Transfer Capacitance <sup>5</sup>	C <sub>rss</sub>			55		
Gate Resistance <sup>4,5</sup>	R <sub>g</sub>	f = 1MHz		1.2		Ω
Total Gate Charge <sup>1,2,5</sup>	Q <sub>g</sub> (V <sub>GS</sub> =10V)	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 10A		28		nC
	Q <sub>g</sub> (V <sub>GS</sub> =4.5V)			12		
Gate-Source Charge <sup>1,2,5</sup>	Q <sub>gs</sub>			5.9		
Gate-Drain Charge <sup>1,2,5</sup>	Q <sub>gd</sub>			2.8		
Turn-On Delay Time <sup>1,2,5</sup>	t <sub>d(on)</sub>		V <sub>DS</sub> = 15V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 5A, R <sub>g</sub> = 3Ω		8.0	
Rise Time <sup>1,2,5</sup>	t <sub>r</sub>			13		
Turn-Off Delay Time <sup>1,2,5</sup>	t <sub>d(off)</sub>			24		
Fall Time <sup>1,2,5</sup>	t <sub>f</sub>			5.8		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Continuous Current	I <sub>S</sub>				30	A
Pulsed Current <sup>3</sup>	I <sub>SM</sub>				244	
Forward Voltage <sup>1,4</sup>	V <sub>SD</sub>	I <sub>F</sub> = I <sub>S</sub> , V <sub>GS</sub> = 0V			1.2	V
Reverse Recovery Time <sup>5</sup>	t <sub>rr</sub>	I <sub>F</sub> = I <sub>S</sub> , dI <sub>F</sub> /dt = 100A / μS		17		nS
Peak Reverse Recovery Current <sup>5</sup>	I <sub>RM(REC)</sub>			0.4		A
Reverse Recovery Charge <sup>5</sup>	Q <sub>rr</sub>			3.5		nC

<sup>1</sup>Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

<sup>2</sup>Independent of operating temperature.

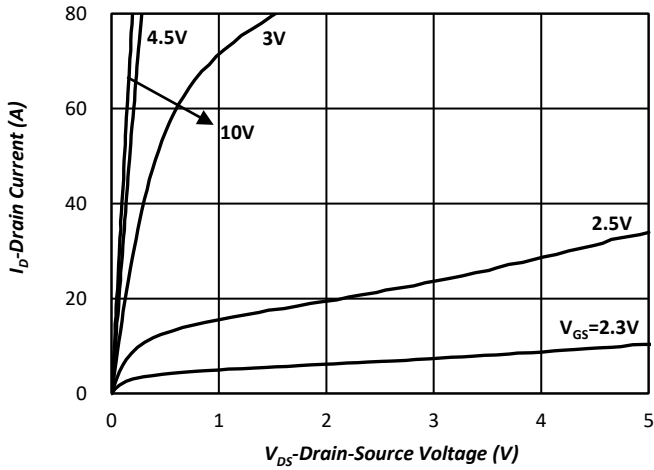
<sup>3</sup>Pulse width limited by maximum junction temperature.

<sup>4</sup>Guarantee by FT test Item

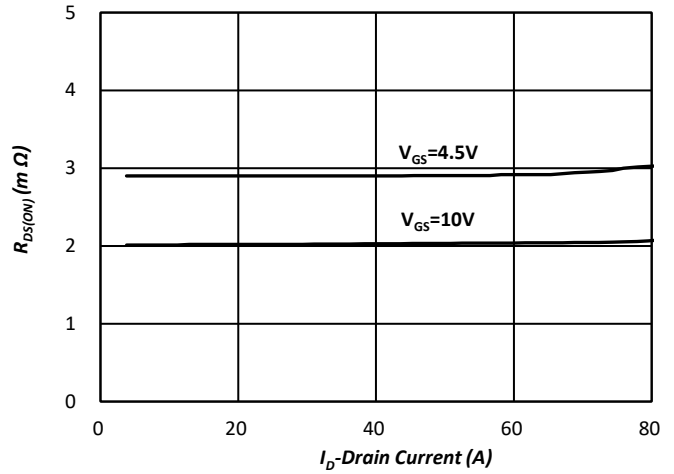
<sup>5</sup>Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

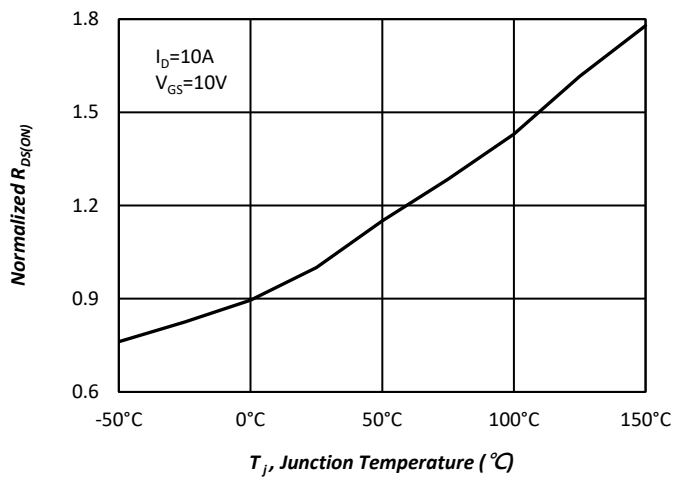
**-Q2\_TYPICAL CHARACTERISTICS**



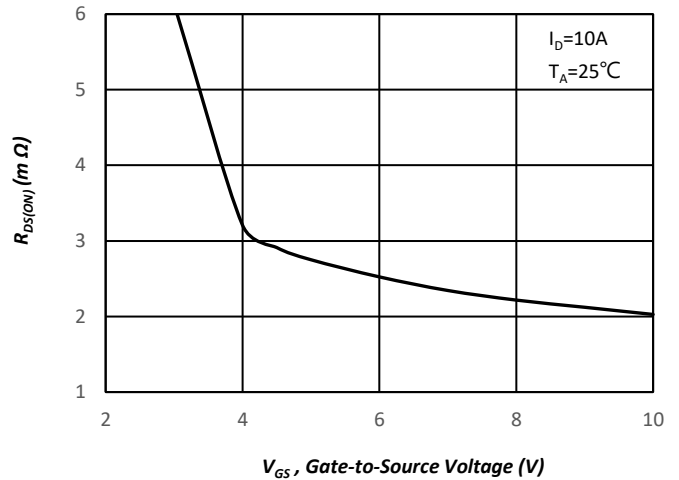
**Fig.1 Typical Output Characteristics**



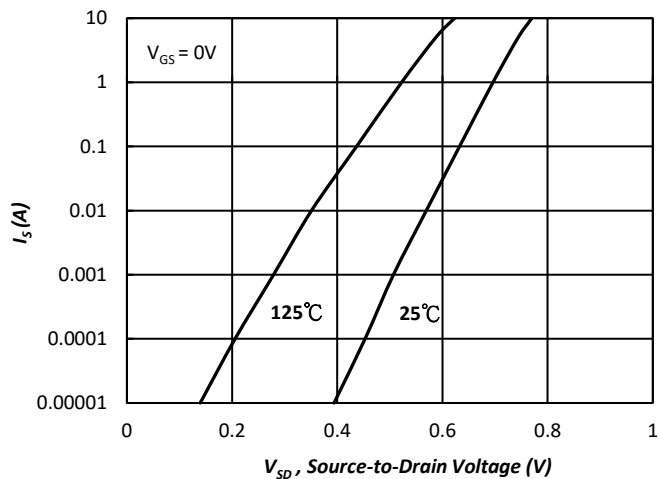
**Fig.2 On-Resistance Variation with Drain Current and Gate Voltage**



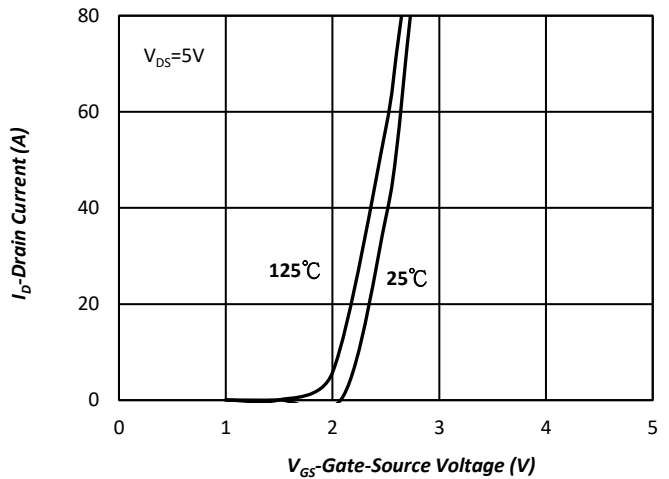
**Fig.3 Normalized On-Resistance v.s. Junction Temperature**



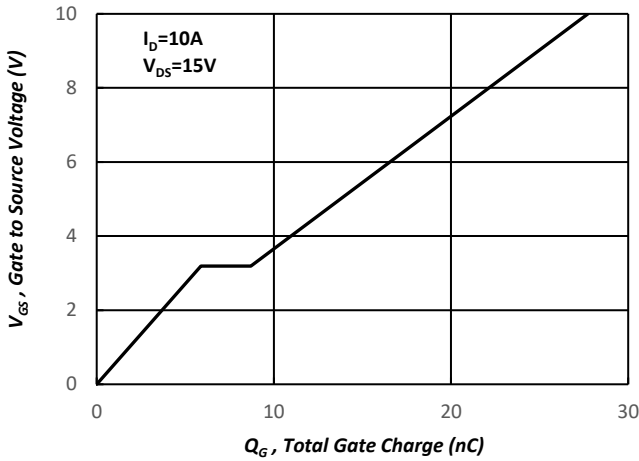
**Fig.4 On-Resistance v.s. Gate Voltage**



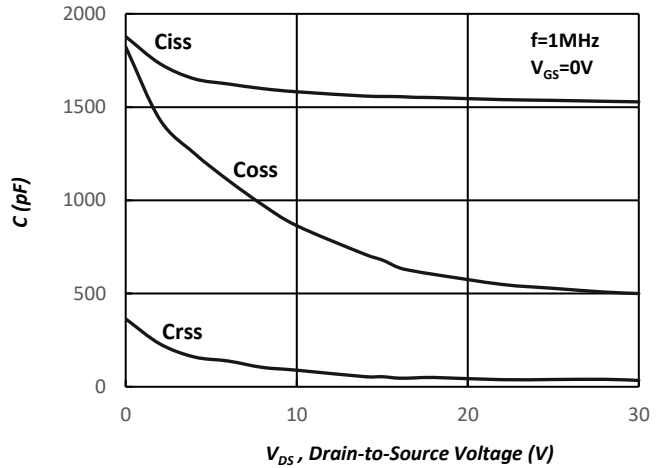
**Fig.5 Forward Characteristic of Reverse Diode**



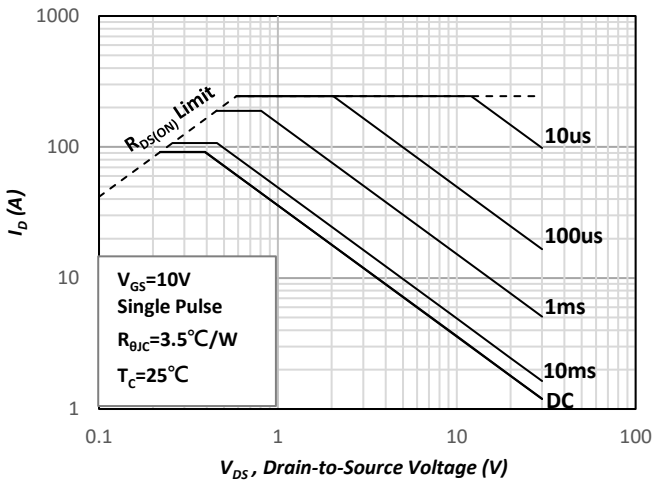
**Fig.6 Transfer Characteristics**



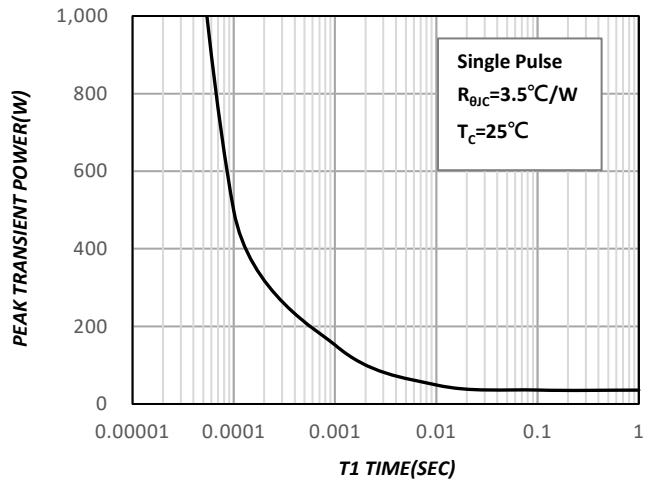
**Fig.7 Gate Charge Characteristics**



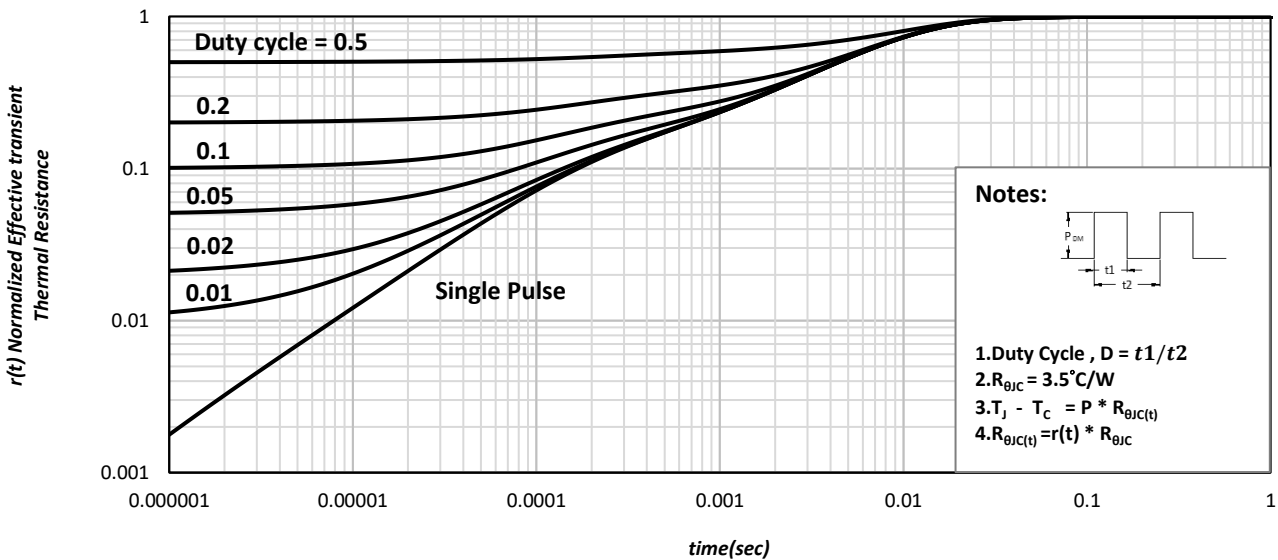
**Fig.8 Typical Capacitance Characteristics**



**Fig.9. Maximum Safe Operating Area**



**Fig.10. Single Pulse Maximum Power Dissipation**



**Fig.11. Effective Transient Thermal Impedance**

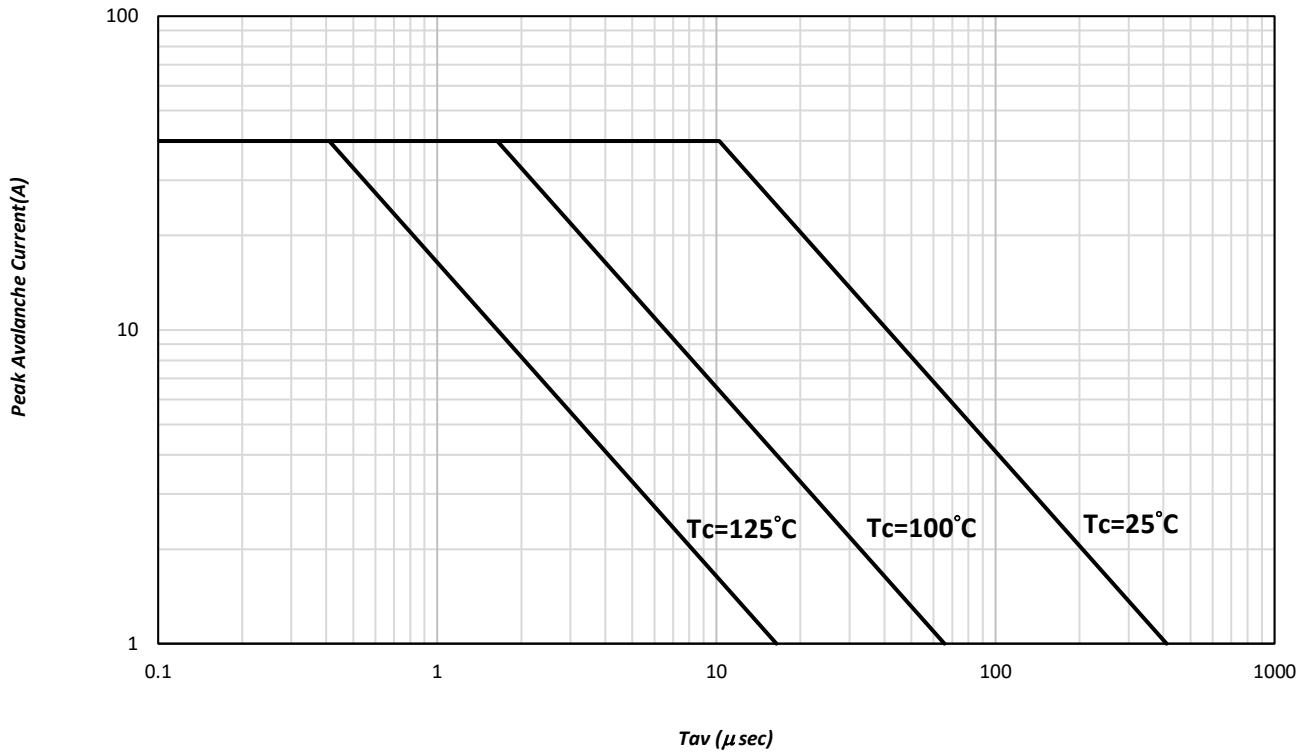
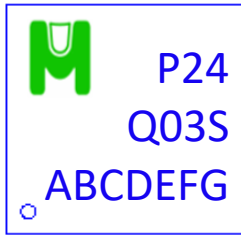


Fig 12. Single Pulse Avalanche Capability Curve

**Ordering & Marking Information:**

**Device Name: EMP24Q03VLCS for DFN3.3X3.3E-08(Dual)**



P24Q03S: Device Name

ABCDEFGH: Date Code

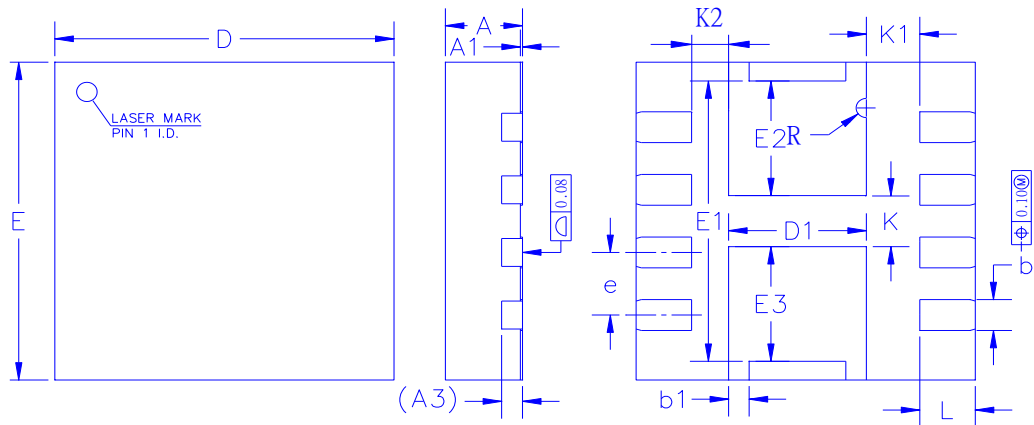
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

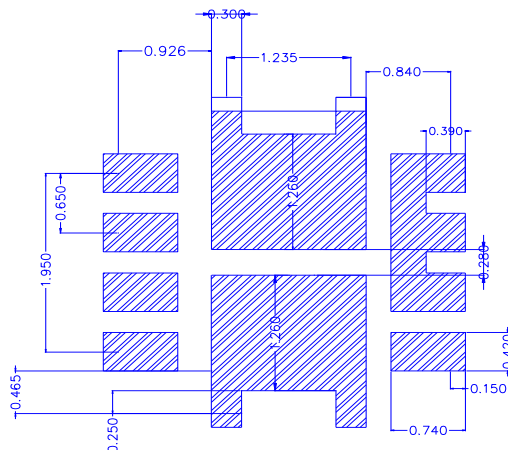
**Outline Drawing**



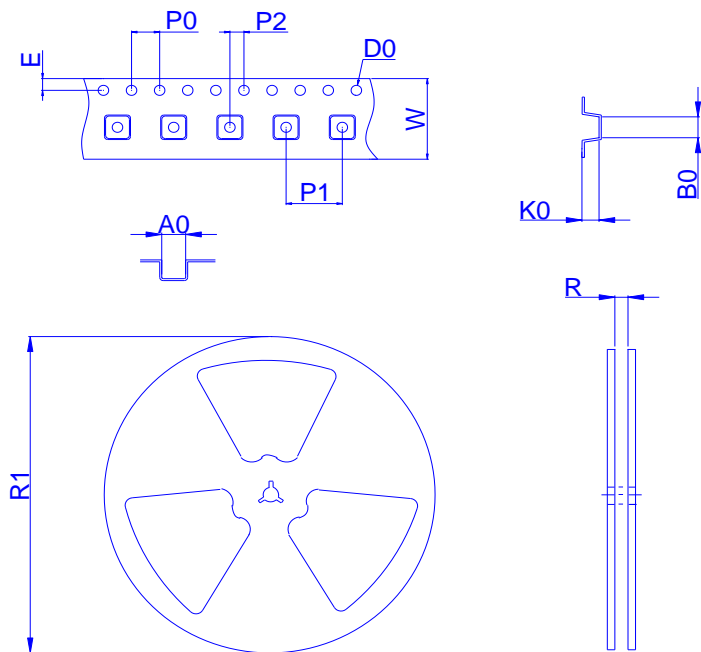
Dimension	A	A1	A3	b	b1	D	E	D1	E1	E2	e	e1
Min.	0.65	-	-	0.27	0.10	3.20	3.20	1.33	1.38	1.09	-	-
Typ.	0.75	-	0.20	0.32	0.20	3.30	3.30	1.43	1.48	1.19	0.65	1.95
Max.	0.85	0.05	-	0.37	0.30	3.40	3.40	1.53	1.58	1.29	-	-

Dimension	K	K1	L	L1
Min.	-	-	-	-
Typ.	0.35	0.44	0.54	0.25
Max.	-	-	-	-

**Footprint**



◆ Tape&Reel Information: 5000pcs/Reel



Package	DFN3.3X3.3E-08(Dual)
Reel	13"
Device orientation	<p>FEED DIRECTION</p> <p>→</p>

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	3.6	3.6	1.55	1.7	1.2	4	8	2	12	12.4	330
±	0.3	0.3	0.2	0.2	0.2	0.1	0.1	0.1	1	2	2