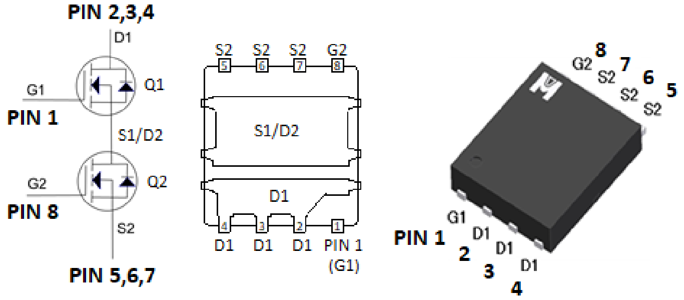
Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH-Q1	N-CH-Q2
BV_{DSS}	30V	30V
$R_{DSON\ (MAX.)}$	5.7mΩ	2.2mΩ
I_D	48A	90A



EDFN5X6-8L

Dual N Channel MOSFET

UIS, Rg 100% Tested

RoHS & Halogen Free & TSCA Compliant

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
			Q1	Q2	
Gate-Source Voltage		V_{GS}	±20	±12	V
Continuous Drain Current	T_C = 25 °C	I_D	48	90	A
	T_A= 25 °C(t≦10s)		18	29	
	T_A= 25 °C(Steady-State)		14	23	
	T_C = 100 °C		30	57	
Pulsed Drain Current[1]		I_{DM}	100	250	
Avalanche Current		I_{AS}	35	60	
Avalanche Energy	L = 0.1mH, R_G=25Ω	E_{AS}	61	180	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	30	90	
Power Dissipation	T_C = 25 °C	P_D	21	40	W
	T_C = 100 °C		8	16	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

100% UIS testing in condition of Q1 V_D=25V, L=0.1mH, V_G=10V, I_L=21A, Rated V_{DS}=30V N-CH

100% UIS testing in condition of Q2 V_D=25V, L=0.1mH, V_G=10V, I_L=36A, Rated V_{DS}=30V N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL		TYPICAL	MAXIMUM		UNIT
Junction-to-Case	$R_{\theta JC}$	Steady State		5.8	3.1	°C / W
Junction-to-Ambient	$R_{\theta JA}$	Steady State		65	65	
	$R_{\theta JA}$	t ≦ 10 s		40	40	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle < 1%

[3]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C.

[4]Guarantee by Engineering test.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	Q1	30			V
			Q2	30			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	Q1	1	1.5	3	
			Q2	1	1.5	3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	Q1			±100	nA
		V_{DS} = 0V, V_{GS} = ±12V	Q2			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24V, V_{GS} = 0V	Q1			1	μA
			Q2			1	
		V_{DS} = 20V, V_{GS} = 0V, T_J = 125 °C	Q1			25	
			Q2			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	Q1	48			A
			Q2	90			
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 20A	Q1		5.0	5.7	mΩ
		V_{GS} = 10V, I_D = 20A	Q2		1.8	2.2	
		V_{GS} = 4.5V, I_D = 20A	Q1		7.0	8.8	
		V_{GS} = 4.5V, I_D = 20A	Q2		2.6	3.4	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 20A	Q1		48		S
		V_{DS} = 5V, I_D = 20A	Q2		72		
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz	Q1		1327		pF
			Q2		3770		
Output Capacitance	C_{oss}		Q1		430		
			Q2		1122		
Reverse Transfer Capacitance	C_{rss}		Q1		37		
			Q2		82		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz	Q1		1.1		Ω
			Q2		1.3		
Total Gate Charge[1,2]	$Q_g(V_{GS}$=10V)	V_{DD} = 15V, V_{GS} = 10V, I_D = 20A	Q1		22		
			Q2		56		
	$Q_g(V_{GS}$=4.5V)		Q1		11		
			Q2		26		

Gate-Source Charge[1,2]	Q_{gs}	V_{DD} = 15V, V_{GS} = 10V, I_D = 20A	Q1		3		nC
			Q2		7.1		
Gate-Drain Charge[1,2]	Q_{gd}		Q1		4.3		
			Q2		8.8		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DD} = 15V, I_D = 5A, V_{GS} = 10V, R_G = 3Ω	Q1		6.3		nS
			Q2		11.3		
Rise Time[1,2]	t_r		Q1		11.3		
			Q2		17.7		
Turn-Off Delay Time[1,2]	$t_{d(off)}$		Q1		40		
			Q2		105.3		
Fall Time[1,2]	t_f		Q1		16.2		
			Q2		41.4		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)							
Continuous Current	I_S		Q1			20	A
			Q2			30	
Pulsed Current[3]	I_{SM}		Q1			80	
			Q2			120	
Forward Voltage[1]	V_{SD}	I_F = 10A, V_{GS} = 0V	Q1			1.2	V
			Q2			1.2	
Reverse Recovery Time	t_{rr}	Q1 I_F = 20A, dI_F/dt = 100A / µS	Q1		30		nS
			Q2		35		
Reverse Recovery Charge	Q_{rr}	Q2 I_F = 20A, dI_F/dt = 100A / µS	Q1		18		nC
			Q2		25		

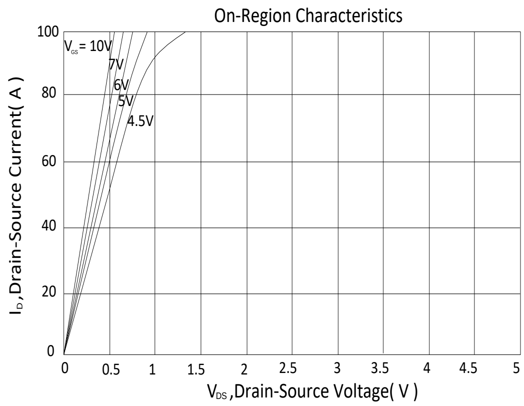
[1]Pulse test : Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

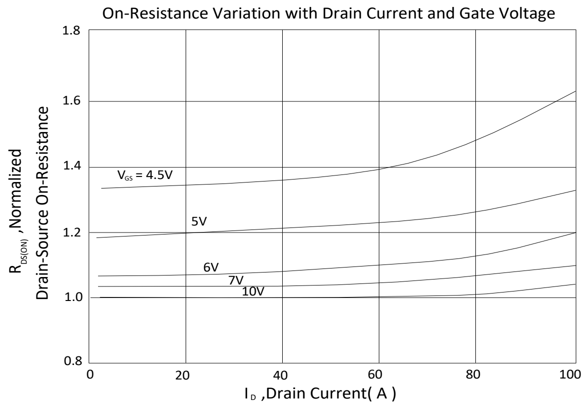
[2]Independent of operating temperature.

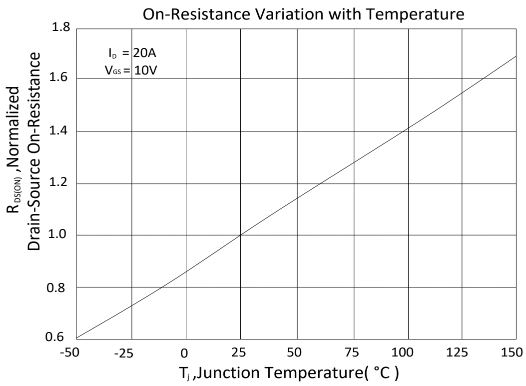
[3]Pulse width limited by maximum junction temperature.

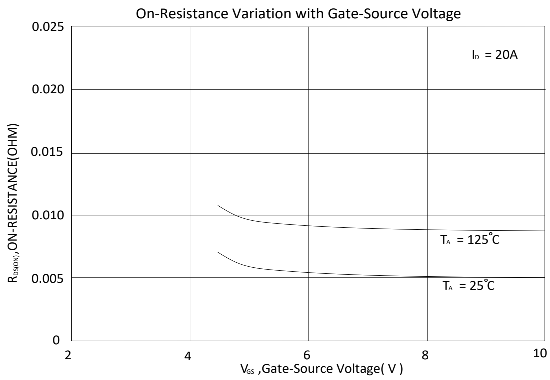
EMC will review datasheet by quarter, and update new version.

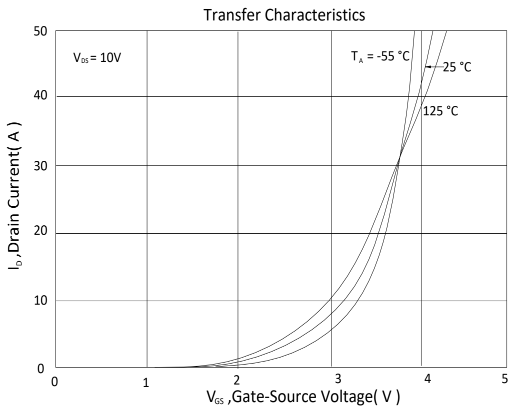
Q1 TYPICAL CHARACTERISTICS

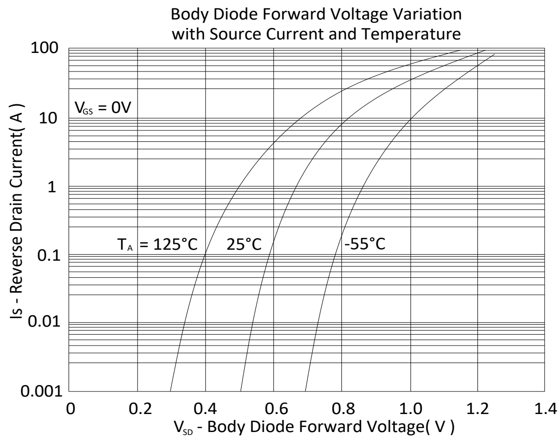


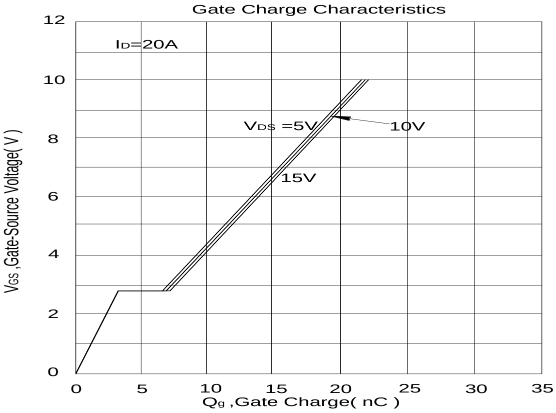


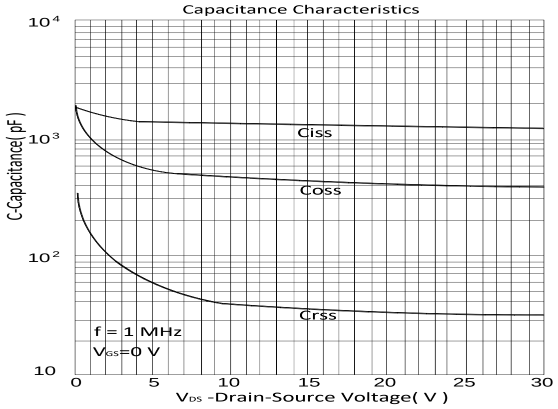


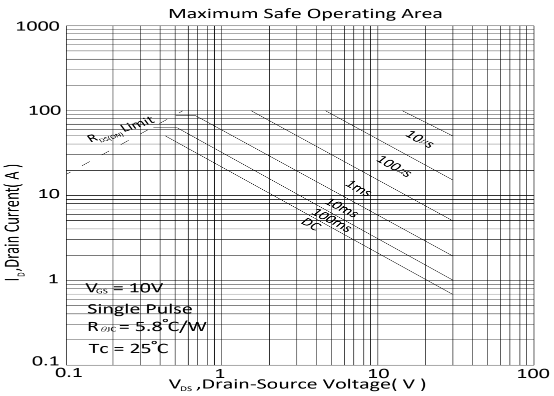


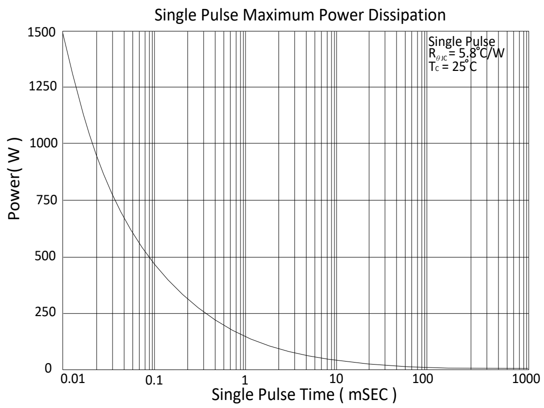


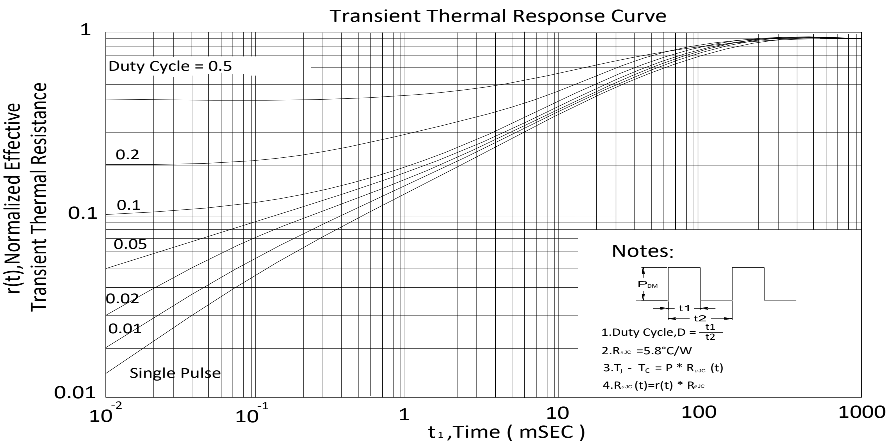



Gate Charge Characteristics
ID=20A
VDS =5V
10V
15V
VGS ,Gate-Source Voltage(V)
Qg ,Gate Charge(nC)
0
2
4
6
8
10
12
0
5
10
15
20
25
30
35

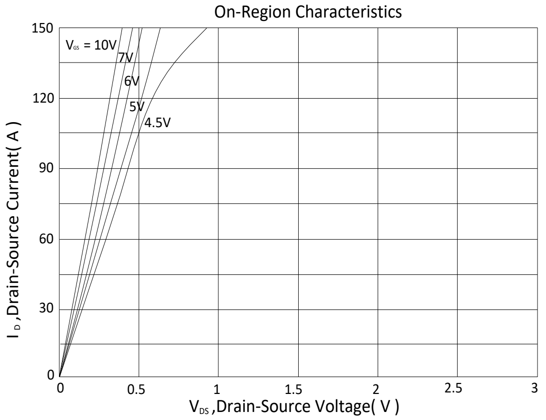

Capacitance Characteristics
Ciss
Coss
Crss
f = 1 MHz
VGS=0 V
C-Capacitance(pF)
VDS -Drain-Source Voltage(V)
10
10²
10³
10⁴
0
5
10
15
20
25
30

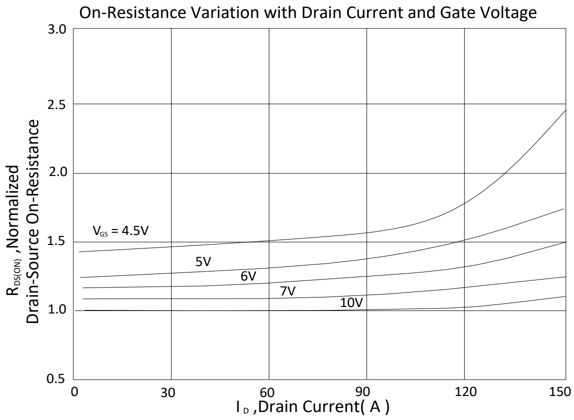

Maximum Safe Operating Area
RDS(ON) Limit
10µs
100µs
1ms
10ms
100ms
DC
VGS = 10V
Single Pulse
RθJC = 5.8°C/W
Tc = 25°C
ID,Drain Current(A)
VDS ,Drain-Source Voltage(V)
0.1
1
10
100
1000

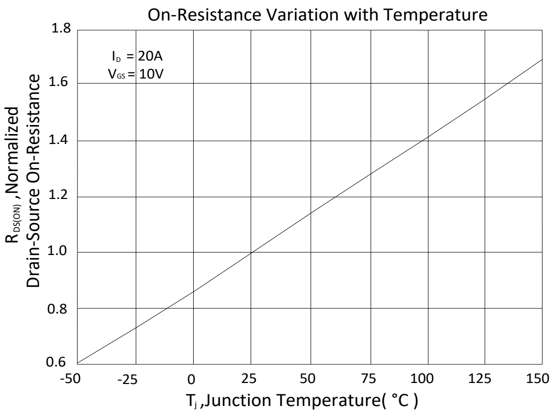

Single Pulse Maximum Power Dissipation
Single Pulse
RθJC = 5.8°C/W
Tc = 25°C
Power(W)
Single Pulse Time (mSEC)
0
250
500
750
1000
1250
1500
0.01
0.1
1
10
100
1000

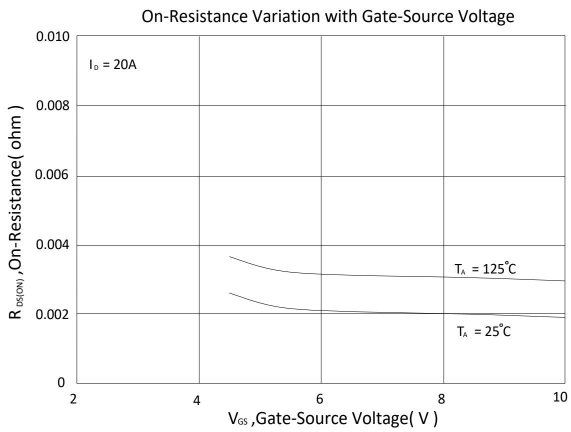

Transient Thermal Response Curve
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Notes:
PDM
t1
t2
1.Duty Cycle,D = t1/t2
2.RθJC =5.8°C/W
3.TJ - TC = P * RθJC (t)
4.RθJC (t)=r(t) * RθJC
r(t),Normalized Effective Transient Thermal Resistance
t1,Time (mSEC)
0.01
0.1
1
10⁻²
10⁻¹
1
10
100
1000

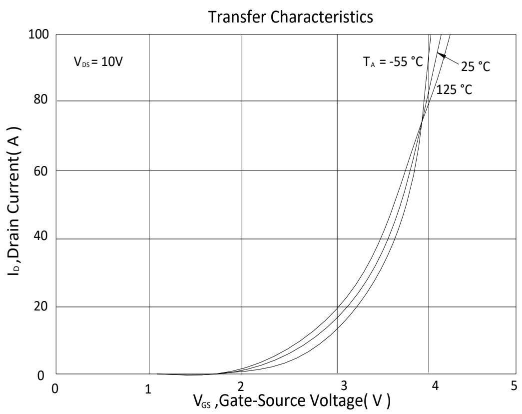
Q2 TYPICAL CHARACTERISTICS

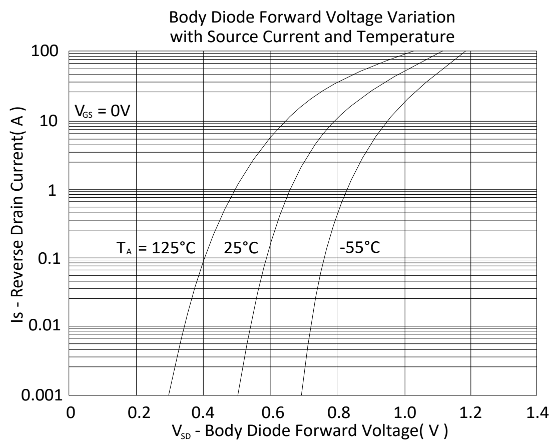


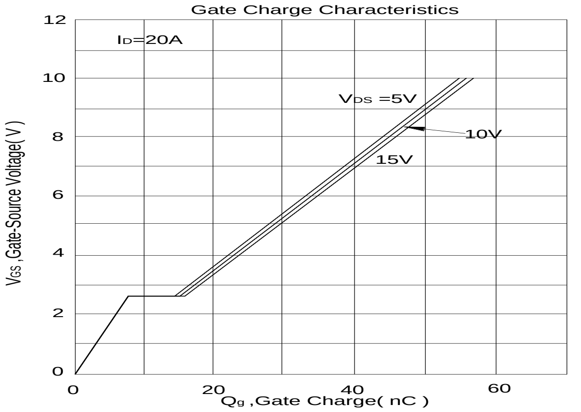


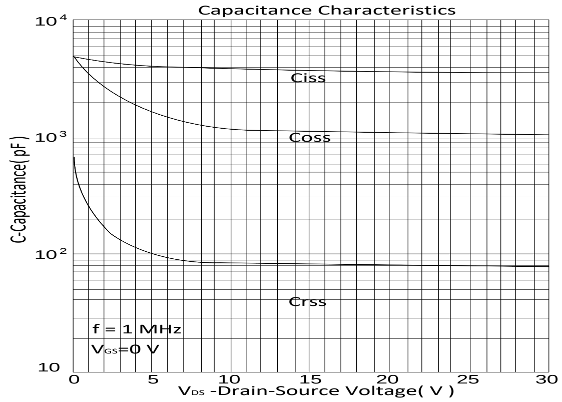


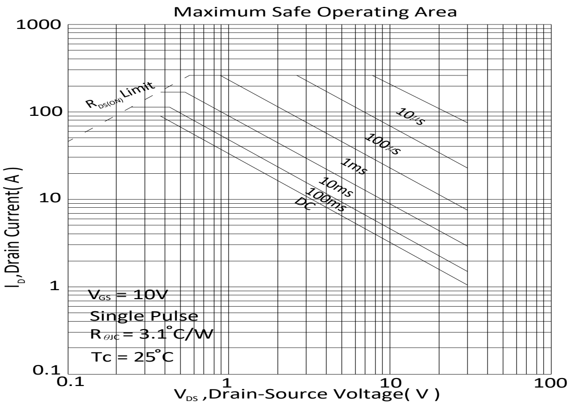


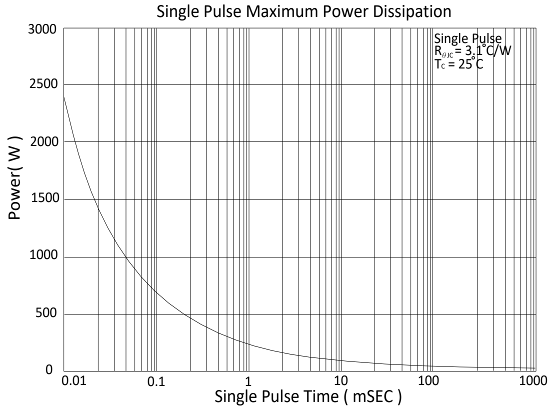


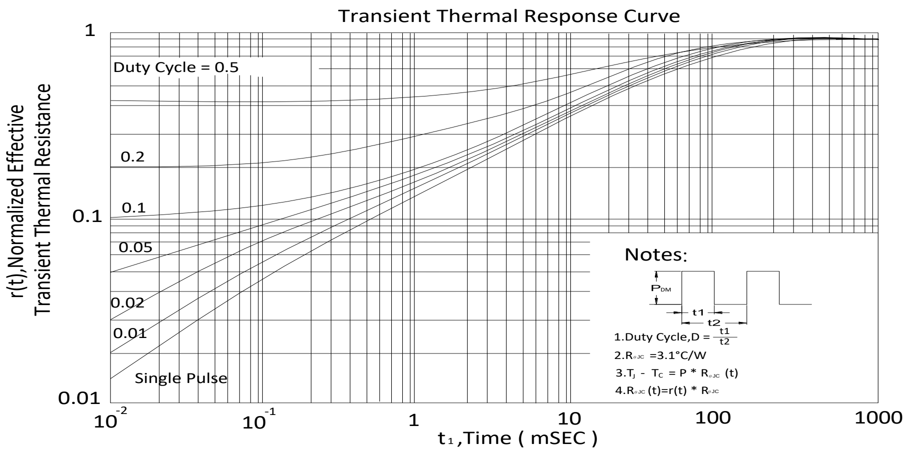



Gate Charge Characteristics
ID=20A
VDS =5V
10V
15V
VGS ,Gate-Source Voltage(V)
Qg ,Gate Charge(nC)
0
2
4
6
8
10
12
0
20
40
60


Capacitance Characteristics
Ciss
Coss
Crss
f = 1 MHz
VGS=0 V
C-Capacitance(pF)
VDS -Drain-Source Voltage(V)
10
10²
10³
10⁴
0
5
10
15
20
25
30


Maximum Safe Operating Area
RDS(ON) Limit
10us
100us
1ms
10ms
100ms
DC
VGS = 10V
Single Pulse
RθJC = 3.1°C/W
Tc = 25°C
ID,Drain Current(A)
VDS ,Drain-Source Voltage(V)
0.1
1
10
100
1000
0.1
1
10
100


Single Pulse Maximum Power Dissipation
Single Pulse
RθJC = 3.1°C/W
TC = 25°C
Power(W)
Single Pulse Time (mSEC)
0
500
1000
1500
2000
2500
3000
0.01
0.1
1
10
100
1000


Transient Thermal Response Curve
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Notes:
PDM
t1
t2
1.Duty Cycle,D = t1/t2
2.RθJC =3.1°C/W
3.TJ - TC = P * RθJC (t)
4.RθJC (t)=r(t) * RθJC
r(t),Normalized Effective
Transient Thermal Resistance
t1 ,Time (mSEC)
0.01
0.1
1
10⁻²
10⁻¹
1
10
100
1000

Ordering & Marking Information

Device Name: EMP19K03HPCS for Asymmetric Dual EDFN5X6

EMP19K03HPCS: Device Name

ABCDEFG: Date Code

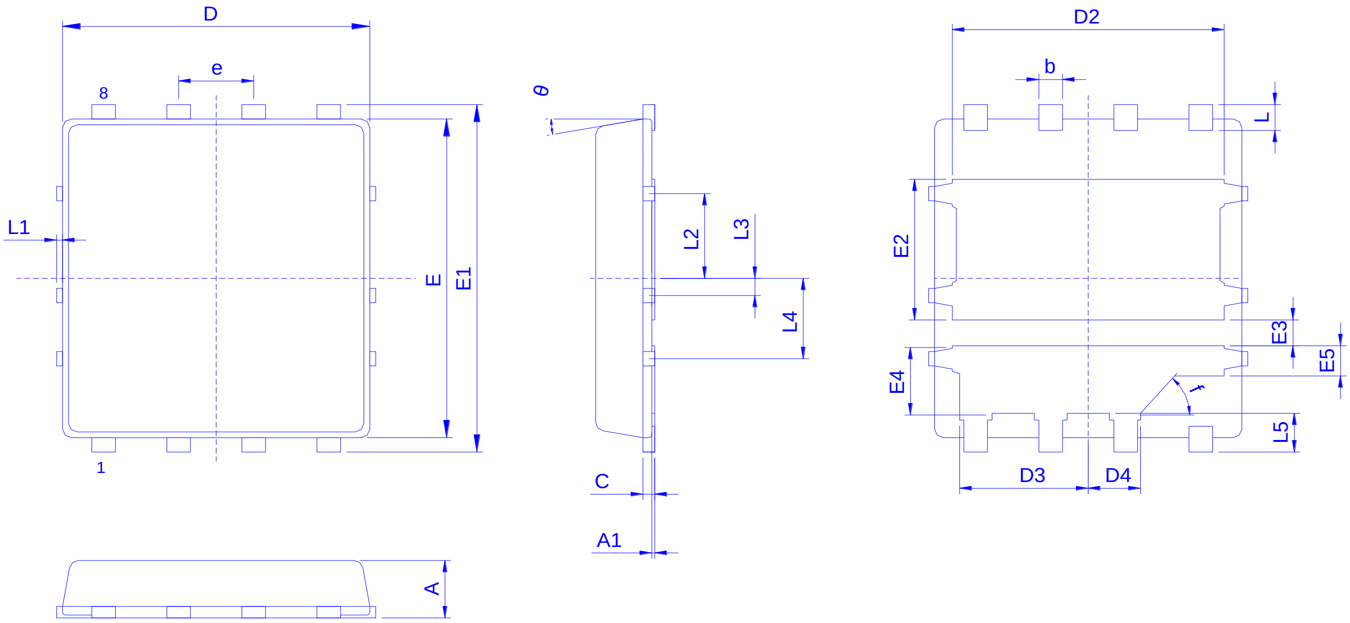
A: Assembly House

B: Year(A:2008 B:2009 C:2010….)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

Outline Drawing

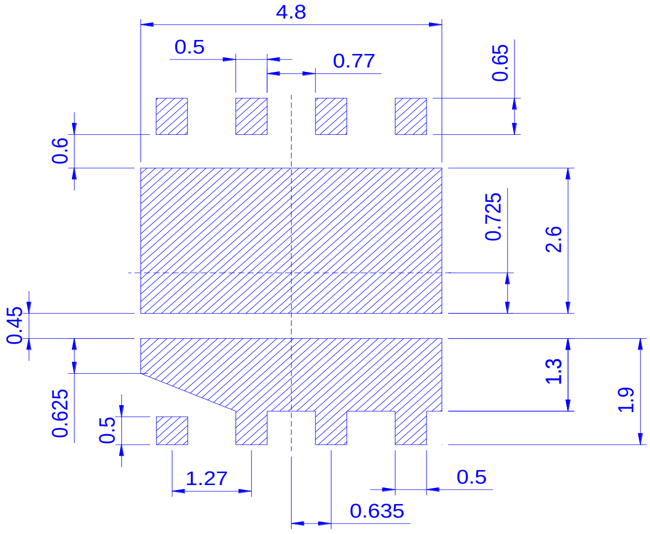


Dimension in mm

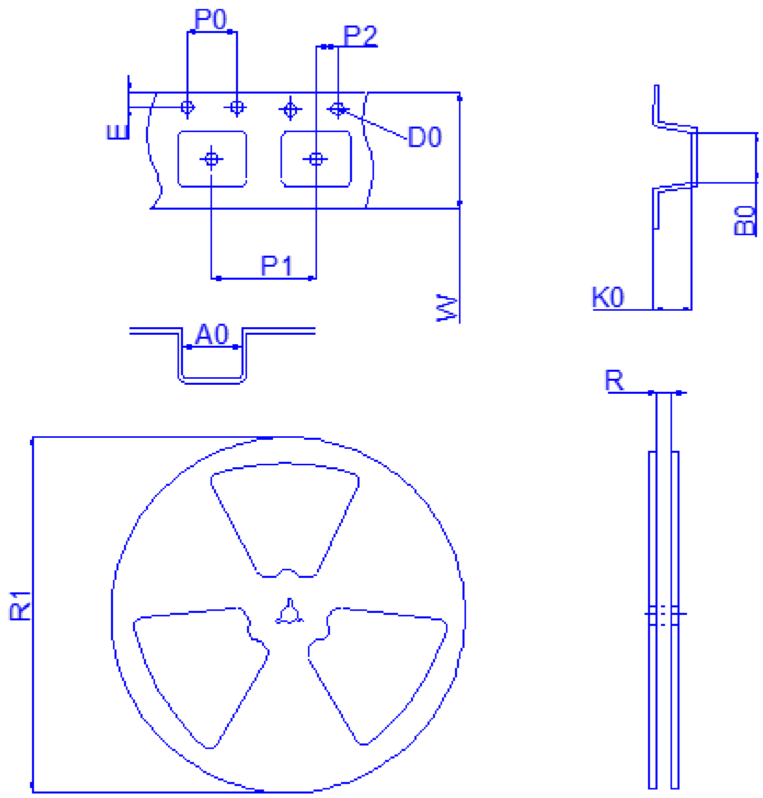
Dimension	A	A1	b	c	D	D2	D3	D4	E	E1	E2	E3	E4	E5
Min.	0.85	0.00	0.35	0.15		4.5	2.125	0.835			2.4	0.40	1.125	0.475
Typ.	0.90		0.40	0.20	5.2	4.6	2.175	0.885	5.55	6.05	2.45	0.45	1.175	0.525
Max.	1.00	0.05	0.45	0.25		4.7	2.225	0.935			2.5	0.50	1.225	0.575

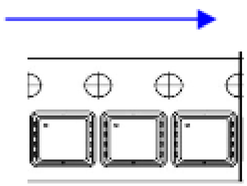
Dimension	e	L	L1	L2	L3	L4	L5	F	θ
Min.		0.35	0	1.375	0.2	1.3	0.575		0°
Typ.	1.27	0.45		1.475	0.3	1.4	0.675	45°	
Max.		0.55	0.1	1.575	0.4	1.5	0.775		10°

Recommended minimum pads



◆ **Tape&Reel Information**:2500pcs/Reel(Dimension in millimeter)



Package	EDFN5X6
Reel	13”
Device orientation	FEED DIRECTION 

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	6.4	5.3	1.5	1.8	1.6	4.0	8.0	2.0	12.0	12.4	330.0
±	0.2	0.2	0.1	0.1	0.6	0.1	0.1	0.1	0.3	2.0	2.0