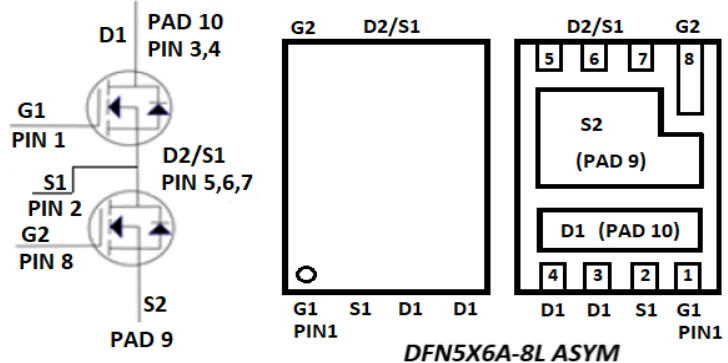


Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

•Product Summary:

	Q1	Q2
BV_{DSS}	30V	30V
$R_{DS(on) (MAX.)}@V_{GS}=10V$	5m Ω	1.4m Ω
$R_{DS(on) (MAX.)}@V_{GS}=4.5V$	8m Ω	1.8m Ω
$I_D @T_C=25^\circ C$	59A	124A
$I_D @T_A=25^\circ C$	14A	27A

• Pin Description:



Dual N Channel MOSFET

UIS, Rg 100% Tested

RoHS & Halogen Free & TSCA Compliant

•ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ C$ Unless Otherwise Noted)



PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS		UNIT	
		Q1	Q2		
Gate-Source Voltage	V_{GS}	20/-16	± 12	V	
Continuous Drain Current	I_D	$T_C = 25^\circ C$	59	124	A
		$T_C = 100^\circ C$	37	78	
Continuous Drain Current	I_D	$T_A = 25^\circ C$	14	27	
		$T_A = 70^\circ C$	11	22	
Pulsed Drain Current ¹	I_{DM}	165	360		
Avalanche Current	I_{AS}	70	110		
Avalanche Energy	L = 0.01mH	EAS	24.5	60.5	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	EAR	122.5	302.5	
Power Dissipation	P_D	$T_C = 25^\circ C$	29	37	W
		$T_C = 100^\circ C$	12	15	
Power Dissipation	P_D	$T_A = 25^\circ C$	1.8	1.8	W
		$T_A = 70^\circ C$	1.2	1.2	
Operating Junction & Storage Temperature Range	T_{jv}, T_{stg}	-55 to 150		$^\circ C$	

• 100% UIS testing in condition of $V_D=25V, L=0.01mH, V_G=10V, I_L=45A, R_G=25\Omega$, Rated $V_{DS}=30V$ N-CH_Q1

• 100% UIS testing in condition of $V_D=25V, L=0.01mH, V_G=10V, I_L=66A, R_G=25\Omega$, Rated $V_{DS}=30V$ N-CH_Q2

•THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM		UNIT
			Q1	Q2	
Junction-to-Case	$R_{\theta JC}$		4.3	3.4	$^\circ C/W$
Junction-to-Ambient ³	$t \leq 10s$	$R_{\theta JA}$	37	37	
	Steady-State	$R_{\theta JA}$	68	68	

¹Pulse width limited by maximum junction temperature.

²Duty cycle < 1%

³The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ C$.

⁴Guarantee by Engineering test



▪ Q1_ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	30			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.2	1.6	2.2	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = +20V/-16V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 30V, V _{GS} = 0V			1	μA
		V _{DS} = 30V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	59			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A		3.9	5	mΩ
		V _{GS} = 4.5V, I _D = 20A		6.3	8	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 5A		38		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		900		pF
Output Capacitance ⁵	C _{oss}			300		
Reverse Transfer Capacitance ⁵	C _{rss}			50		
Gate Resistance ^{4,5}	R _g	f = 1MHz		0.8		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 15V, V _{GS} = 10V, I _D = 20A		17		nC
	Q _g (V _{GS} =4.5V)			8.0		
Gate-Source Charge ^{1,2,5}	Q _{gs}			3.5		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			2.0		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 15V, V _{GS} = 10V, I _D = 5A, R _g = 3Ω		7.0		nS
Avalanche Energy	t _r			13		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			16		
Fall Time ^{1,2,5}	t _f			2.7		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				24	A
Pulsed Current ³	I _{SM}				165	
Forward Voltage ^{1,4}	V _{SD}	I _F = 20A, V _{GS} = 0V			1.2	V
Reverse Recovery Time ⁵	t _{rr}	I _F = 20A, di/dt = 400A / μS		10		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			1.8		A
Reverse Recovery Charge ⁵	Q _{rr}			10		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

-Q1_TYPICAL CHARACTERISTICS

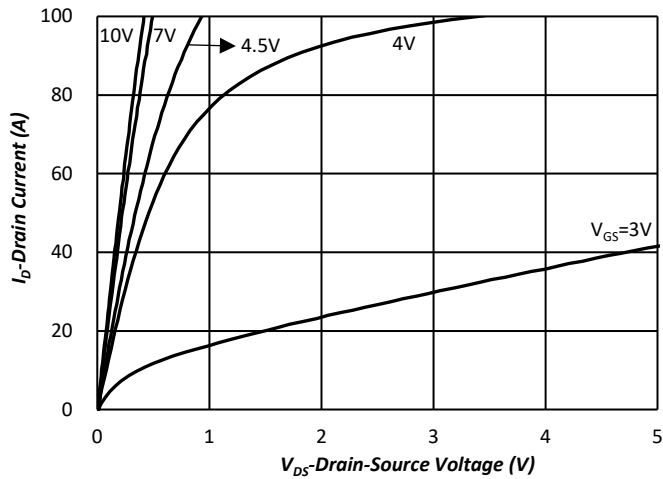


Fig.1 Typical Output Characteristics

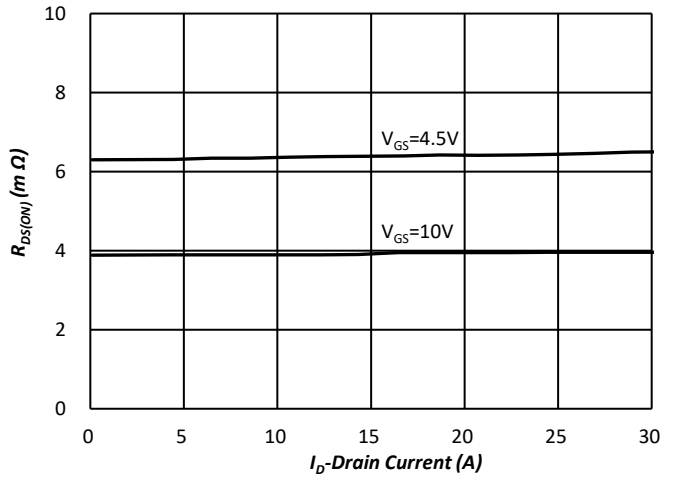


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

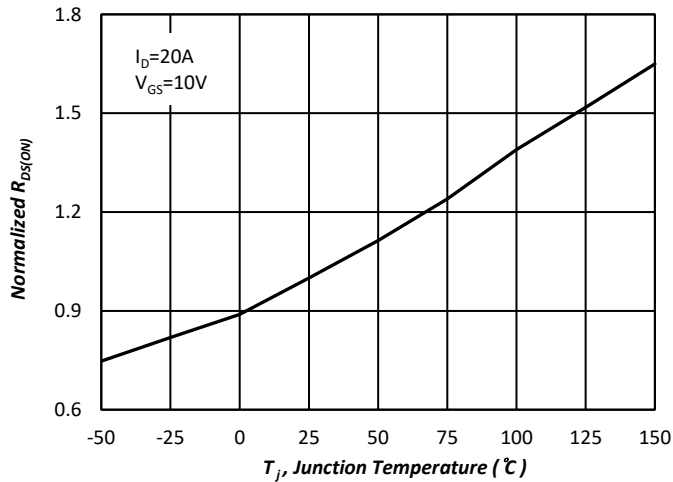


Fig.3 Normalized On-Resistance v.s. Junction Temperature

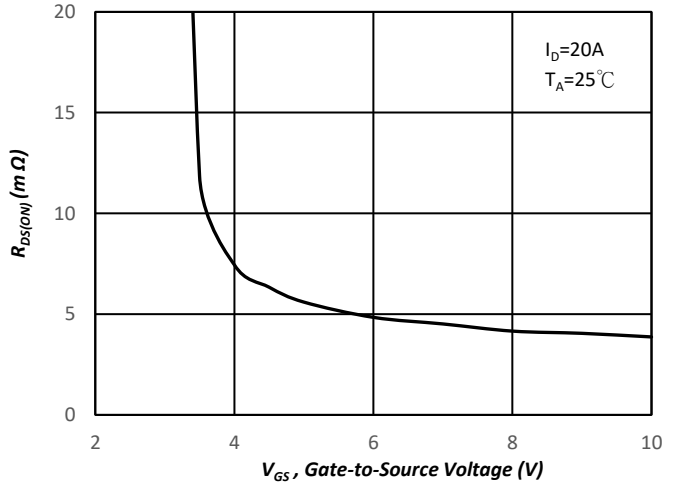


Fig.4 On-Resistance v.s. Gate Voltage

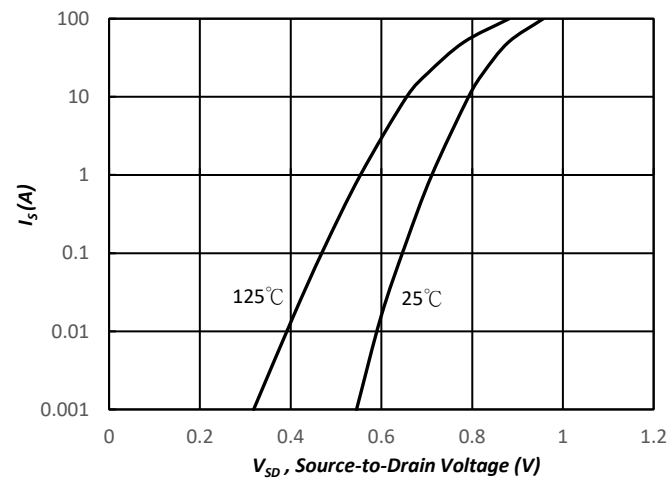


Fig.5 Forward Characteristic of Reverse Diode

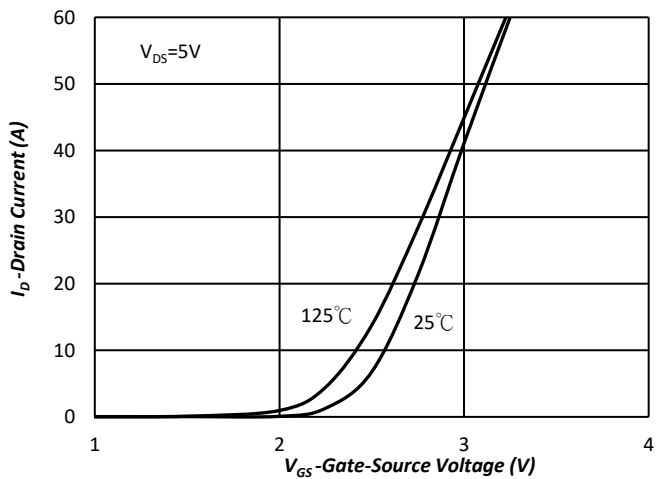


Fig.6 Transfer Characteristics

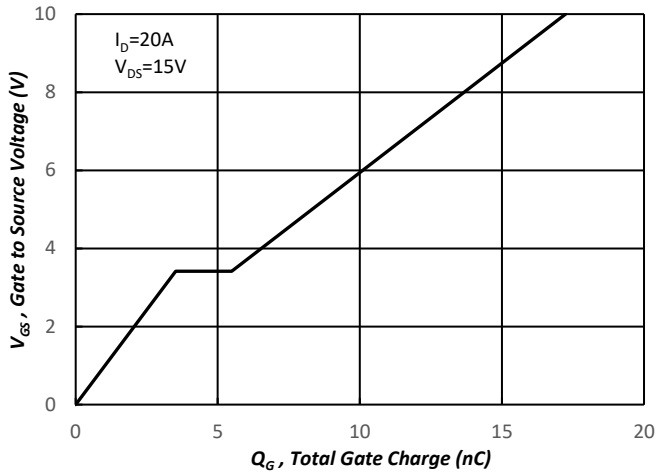


Fig.7 Gate Charge Characteristics

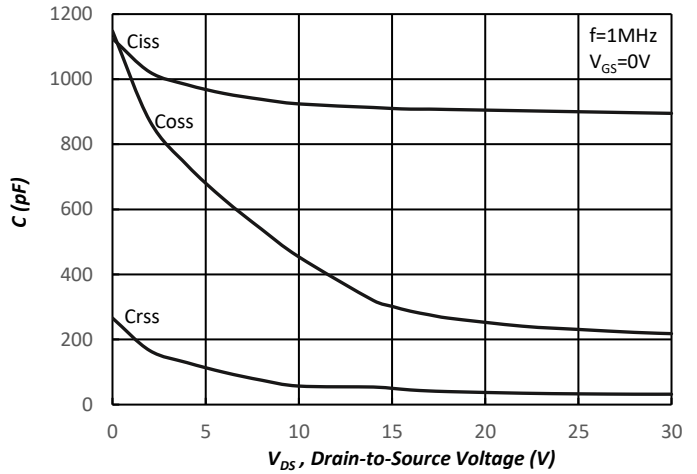


Fig.8 Typical Capacitance Characteristics

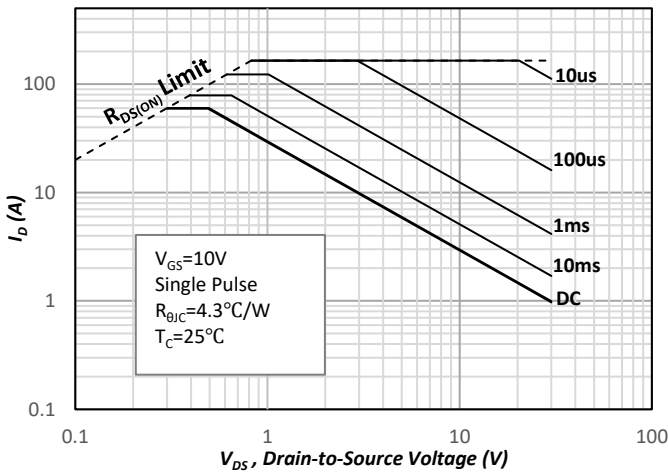


Fig.9. Maximum Safe Operating Area

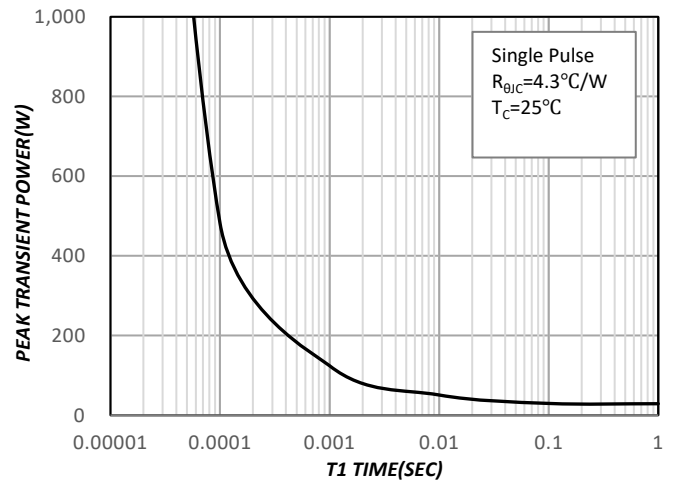


Fig.10. Single Pulse Maximum Power Dissipation

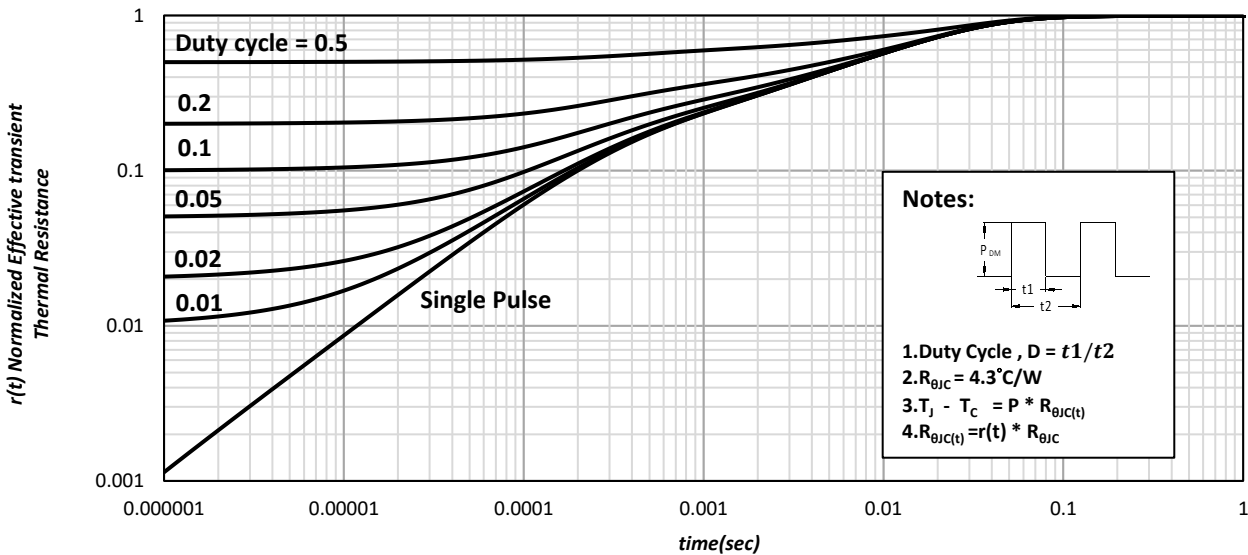


Fig.11. Effective Transient Thermal Impedance



▪ Q2_ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	30			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.2	1.5	2.2	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 30V, V _{GS} = 0V			1	μA
		V _{DS} = 30V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	124			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A		1.0	1.4	mΩ
		V _{GS} = 4.5V, I _D = 20A		1.4	1.8	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 5A		120		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		3650		pF
Output Capacitance ⁵	C _{oss}			1150		
Reverse Transfer Capacitance ⁵	C _{rss}			60		
Gate Resistance ^{4,5}	R _g	f = 1MHz		0.7		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 15V, V _{GS} = 10V, I _D = 20A		60		nC
	Q _g (V _{GS} =4.5V)			27		
Gate-Source Charge ^{1,2,5}	Q _{gs}			12		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			5.0		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 15V, V _{GS} = 10V, I _D = 5A, R _g = 3Ω		11		nS
Avalanche Energy	t _r			15		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			41		
Fall Time ^{1,2,5}	t _f			12		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				31	A
Pulsed Current ³	I _{SM}				360	
Forward Voltage ^{1,4}	V _{SD}	I _F = 20A, V _{GS} = 0V			1.2	V
Reverse Recovery Time ⁵	t _{rr}	I _F = 20A, di/dt = 400A / μS		33		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			3.7		A
Reverse Recovery Charge ⁵	Q _{rr}			66		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

-Q2_TYPICAL CHARACTERISTICS

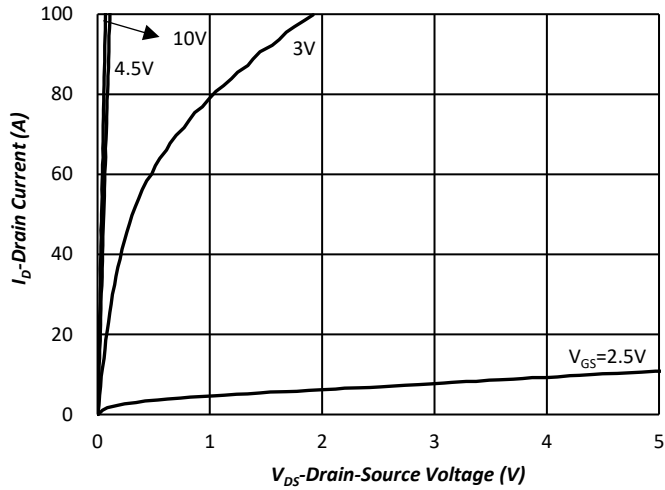


Fig.1 Typical Output Characteristics

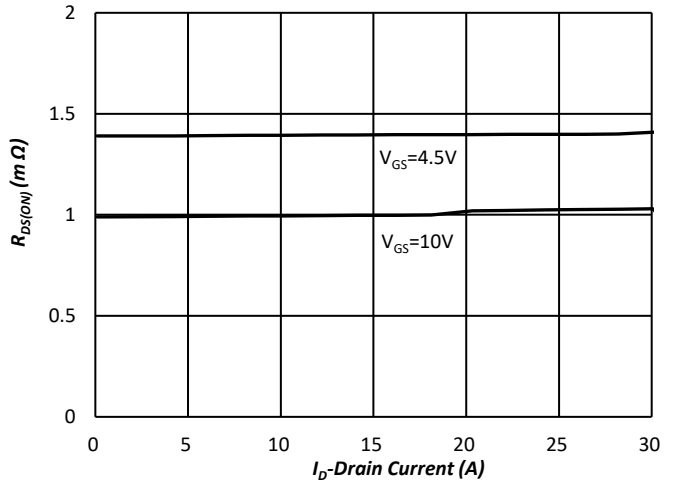


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

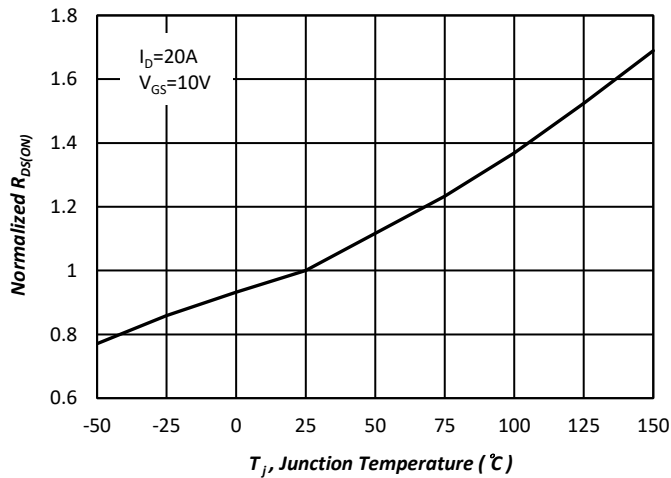


Fig.3 Normalized On-Resistance v.s. Junction Temperature

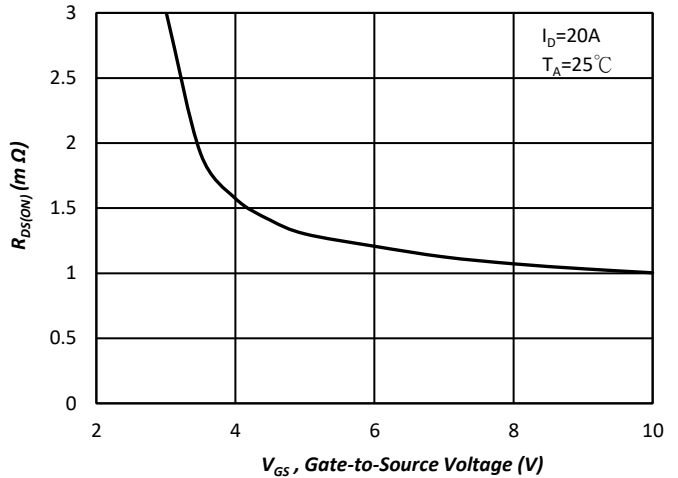


Fig.4 On-Resistance v.s. Gate Voltage

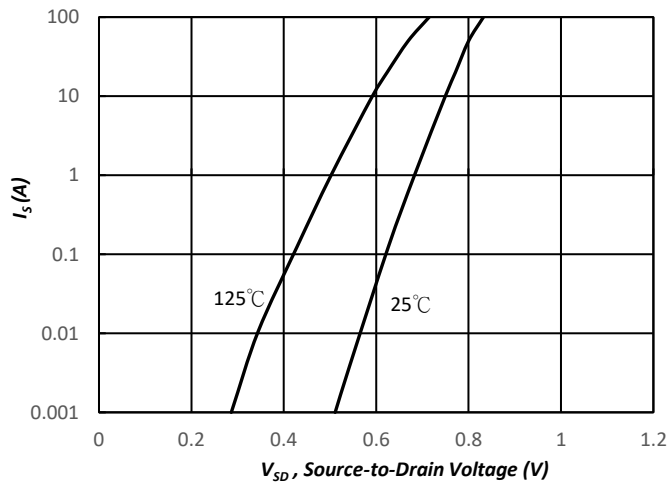


Fig.5 Forward Characteristic of Reverse Diode

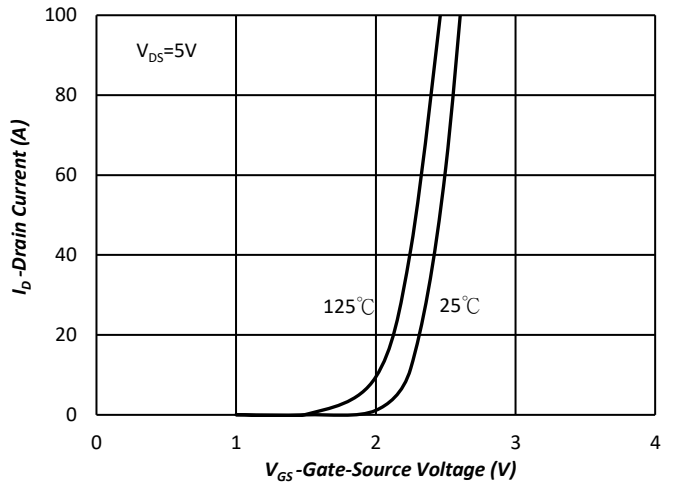


Fig.6 Transfer Characteristics

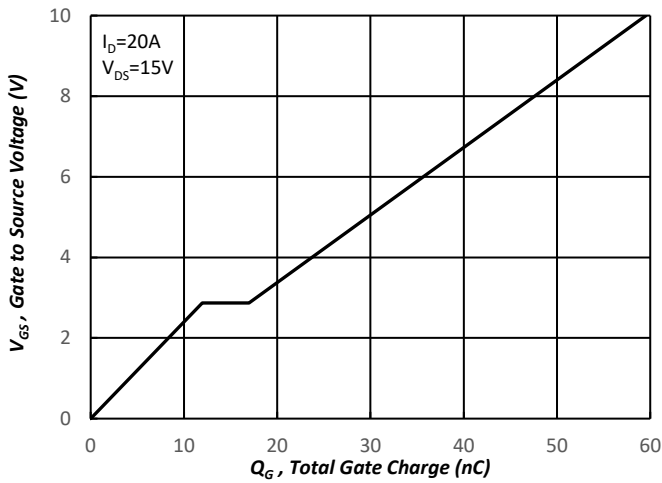


Fig.7 Gate Charge Characteristics

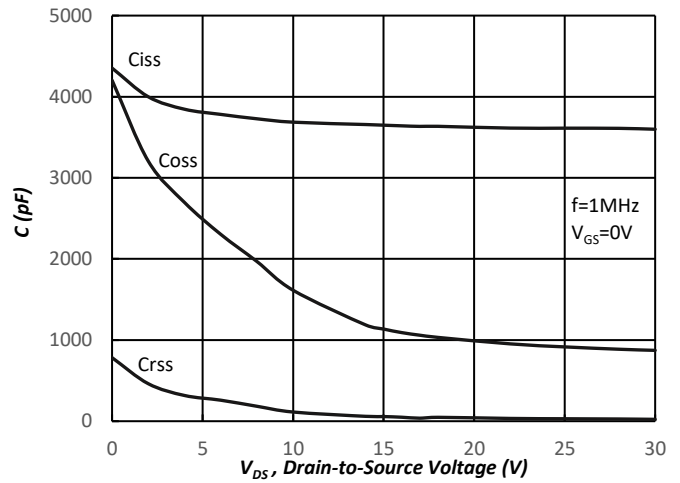


Fig.8 Typical Capacitance Characteristics

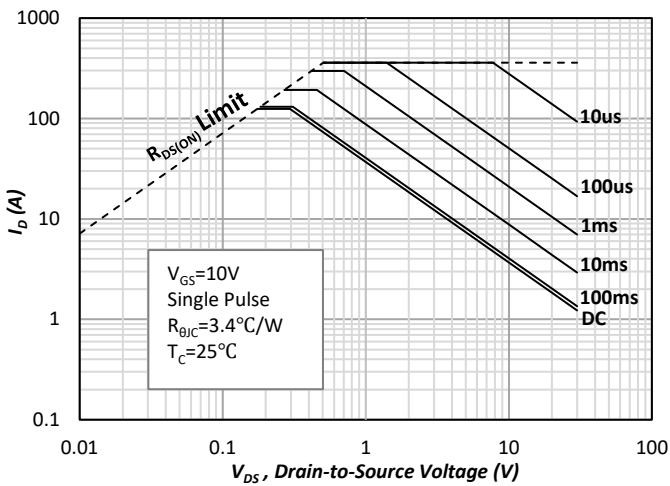


Fig.9. Maximum Safe Operating Area

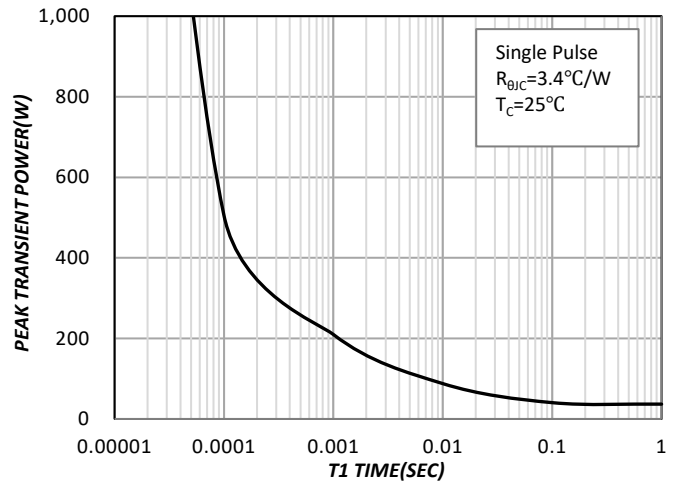


Fig.10. Single Pulse Maximum Power Dissipation

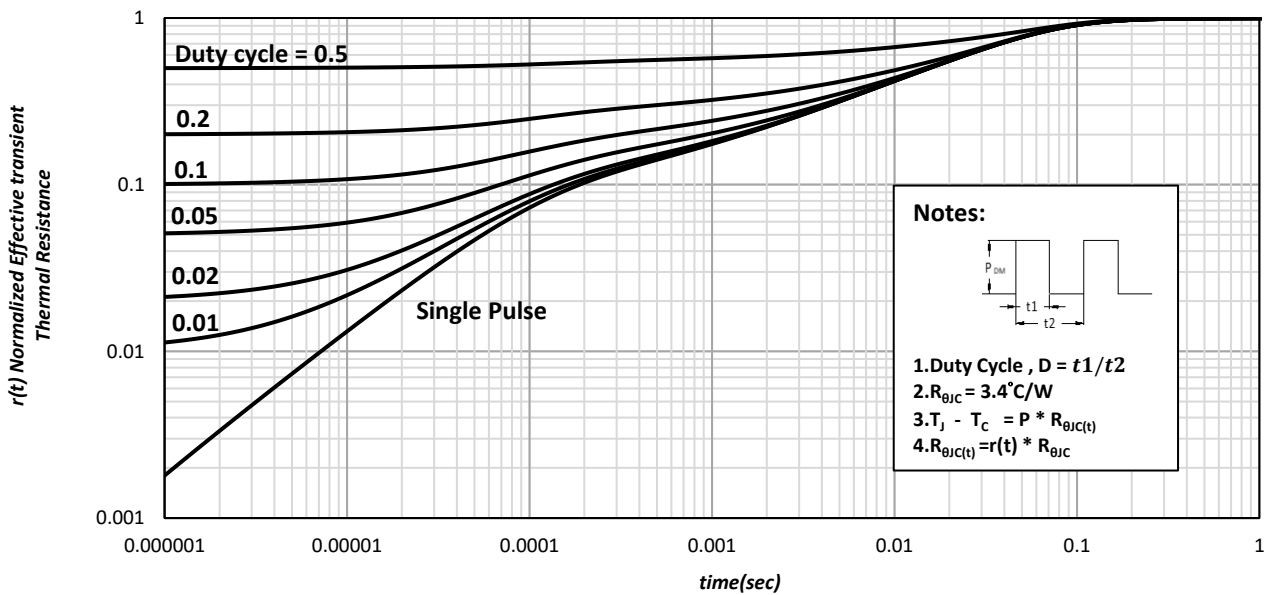
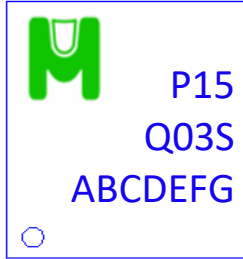


Fig.11. Effective Transient Thermal Impedance

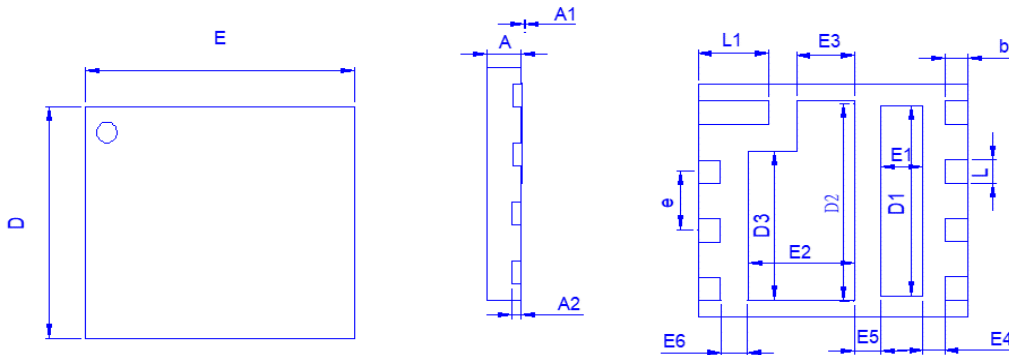
Ordering & Marking Information:

Device Name: EMP15Q03HTCS for DFN5X6A-8L ASYM



→ P15Q03S : Device Name
 → ABCDEFG: Date Code
 A: Assembly House
 B: Year(A:2008 B:2009 C:2010....)
 C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)
 DEFG: Serial No.

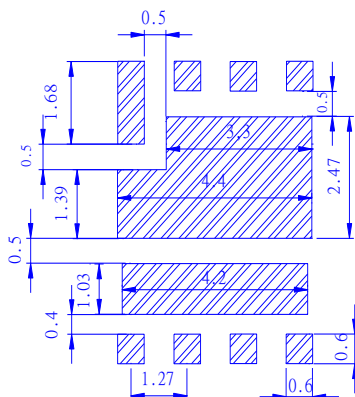
Outline Drawing



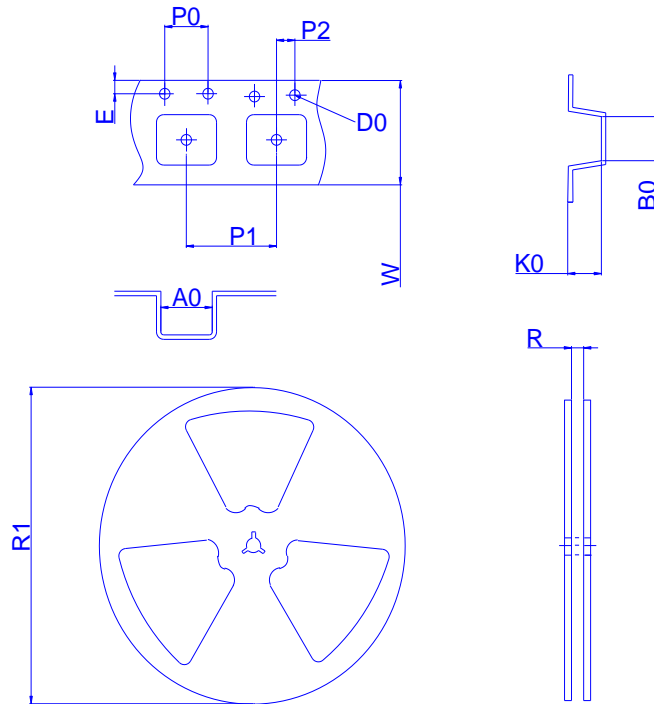
Dimension	A	A1	A2	D	E	D1	D2	D3	E1	E2	E3	E4	E5
Min	0.7	0	0	4.9	5.9	3.85	4.17	3.1	0.83	2.27	1.195	0.4	0.48
Typ.	0.75	0.02	0.2	5	6	3.9	4.22	3.15	0.91	2.37	1.295	0.49	0.53
Max	0.8	0.05	0	5.1	6.1	4.2	4.4	3.305	1.03	2.51	1.42	0.6	0.7

Dimension	E6	L	L1	e	b
Min	0.5	0.4	1.475	1.17	0.4
Typ.	0.6	0.48	1.57	1.27	0.5
Max	0.7	0.6	1.675	1.37	0.6

Footprint



◆ Tape&Reel Information:2500pcs/Reel



Package	DFN5X6A-8L
Reel	13"
Device orientation	<p>FEEED DIRECTION</p>

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	6.4	5.3	1.5	1.8	1.6	4	8	2	12	12.4	330
±	0.2	0.2	0.1	0.1	0.6	0.1	0.1	0.1	0.3	2	2