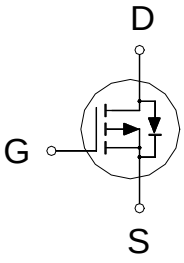
杰力科技股份有限公司
Excelliance MOS Corporation

P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-20V
$R_{DSON\ (MAX.)}$	100mΩ
I_D	-4.5A



Pb-Free Lead Plating & Halogen Free

GP
GREEN PRODUCT

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_A = 25 °C	I_D	-4.5	A
	T_A = 70 °C		-3.3	
Pulsed Drain Current[1]		I_{DM}	-18	
Power Dissipation	T_A = 25 °C	P_D	2.5	W
	T_A = 70 °C		1.6	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		6	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$		50	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]50°C / W when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-0.3	-0.75	-1.2	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -16V, V_{GS} = 0V			-1	μA
		V_{DS} = -16V, V_{GS} = 0V, T_J = 125 °C			-10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -4.5V	-4.5			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -4.5V, I_D = -3.4A		83	100	mΩ
		V_{GS} = -2.5V, I_D = -2.5A		110	135	
		V_{GS} = -1.8V, I_D = -1A		140	180	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -3A		4.5		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -10V, f = 1MHz		450		pF
Output Capacitance	C_{oss}			58		
Reverse Transfer Capacitance	C_{rss}			41		
Total Gate Charge[1,2]	Q_g	V_{DS} = -10V, V_{GS} = -4.5V, I_D = -3A		5.4		nC
Gate-Source Charge[1,2]	Q_{gs}			1.0		
Gate-Drain Charge[1,2]	Q_{gd}			1.3		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = -10V, I_D = -1A, V_{GS} = -4.5V, R_{GS} = 6Ω		10		nS
Rise Time[1,2]	t_r			20		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			15		
Fall Time[1,2]	t_f			12		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				-4.5	A
Pulsed Current[3]	I_{SM}				-18	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			-1.2	V

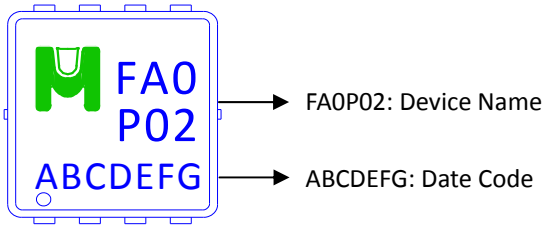
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

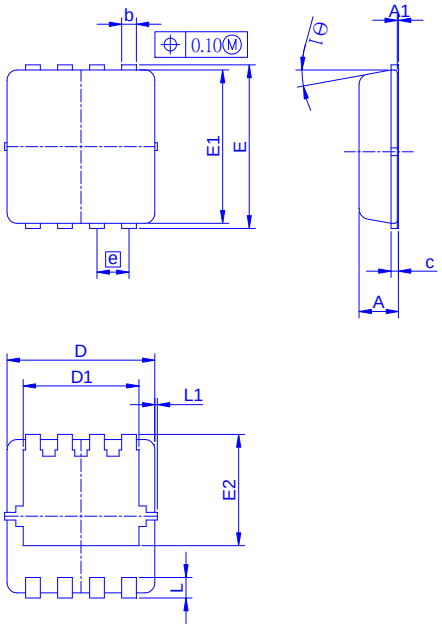
[3]Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMFA0P02V for EDFN 3 x 3



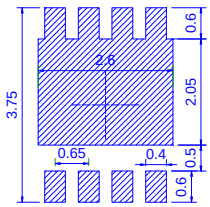
Outline Drawing



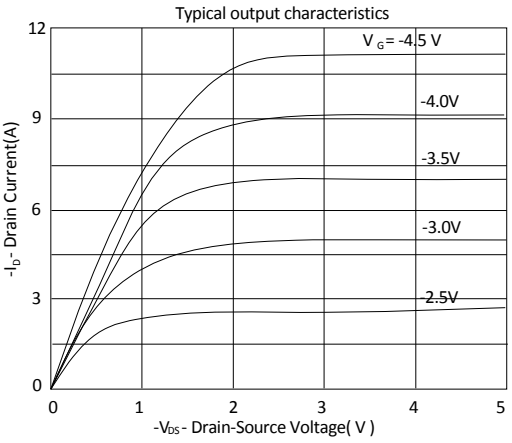
Dimension in mm

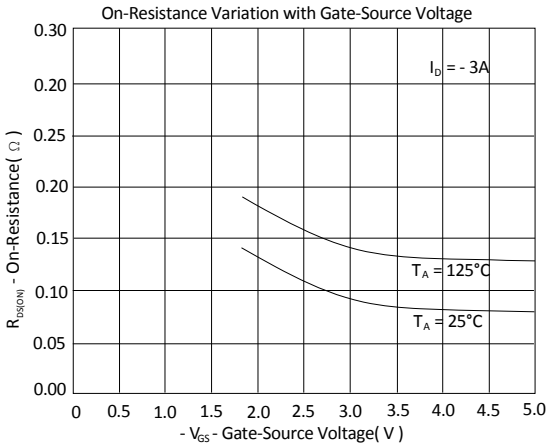
Dimension	A	A1	b	c	D	D1	E	E1	E2	e	L	L1	θ1
Min.	0.65	0	0.20	0.10	2.90	2.15	3.10	2.90	1.53	0.55	0.25	-	0°
Typ.	0.75	-	0.30	0.15	3.00	2.45	3.20	3.00	1.97	0.65	0.40	0.075	10°
Max.	0.90	0.05	0.40	0.25	3.30	2.74	3.50	3.30	2.59	0.75	0.60	0.150	14°

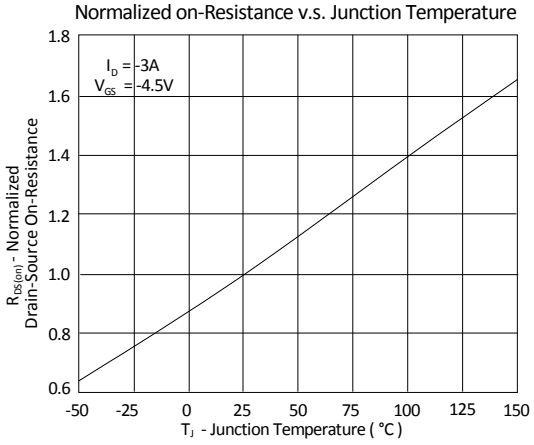
Recommended minimum pads

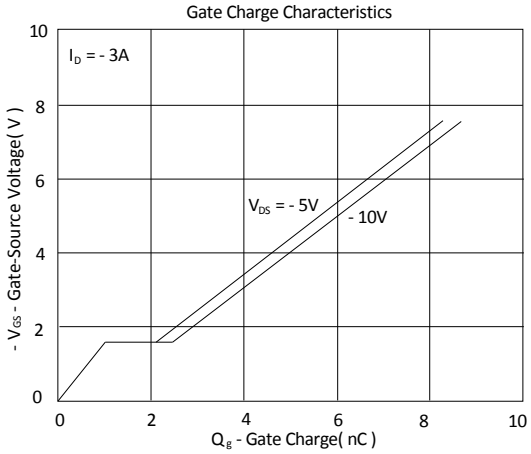


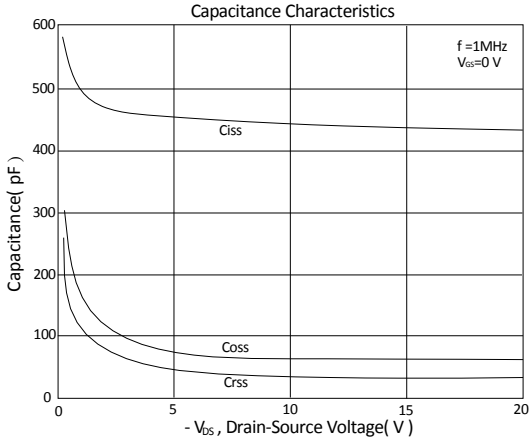
TYPICAL CHARACTERISTICS

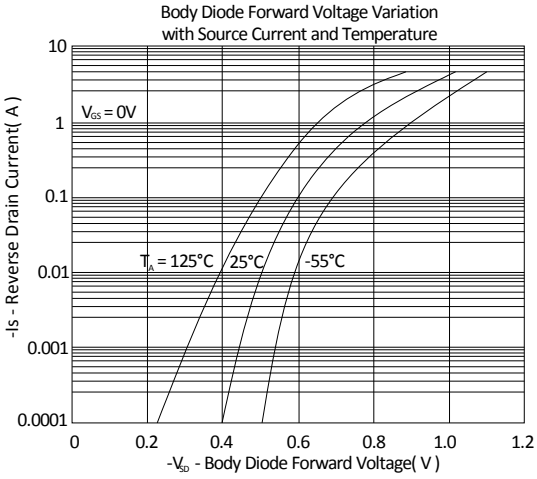




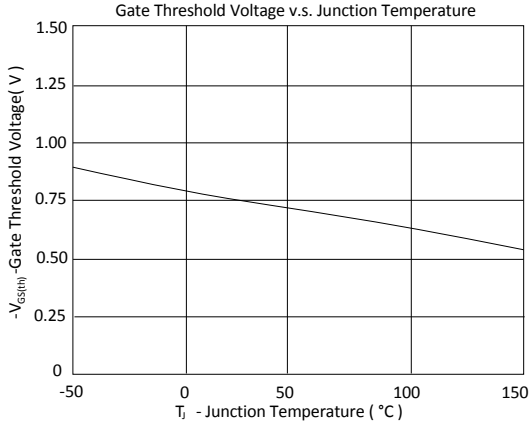




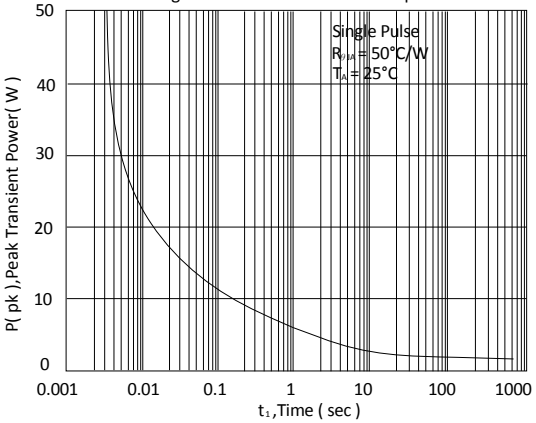




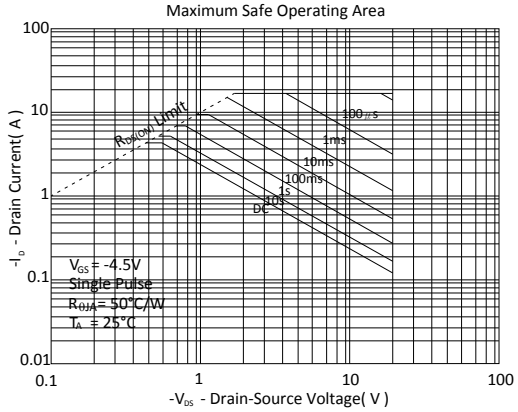
Gate Threshold Voltage v.s. Junction Temperature



Single Pulse Maximum Power Dissipation



Maximum Safe Operating Area



Transient Thermal Response Curve