杰力科技股份有限公司
Excelliance MOS Corporation

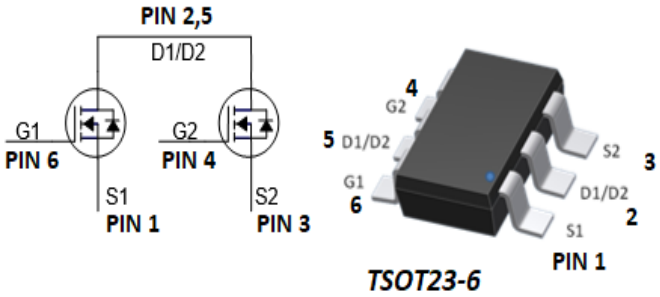
EMF30G02K

Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

▪Product Summary:

	N-CH
BVDSS	20 V
$R_{DSON\ (MAX.)}$@V_{GS}=4.5V	30 mΩ
$R_{DSON\ (MAX.)}$@V_{GS}=2.5V	51 mΩ
I_D @T_A=25°C	5 A

▪ Pin Description:



Dual N Channel MOSFET
Rg 100% Tested
Pb-Free Lead Plating & Halogen Free

▪ ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_A = 25 °C	I_D	5	A
	T_A = 70 °C		4	
Pulsed Drain Current[1]		I_{DM}	20	
Power Dissipation	T_A = 25 °C	P_D	1.3	W
	T_A = 70 °C		0.8	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

▪THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Ambient[3]	$R_{\theta JA}$		100	°C/W

[1]Pulse width limited by maximum junction temperature.
[2]Duty cycle < 1%
[3]100°C / W when mounted on a 1 in^2 pad of 2 oz copper.

▪ **ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage[4]	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250uA	20			V
Gate Threshold Voltage[4]	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250uA	0.45	0.75	1.2	
Gate-Body Leakage[4]	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current[4]	I_{DSS}	V_{DS} = 16V, V_{GS} = 0V			1	uA
		V_{DS} = 16V, V_{GS} = 0V, T_J = 125 °C			10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 4.5V	5			A
Drain-Source On-State Resistance[1,4]	$R_{DS(ON)}$	V_{GS} = 4.5V, I_D = 5A	15	26	30	mΩ
		V_{GS} = 2.5V, I_D = 4A	20	45	51	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 5A		7		S
DYNAMIC						
Input Capacitance[5]	C_{iss}	V_{GS} = 0V, V_{DS} = 10V, f = 1MHz		280		pF
Output Capacitance[5]	C_{oss}			47		
Reverse Transfer Capacitance[5]	C_{rss}			38		
Gate Resistance[4,5]	R_g	f = 1MHz		1.1		Ω
Total Gate Charge[1,2,5]	Q_g	V_{DS} = 10V, V_{GS} = 4.5V, I_D = 5A		6.2		
Gate-Source Charge[1,2,5]	Q_{gs}			0.9		
Gate-Drain Charge[1,2,5]	Q_{gd}			2.1		
Turn-On Delay Time[1,2,5]	$t_{d(on)}$	V_{DS} = 10V, V_{GS} = 4.5V, I_D = 5A , Rg = 6Ω		12.0		nS
Rise Time[1,2,5]	t_r			15.0		
Turn-Off Delay Time[1,2,5]	$t_{d(off)}$			30.0		
Fall Time[1,2,5]	t_f			13.0		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				5	A
Pulsed Current[3]	I_{SM}				20	
Forward Voltage[1,4]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.2	V

[1]Pulse test : Pulse Width ≦ 300 usec, Duty Cycle ≦ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

[4]Guarantee by FT test Item

[5]Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪TYPICAL CHARACTERISTICS

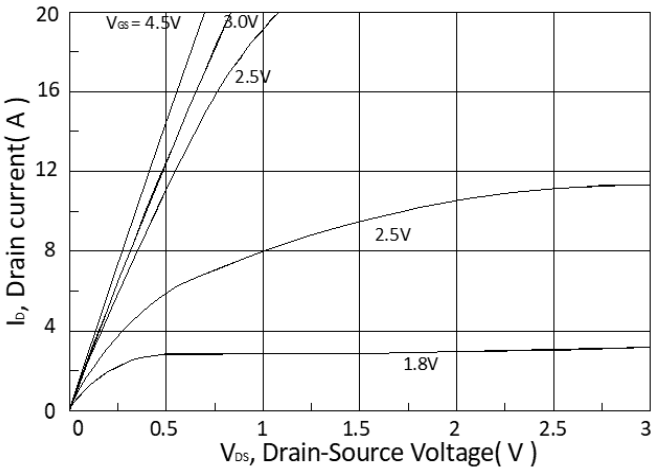


Fig.1 Typical Output Characteristics

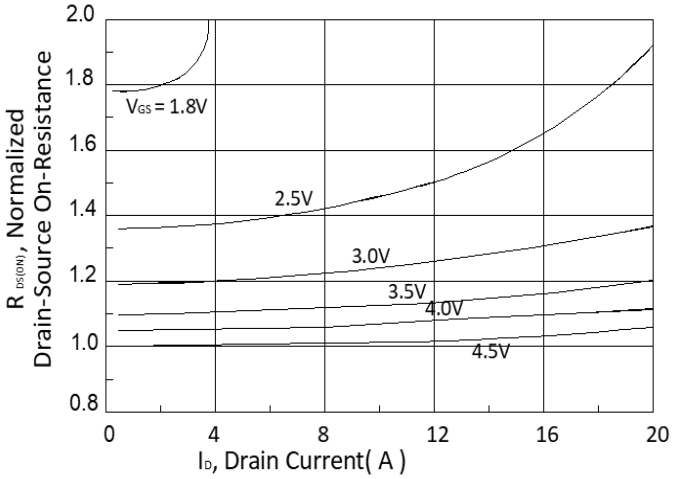


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

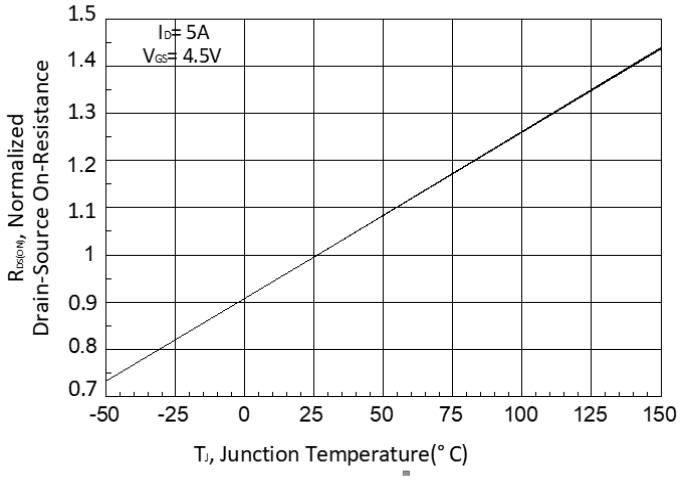


Fig.3 Normalized On-Resistance v.s. Junction Temperature

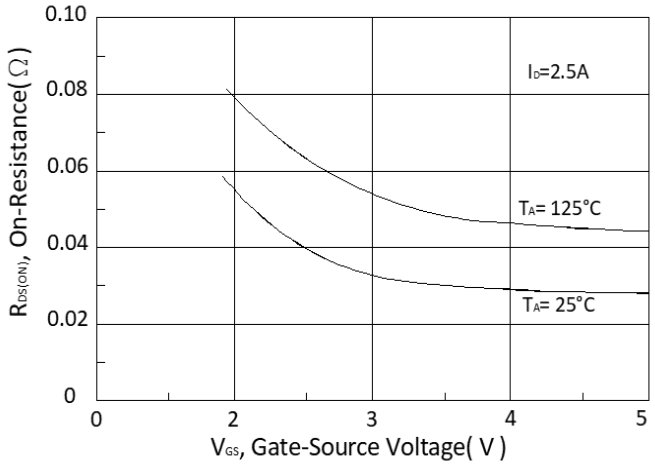


Fig.4 On-Resistance v.s. Gate Voltage

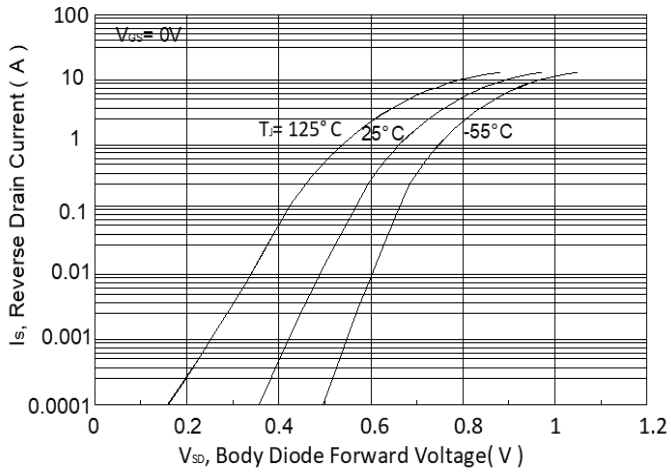


Fig.5 Forward Characteristic of Reverse Diode

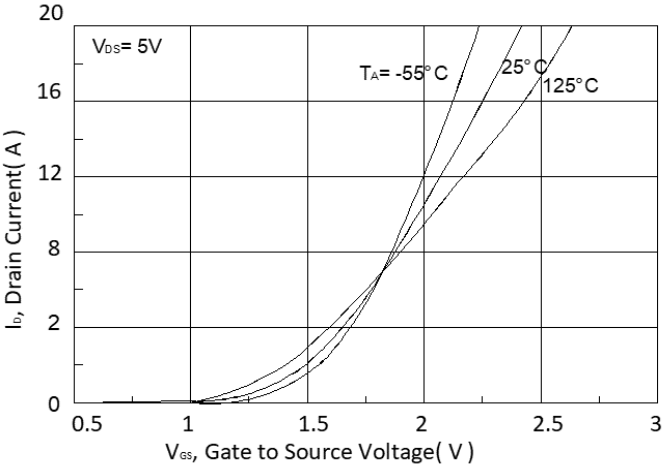


Fig.6 Transfer Characteristics

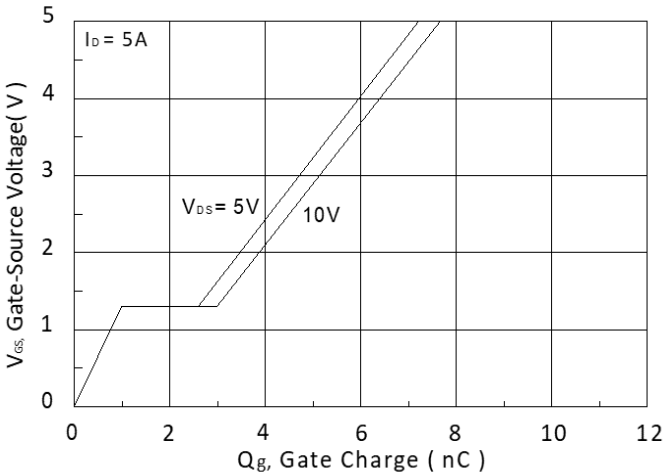


Fig.7 Gate Charge Characteristics

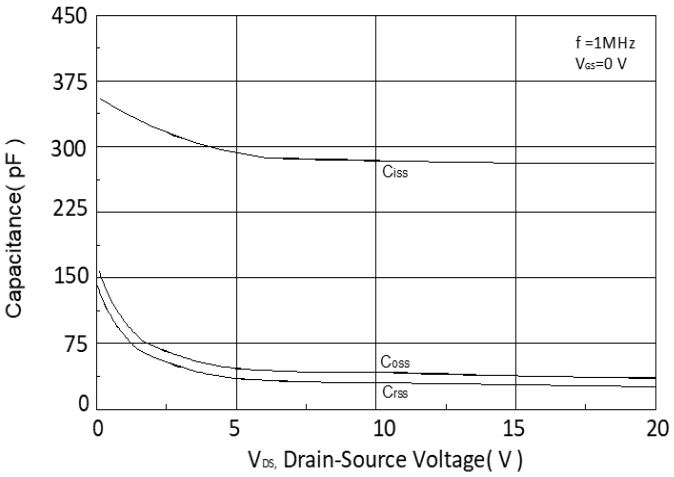


Fig.8 Typical Capacitance Characteristics

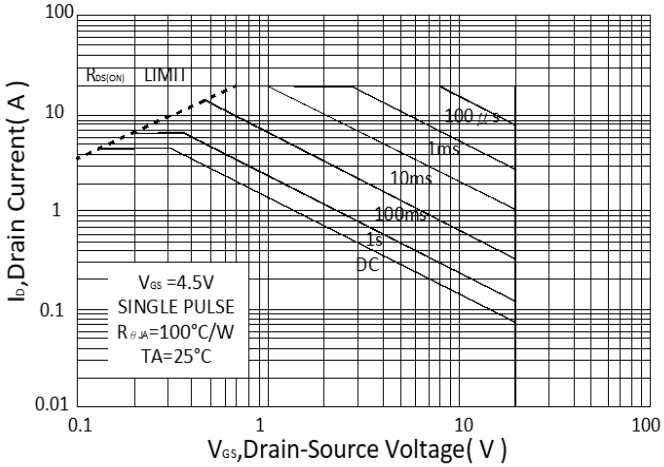


Fig 9. Maximum Safe Operating Area

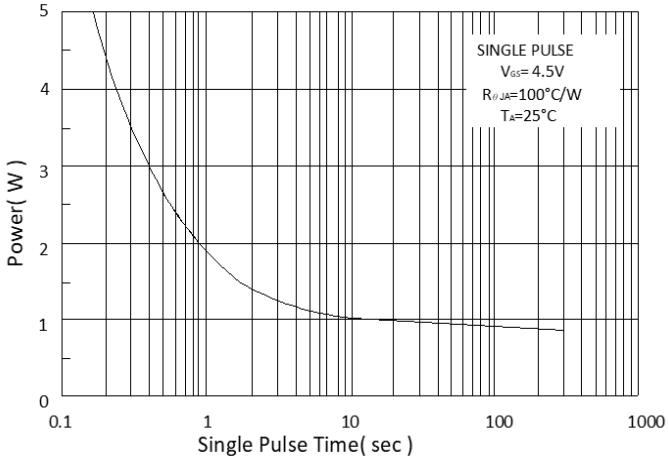


Fig 10. Single Pulse Maximum Power Dissipation

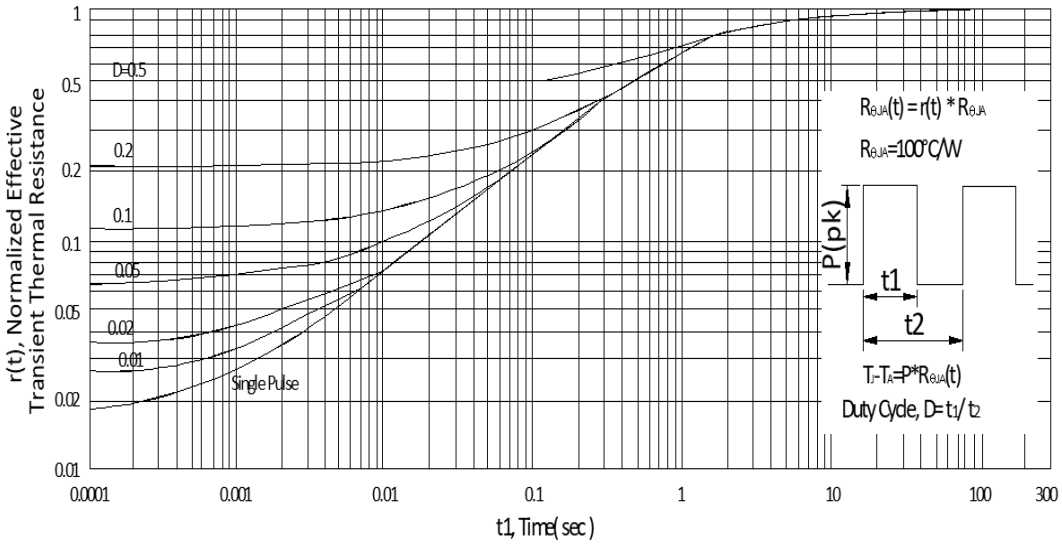
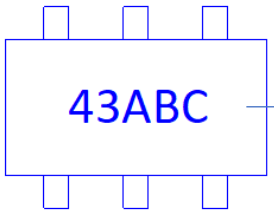


Fig 11. Effective Transient Thermal Impedance

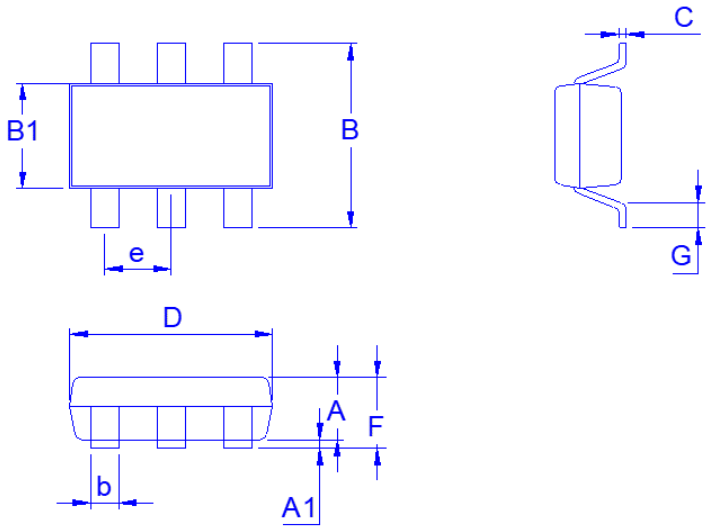
Ordering & Marking Information:

Device Name: EMF30G02K for TSOT23-6



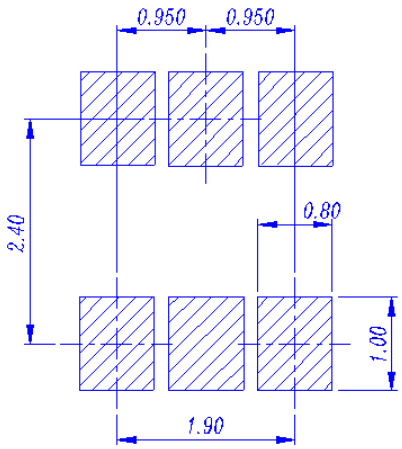
43: Device Code ,43 for EMF30G02K
ABC: Date Code

Outline Drawing

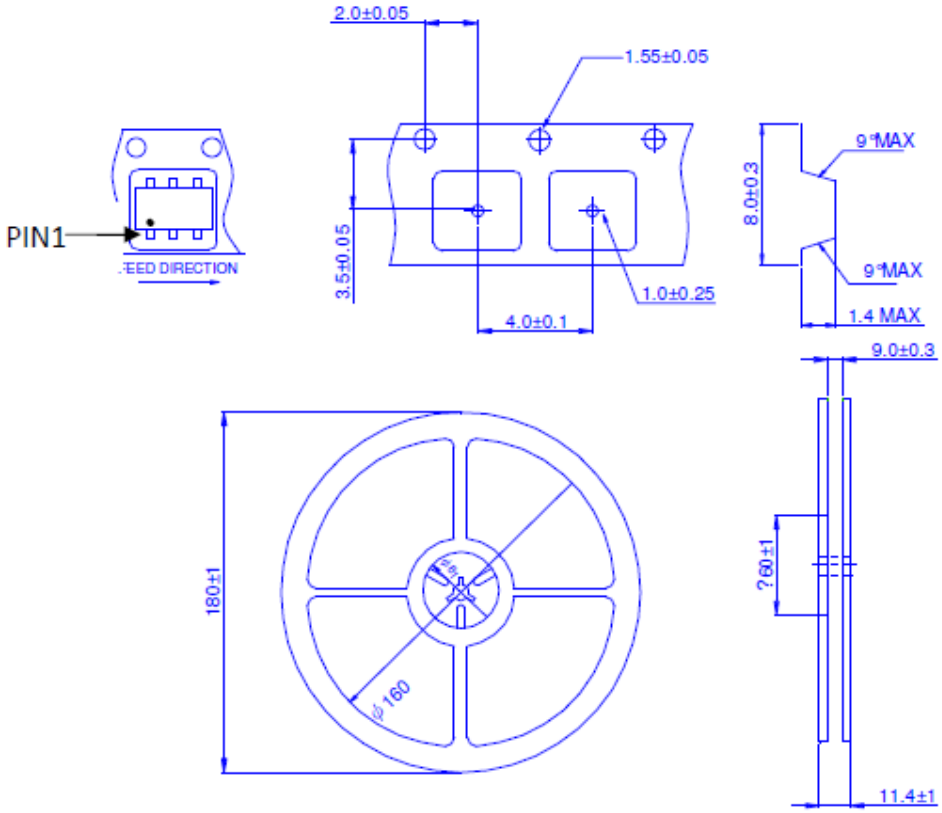


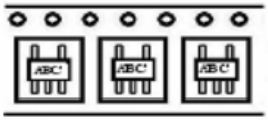
Dimension	A	A1	B	B1	b	C	D	e	F	G
Min.	0.85	0	2.5	1.5	0.3	0.08	2.7		0.85	0.2
Typ.	0.95		2.8	1.6	0.4		2.9	0.95		
Max.	1.25	0.15	3.1	1.7	0.5	0.2	3.1		1.4	0.6

Footprint



◆ **Tape&Reel Information:3000pcs/Reel** (Dimension in millimeter)



產品別	TSOT23-6
Reel尺寸	7"
編帶方式	R-Type 
前空格	50
後空格	50
裝箱數	
滿捲數量	3K
捲/內盒比	05:01
內盒滿箱數	15K
內/外箱比	08:01
外箱滿箱數	120K