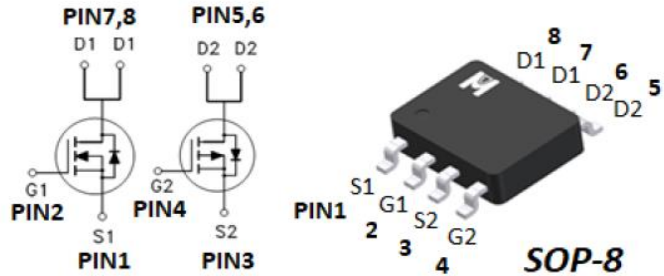


N-Channel + P-Channel Logic Level Enhancement Mode Field Effect Transistor

•Product Summary:

	N-CH	P-CH
BV_{DSS}	20V	-20V
$R_{DSON (MAX.)}@V_{GS}=4.5V$	20m Ω	78m Ω
$R_{DSON (MAX.)}@V_{GS}=2.5V$	30m Ω	105m Ω
$I_D @T_C=25^\circ C$	13A	-5A
$I_D @T_A=25^\circ C$	6A	-3A

• Pin Description:



N + P Channel MOSFET

UIS, Rg 100% Tested

RoHS & Halogen Free & TSCA Compliant



• ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS		UNIT	
		N-CH	P-CH		
Gate-Source Voltage	V_{GS}	± 12	± 12	V	
Continuous Drain Current	I_D	$T_C = 25^\circ C$	13	-5	A
		$T_C = 100^\circ C$	8	-3	
Continuous Drain Current	I_D	$T_A = 25^\circ C$	6	-3	
		$T_A = 70^\circ C$	5	-2	
Pulsed Drain Current ¹	I_{DM}	22	-10		
Avalanche Current	I_{AS}	21	-16		
Avalanche Energy	EAS	L = 0.1mH	22	12.8	mJ
Repetitive Avalanche Energy ²		L = 0.05mH	11	6.4	
Power Dissipation	P_D	$T_C = 25^\circ C$	6	4.6	W
		$T_C = 100^\circ C$	2.4	1.9	
Power Dissipation	P_D	$T_A = 25^\circ C$	1.3	1.5	W
		$T_A = 70^\circ C$	0.8	1	
Operating Junction & Storage Temperature Range	T_j, T_{stg}	-55 to 150		$^\circ C$	

• 100% UIS testing in condition of $V_D=25V, L=0.1mH, V_G=4.5V, I_L=13A$, Rated $V_{DS}=20V$ N-CH

• 100% UIS testing in condition of $V_D=25V, L=0.1mH, V_G=4.5V, I_L=10A$, Rated $V_{DS}=20V$ P-CH

•THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM		UNIT
			N-CH	P-CH	
Junction-to-Case	$R_{\theta JC}$		21	27	$^\circ C/W$
Junction-to-Ambient ^{3,4}	$R_{\theta JA}$	$t \leq 10s$	76	65	
		Steady-State	95	81	

¹Pulse width limited by maximum junction temperature.

²Duty cycle < 1%

³The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ C$.

⁴Guarantee by Engineering test



▪ N-CH_ELECTRICAL CHARACTERISTICS (T_j = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	20			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	0.45	0.7	1.2	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 16V, V _{GS} = 0V			1	μA
		V _{DS} = 16V, V _{GS} = 0V, T _j = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 5V, V _{GS} = 4.5V	13			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 4.5V, I _D = 6A		15	20	mΩ
		V _{GS} = 2.5V, I _D = 4A		21	30	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 6A		7		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 10V, f = 1MHz		711		pF
Output Capacitance ⁵	C _{oss}			114		
Reverse Transfer Capacitance ⁵	C _{rss}			101		
Gate Resistance ^{4,5}	R _g	f = 1MHz		1.5		Ω
Total Gate Charge ^{1,2,5}	Q _g	V _{DS} = 10V, V _{GS} = 4.5V, I _D = 5A		11		nC
Gate-Source Charge ^{1,2,5}	Q _{gs}			1.5		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			3.1		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 10V, V _{GS} = 10V, I _D = 5A, R _g = 3Ω		8.7		nS
Rise Time ^{1,2,5}	t _r			22		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			32		
Fall Time ^{1,2,5}	t _f			29.4		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				13	A
Pulsed Current ³	I _{SM}				52	
Forward Voltage ^{1,4}	V _{SD}	I _F = I _S , V _{GS} = 0V			1.3	V
Reverse Recovery Time ⁵	t _{rr}	I _F = I _S , dI _F /dt = 100A / μS		6.6		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			0.37		A
Reverse Recovery Charge ⁵	Q _{rr}			1.4		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.



▪ N-CH_TYPICAL CHARACTERISTICS

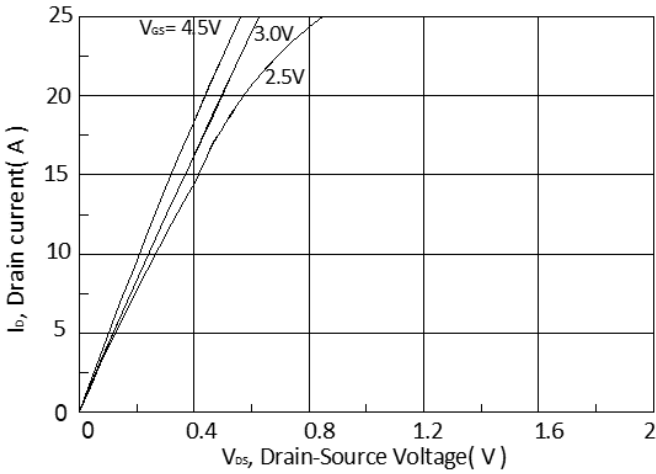


Fig.1 Typical Output Characteristics

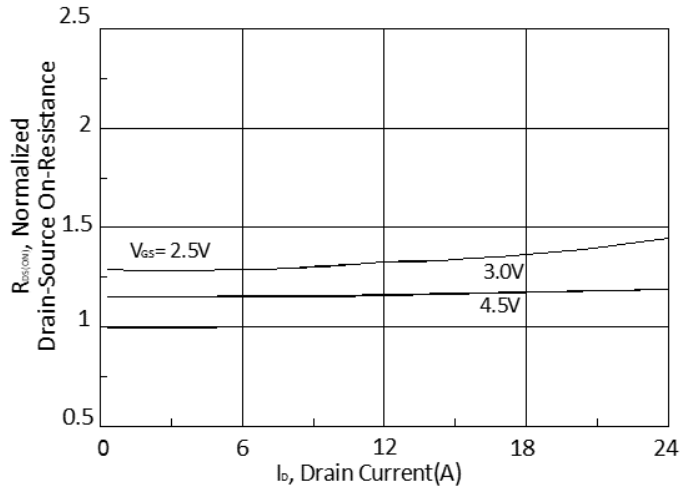


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

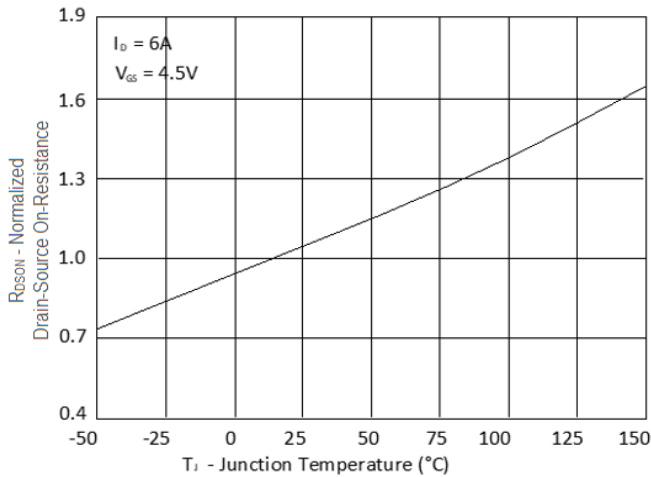


Fig.3 Normalized On-Resistance v.s. Junction Temperature

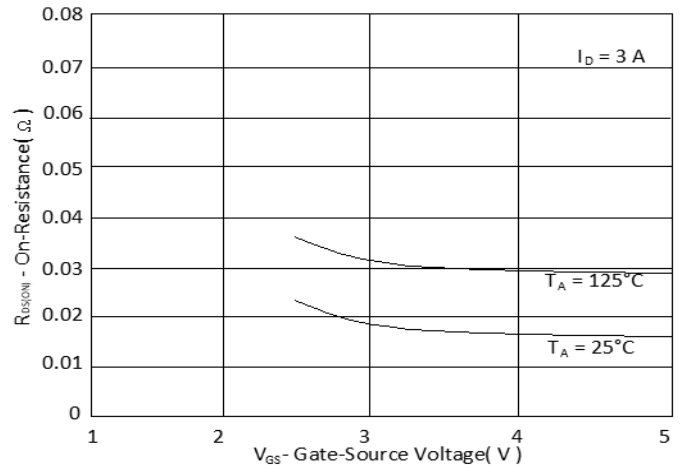


Fig.4 On-Resistance v.s. Gate Voltage

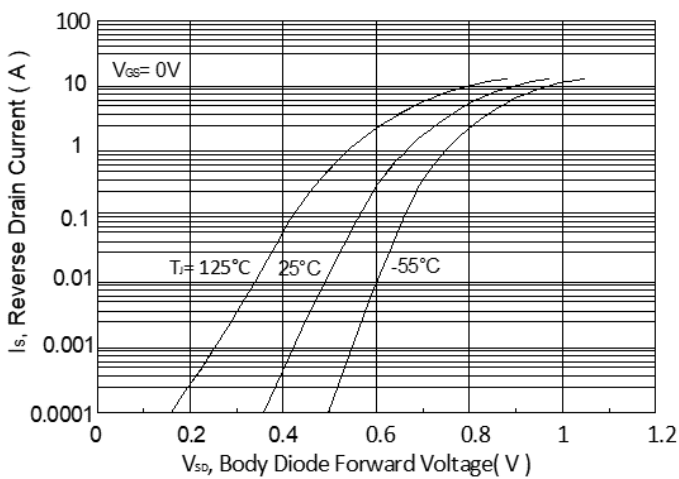


Fig.5 Forward Characteristic of Reverse Diode

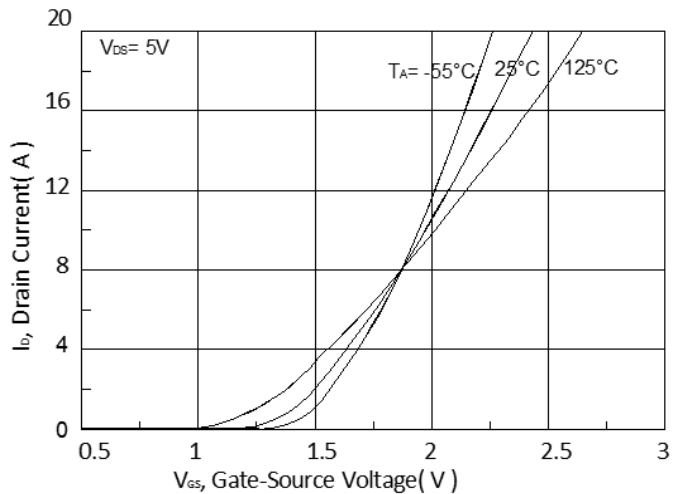


Fig.6 Transfer Characteristics

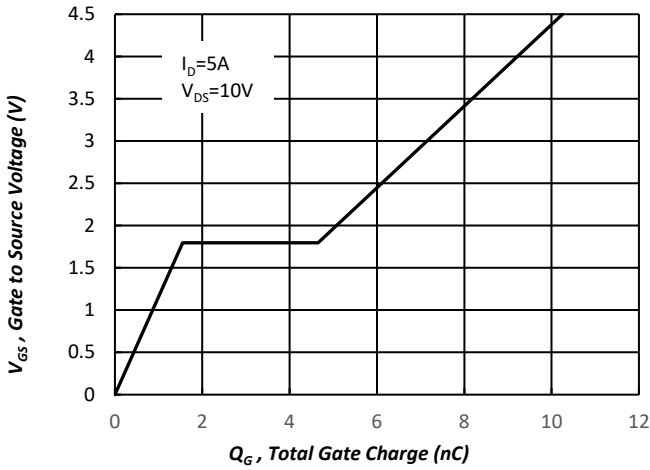


Fig.7 Gate Charge Characteristics

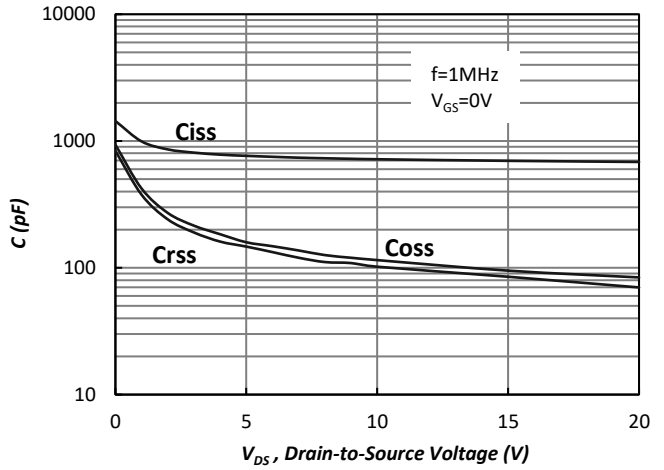


Fig.8 Typical Capacitance Characteristics

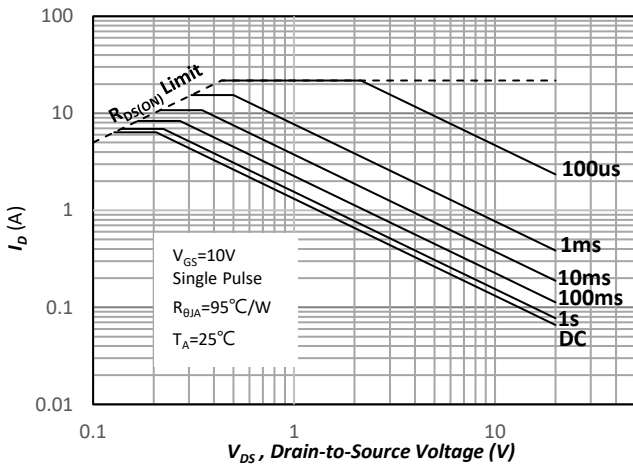


Fig.9. Maximum Safe Operating Area

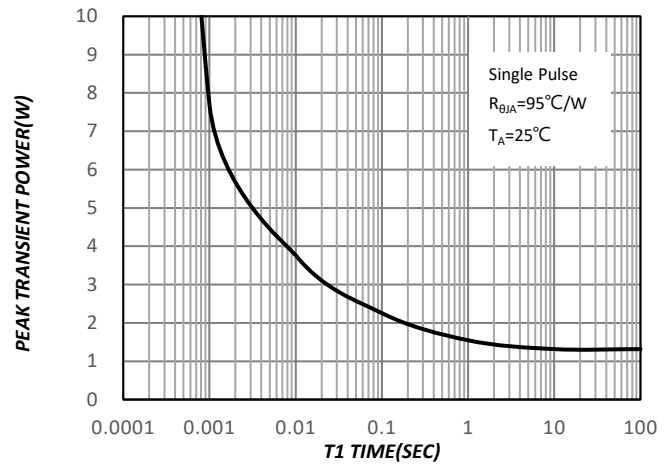


Fig.10. Single Pulse Maximum Power Dissipation

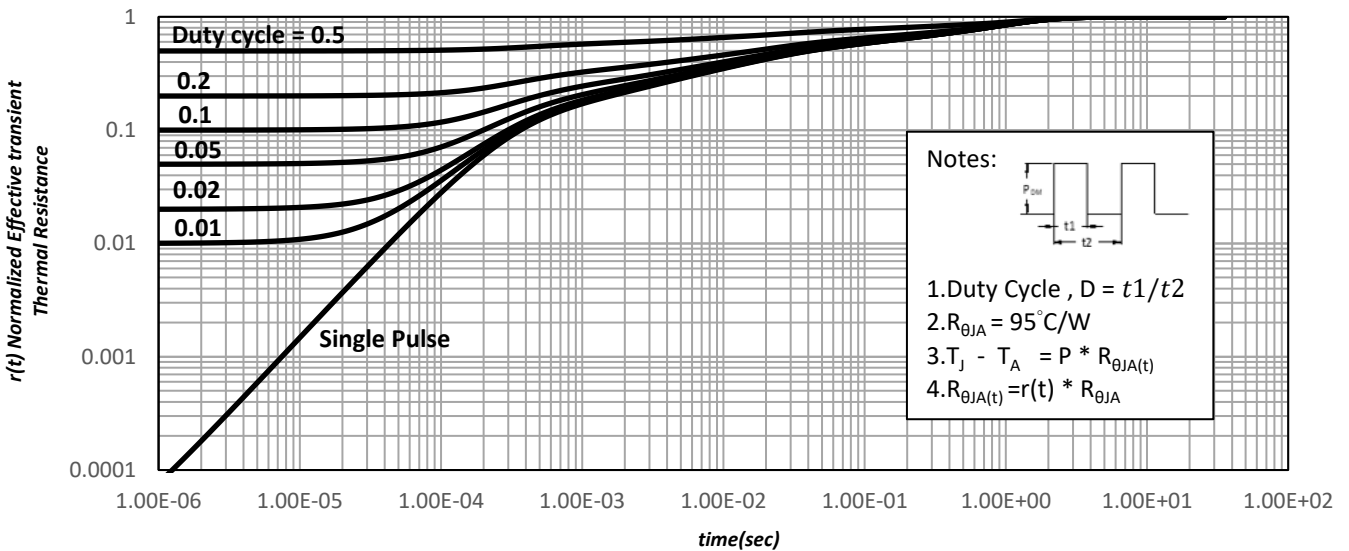


Fig.11. Effective Transient Thermal Impedance

▪ P-CH_ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-20			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-0.45	-0.8	-1.2	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = -16V, V _{GS} = 0V			1	μA
		V _{DS} = -16V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = -5V, V _{GS} = -4.5V	-5			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = -4.5V, I _D = -3.5A		60	78	mΩ
		V _{GS} = -2.5V, I _D = -2A		81	105	
Forward Transconductance ¹	g _{fs}	V _{DS} = -5V, I _D = -3.5A		10		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = -10V, f = 1MHz		395		pF
Output Capacitance ⁵	C _{oss}			77		
Reverse Transfer Capacitance ⁵	C _{rss}			53		
Gate Resistance ^{4,5}	R _g	f = 1MHz		9.7		Ω
Total Gate Charge ^{1,2,5}	Q _g	V _{DS} = -10V, V _{GS} = -4.5V, I _D = -5A		4.4		nC
Gate-Source Charge ^{1,2,5}	Q _{gs}			1.2		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			1.0		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = -10V, V _{GS} = -4.5V, I _D = -5A, R _g = 3Ω		7.5		nS
Rise Time ^{1,2,5}	t _r			25.5		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			23.2		
Fall Time ^{1,2,5}	t _f			33.6		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				-5	A
Pulsed Current ³	I _{SM}				-20	
Forward Voltage ^{1,4}	V _{SD}	I _F = I _S , V _{GS} = 0V			-1.3	V
Reverse Recovery Time ⁵	t _{rr}	I _F = I _S , dI _F /dt = 100A / μS		9.4		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			0.78		A
Reverse Recovery Charge ⁵	Q _{rr}			3.7		nC

¹ Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

² Independent of operating temperature.

³ Pulse width limited by maximum junction temperature.

⁴ Guarantee by FT test Item

⁵ Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.



▪ P-CH_TYPICAL CHARACTERISTICS

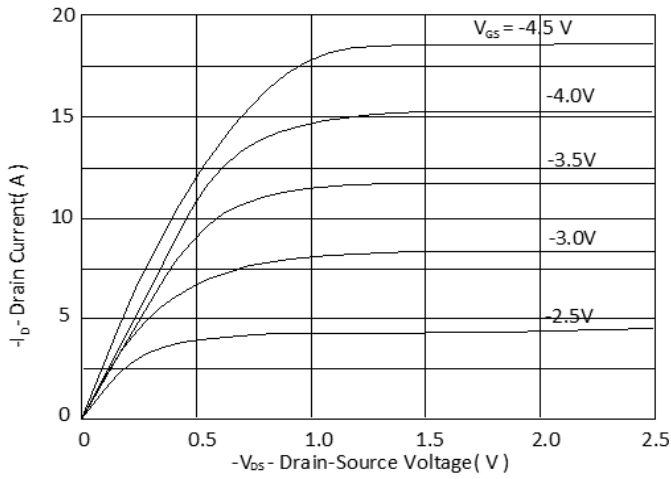


Fig.1 Typical Output Characteristics

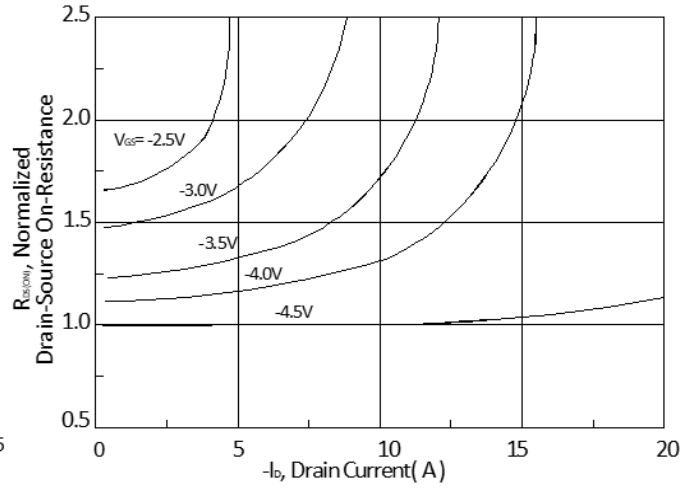


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

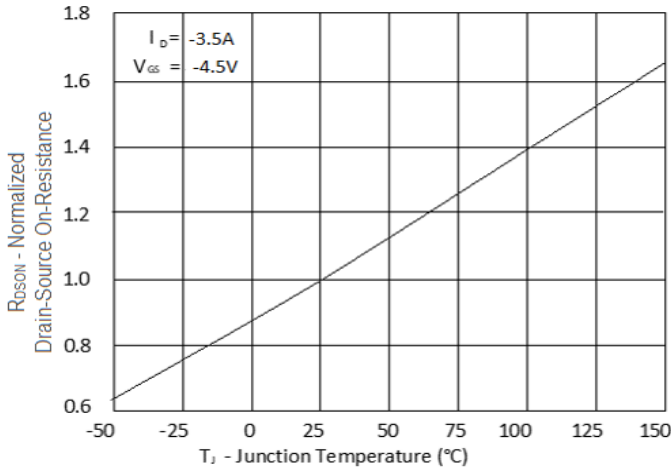


Fig.3 Normalized On-Resistance v.s. Junction Temperature

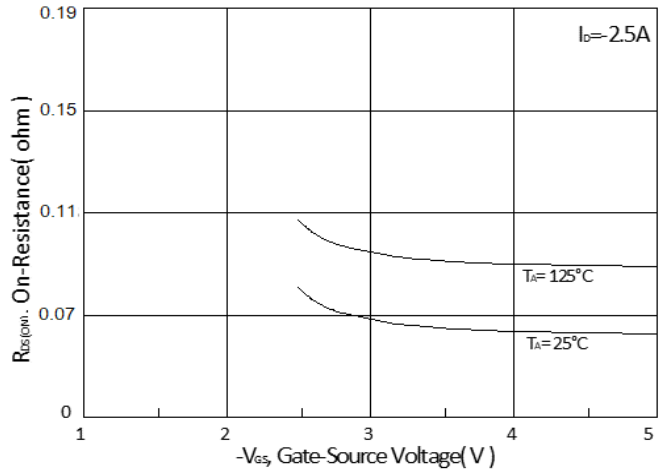


Fig.4 On-Resistance v.s. Gate Voltage

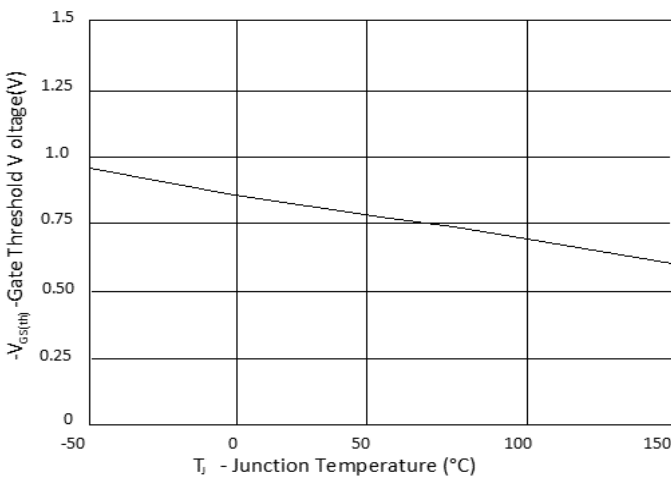


Fig.5 Forward Characteristic of Reverse Diode

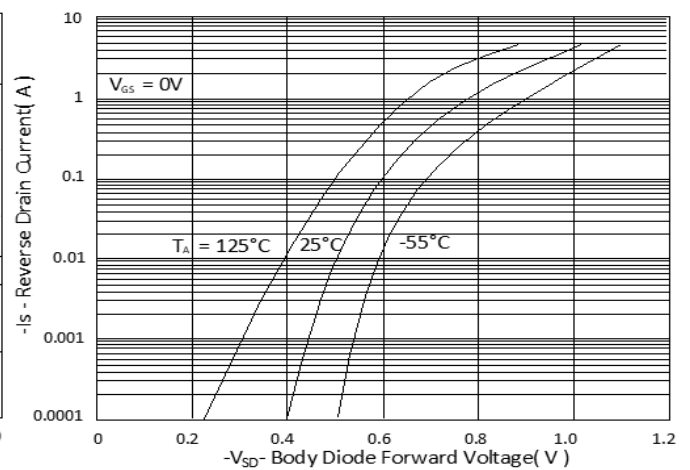


Fig.6 Transfer Characteristics

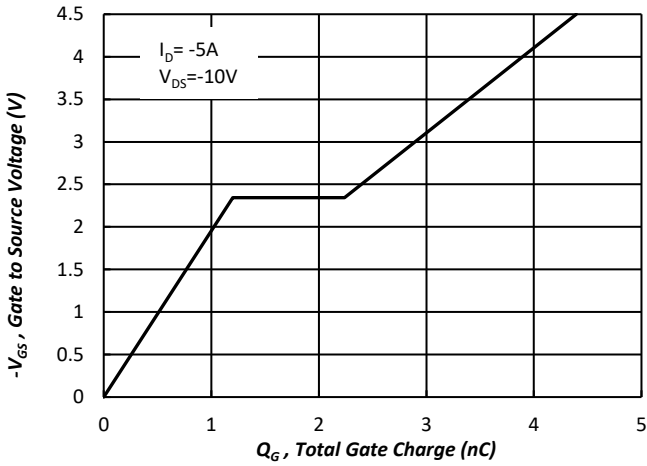


Fig.7 Gate Charge Characteristics

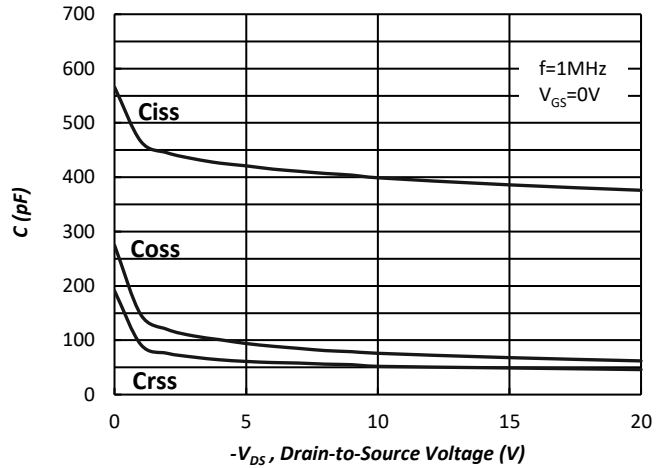


Fig.8 Typical Capacitance Characteristics

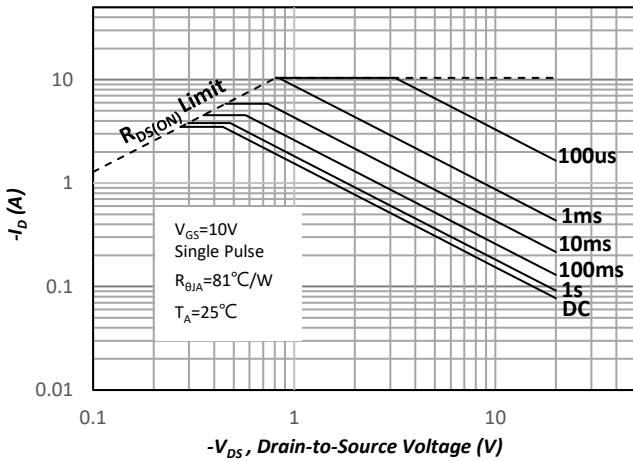


Fig.9. Maximum Safe Operating Area

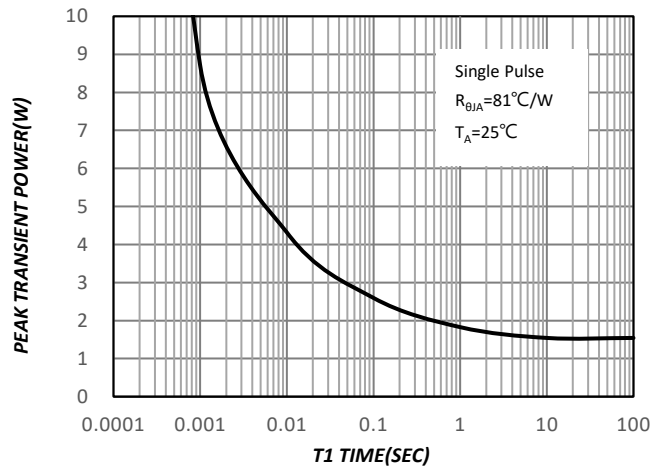


Fig.10. Single Pulse Maximum Power Dissipation

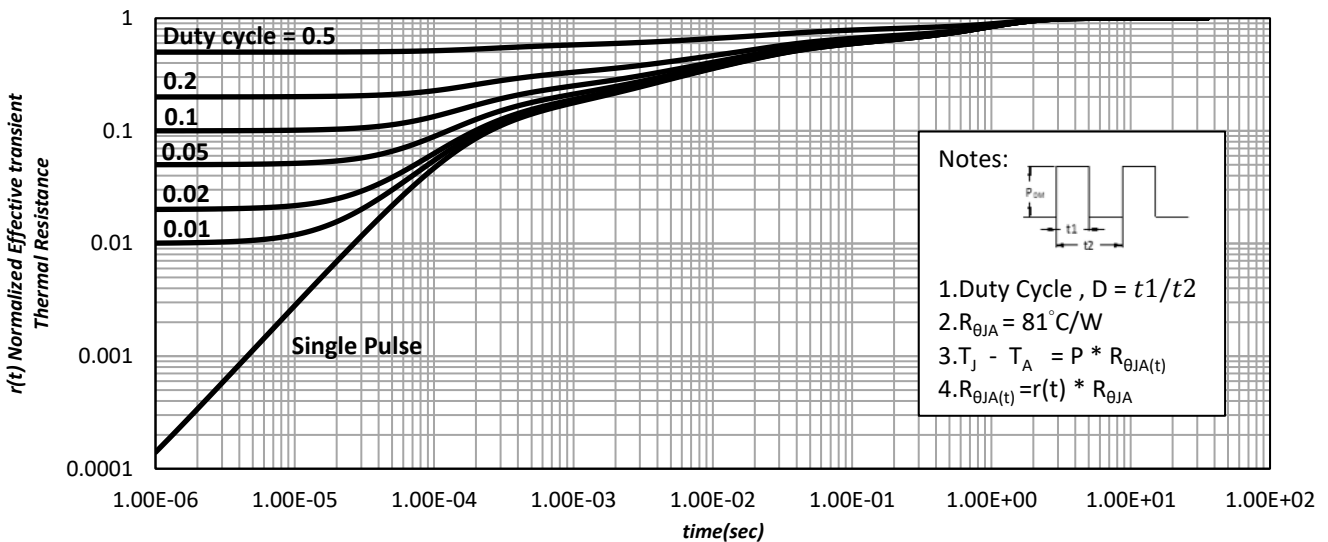


Fig.11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMF20C02G for SOP-8



F20C02: Device Name

ABCDEFGG: Date Code

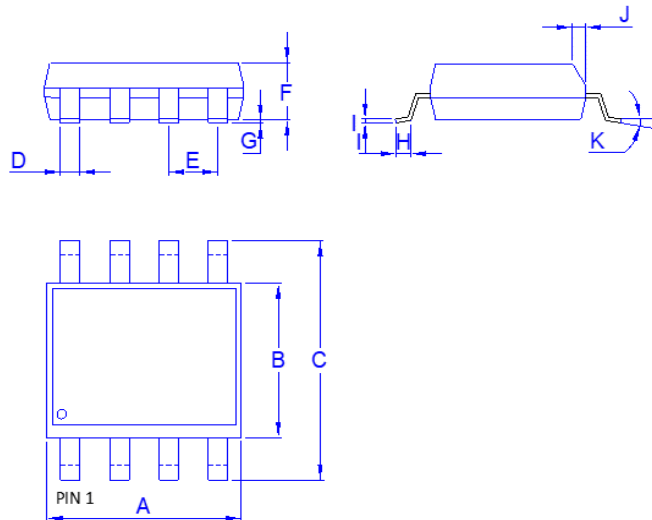
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

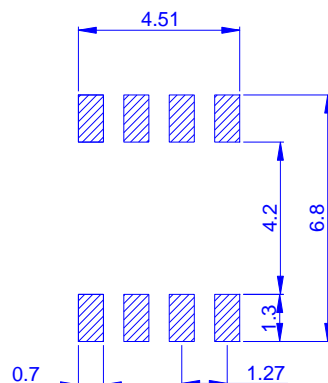
DEFG: Serial No.

Outline Drawing

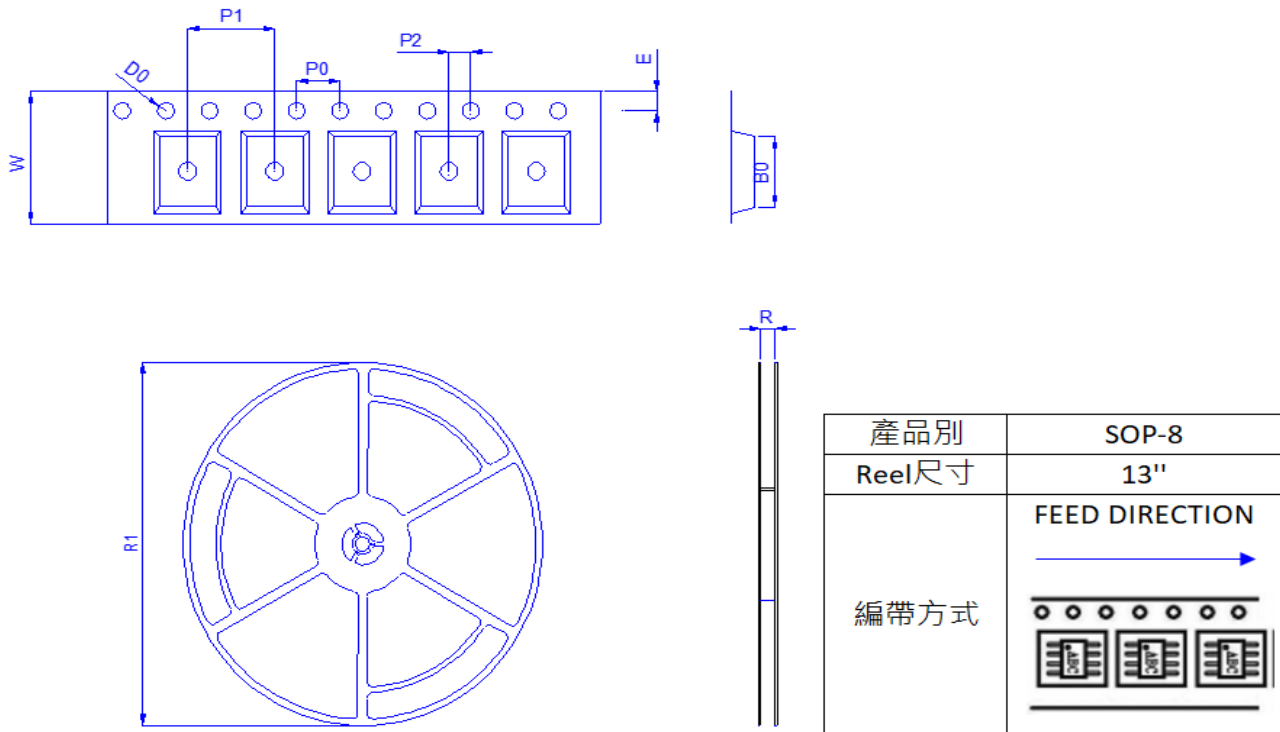


Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.7	3.8	5.8	0.31		1.35	0.01	0.4	0.1	0.25	0°
Typ.	4.9	3.9	6	0.41	1.27	1.55	0.18	0.6	0.2	0.3	
Max.	5.1	4	6.2	0.51		1.75	0.25	1.27	0.25	0.5	8°

Footprint



◆ Tape&Reel Information:2500pcs/Reel



Dimension in mm

Dimension	Carrier tape							Reel	
	B0	D0	E	P0	P1	P2	W	R	R1
Typ.	6.5	1.5	1.75	4	8	2	12	12.4	330
±	0.4	0.2	0.2	0.2	0.2	0.2	0.5	REF	REF