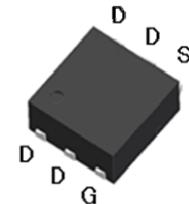
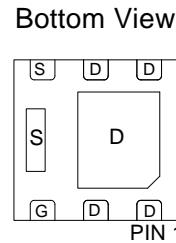
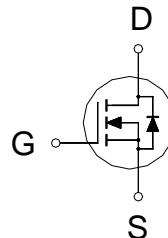


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV <sub>DSS</sub>	20V
R <sub>DSON</sub> (MAX.)	14.8mΩ
I <sub>D</sub>	8A



UIS, R<sub>G</sub> 100% Tested

Pb-Free Lead Plating & Halogen Free



**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C Unless Otherwise Noted)**

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V <sub>GS</sub>	±12	V
Continuous Drain Current	T <sub>A</sub> = 25 °C	I <sub>D</sub>	8	A
	T <sub>A</sub> = 70 °C		6.2	
Pulsed Drain Current <sup>1</sup>		I <sub>DM</sub>	32	
Avalanche Current		I <sub>AS</sub>	10	
Avalanche Energy	L = 0.1mH, I <sub>AS</sub> =10A, RG=25Ω	E <sub>AS</sub>	5	mJ
Repetitive Avalanche Energy <sup>2</sup>	L = 0.05mH	E <sub>AR</sub>	2.5	
Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.08	W
	T <sub>A</sub> = 70 °C		1.33	
Operating Junction & Storage Temperature Range		T <sub>j</sub> , T <sub>stg</sub>	-55 to 150	°C

**THERMAL RESISTANCE RATINGS**

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R <sub>θJC</sub>	12	60	°C / W
Junction-to-Ambient <sup>3</sup>	R <sub>θJA</sub>			

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle ≤ 1%

<sup>3</sup>60°C / W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0V, I_D = 250\mu\text{A}$	20			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	0.4	0.75	1.2	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 12V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 16V, V_{GS} = 0V$			1	$\mu\text{A}$
		$V_{DS} = 16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$			10	
On-State Drain Current <sup>1</sup>	$I_{D(\text{ON})}$	$V_{DS} = 5V, V_{GS} = 4.5V$	8			A
Drain-Source On-State Resistance <sup>1</sup>	$R_{DS(\text{ON})}$	$V_{GS} = 4.5V, I_D = 8A$		13	14.8	$\text{m}\Omega$
		$V_{GS} = 2.5V, I_D = 5A$		19	23	
Forward Transconductance <sup>1</sup>	$g_{fs}$	$V_{DS} = 5V, I_D = 8A$		9		S
DYNAMIC						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = 10V, f = 1\text{MHz}$		1192		$\text{pF}$
Output Capacitance	$C_{oss}$			203		
Reverse Transfer Capacitance	$C_{rss}$			174		
Total Gate Charge <sup>1,2</sup>	$Q_g$	$V_{DS} = 10V, V_{GS} = 4.5V, I_D = 8A$		14.2		$\text{nC}$
Gate-Source Charge <sup>1,2</sup>	$Q_{gs}$			1.8		
Gate-Drain Charge <sup>1,2</sup>	$Q_{gd}$			5		
Turn-On Delay Time <sup>1,2</sup>	$t_{d(\text{on})}$	$V_{DS} = 10V, I_D = 1A, V_{GS} = 4.5V, R_{GS} = 6\Omega$		15		$\text{nS}$
Rise Time <sup>1,2</sup>	$t_r$			18		
Turn-Off Delay Time <sup>1,2</sup>	$t_{d(\text{off})}$			35		
Fall Time <sup>1,2</sup>	$t_f$			20		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ )						
Continuous Current	$I_S$				8	$\text{A}$
Pulsed Current <sup>3</sup>	$I_{SM}$				32	
Forward Voltage <sup>1</sup>	$V_{SD}$	$I_F = I_S, V_{GS} = 0V$			1.2	V

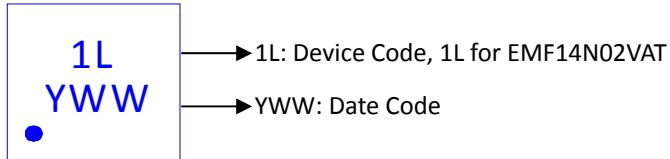
<sup>1</sup>Pulse test : Pulse Width  $\leq 300 \mu\text{sec}$ , Duty Cycle  $\leq 2\%$ .

<sup>2</sup>Independent of operating temperature.

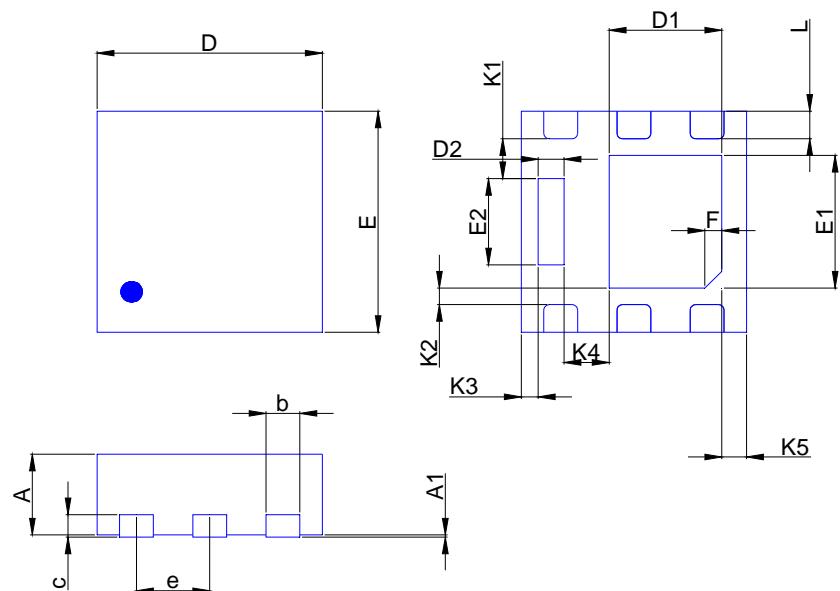
<sup>3</sup>Pulse width limited by maximum junction temperature.

### Ordering & Marking Information:

Device Name: EMF14N02VAT for EDFN 2 x 2



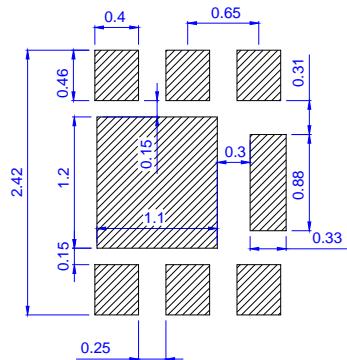
### Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	e	F	f	K1	K2	L	K3	K4	K5
Min.	0.5	0	0.25		1.9	0.9	0.13	1.9	1.1	0.65	0.55			0.28	0.05	0.2	0.01	0.27	0.07
Typ.		0.02	0.3	0.1	2	1.1	0.25	2	1.2	0.75	0.65	0.15	45°	0.38	0.15	0.25	0.11	0.37	0.17
Max.	0.65	0.05	0.35		2.1	1.2	0.35	2.1	1.3	0.88	0.75			0.48	0.25	0.3	0.21	0.47	0.27

### Recommended minimum pads





## TYPICAL CHARACTERISTICS

