杰力科技股份有限公司
Excelliance MOS Corporation

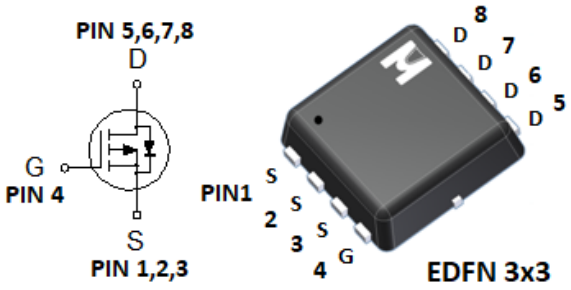
EMDA0P10V

Single P-Channel Logic Level Enhancement Mode Field Effect Transistor

▪Product Summary:

	P-CH
BV_{DSS}	-100 V
$R_{DSON\ (MAX.)}$@V_{GS}= -10V	132 mΩ
I_D @T_C=25°C	-13 A
I_D @T_A=25°C	-3 A

▪ Pin Description:



Single P Channel MOSFET
UIS, Rg 100% Tested
RoHS & Halogen Free & TSCA Compliant

▪ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current	T_C = 25 °C	I_D	-13	A
	T_C = 100 °C		-8	
Continuous Drain Current	T_A = 25 °C	I_D	-3	
	T_A = 70 °C		-2	
Pulsed Drain Current[1]		I_{DM}	-38	
Avalanche Current		I_{AS}	-20	
Avalanche Energy	L = 0.1mH	EAS	20	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	EAR	10	
Power Dissipation	T_C = 25 °C	P_D	46.3	W
	T_C = 100 °C		18.5	
Power Dissipation	T_A = 25 °C	P_D	3.6	W
	T_A = 70 °C		2.3	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

▪ 100% UIS testing in condition of VD=80V, L=0.1mH, VG=10V, IL= 12A, Rated VDS=100V P-CH

▪THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case		$R_{\theta JC}$		2.7	°C/W
Junction-to-Ambient[3]	t≦10s	$R_{\theta JA}$		35	
	Steady-State	$R_{\theta JA}$		60	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≦ 1%

[3]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C.

[4]Guarantee by Engineering test.

▪ ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage[4]	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-100			V
Gate Threshold Voltage[4]	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-2.5	-4.0	
Gate-Body Leakage[4]	I_{GSS}	V_{DS} = 0V, V_{GS} = ±25V			±100	nA
Zero Gate Voltage Drain Current[4]	I_{DSS}	V_{DS} = -80V, V_{GS} = 0V			-1	μA
		V_{DS} = -70V, V_{GS} =0V, T_J = 125 °C			-25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -10V	-13			A
Drain-Source On-State Resistance[1,4]	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -3.5A		105	132	mΩ
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -3.5A		25		S
DYNAMIC						
Input Capacitance[5]	C_{iss}	V_{GS} = 0V, V_{DS} = -50V, f = 1MHz		3551		pF
Output Capacitance[5]	C_{oss}			80		
Reverse Transfer Capacitance[5]	C_{rss}			56		
Gate Resistance[4,5]	R_g	f = 1MHz		4.4		Ω
Total Gate Charge[1,2,5]	Q_g	V_{DS} = -50V, V_{GS} = -10V, I_D = -3.5A		73		nC
Gate-Source Charge[1,2,5]	Q_{gs}			15		
Gate-Drain Charge[1,2,5]	Q_{gd}			16		
Turn-On Delay Time[1,2,5]	$t_{d(on)}$	V_{DS} = -50V, V_{GS} = -10V, I_D = -5A , Rg = 6Ω		11.7		nS
Rise Time[1,2,5]	t_r			16.6		
Turn-Off Delay Time[1,2,5]	$t_{d(off)}$			119.7		
Fall Time[1,2,5]	t_f			27.9		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				-13	A
Pulsed Current[3]	I_{SM}				-38	
Forward Voltage[1,4]	V_{SD}	I_F = I_S, V_{GS} = 0V			-1.2	V
Reverse Recovery Time[5]	t_{rr}	I_F = -3.5A , dI_F/dt = 100A / μS		50.6		nS
Reverse Recovery Charge[5]	Q_{rr}			125.5		nC
Peak Reverse Recovery Current[5]	$I_{RM(REC)}$			6.9		A
Reverse Recovery Fall Time[5]	Ta			47.3		nS
Reverse Recovery Rise Time[5]	Tb			3.4		nS

[1]Pulse test : Pulse Width ≦ 300 usec, Duty Cycle ≦ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

[4]Guarantee by FT test Item

[5]Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪TYPICAL CHARACTERISTICS

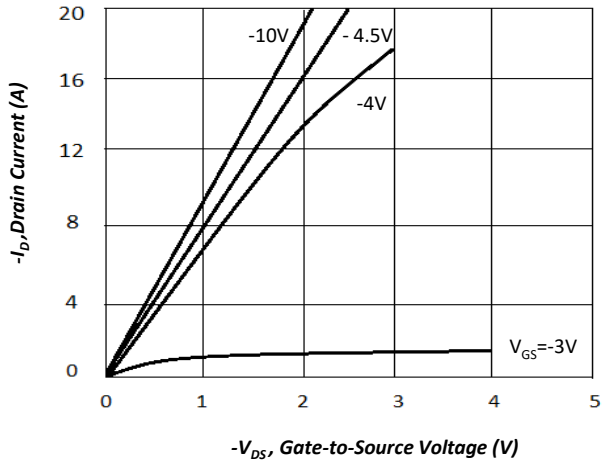


Fig.1 Typical Output Characteristics

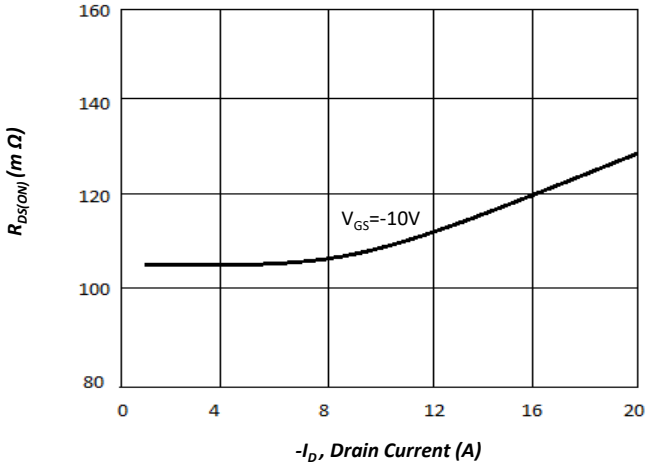


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

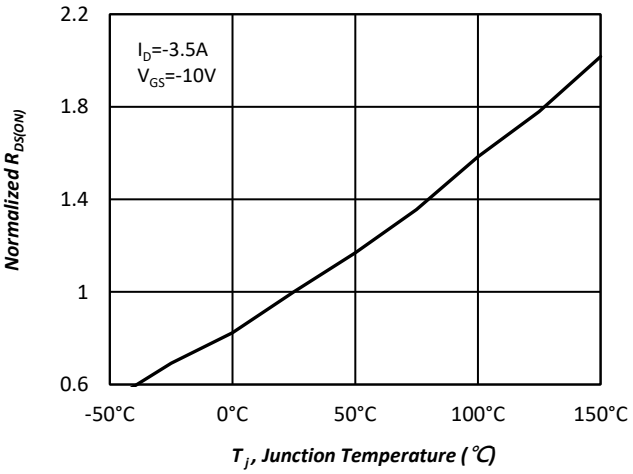


Fig.3 Normalized On-Resistance v.s. Junction Temperature

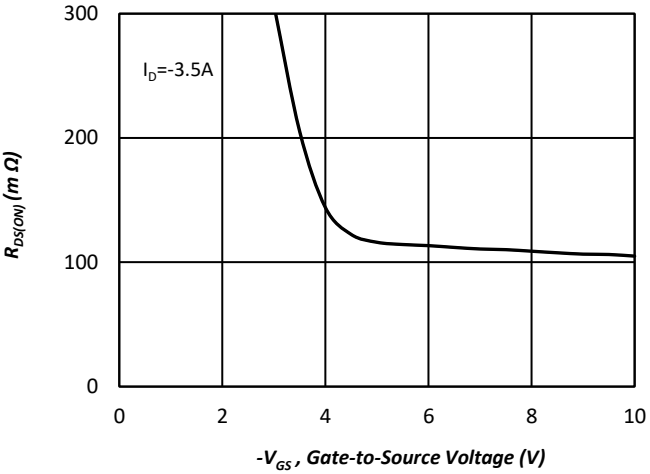


Fig.4 On-Resistance v.s. Gate Voltage

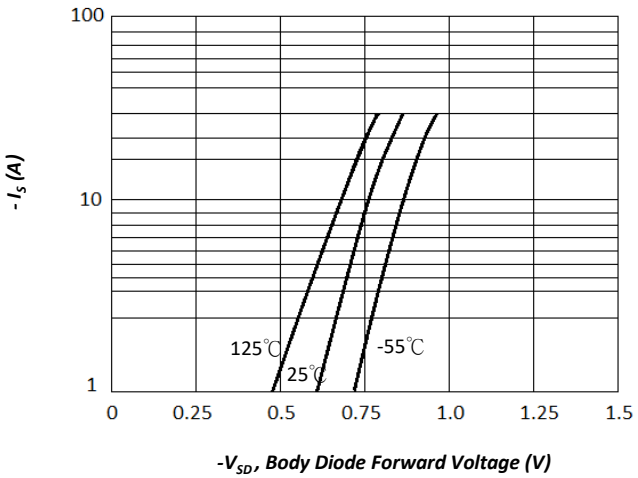


Fig.5 Forward Characteristic of Reverse Diode

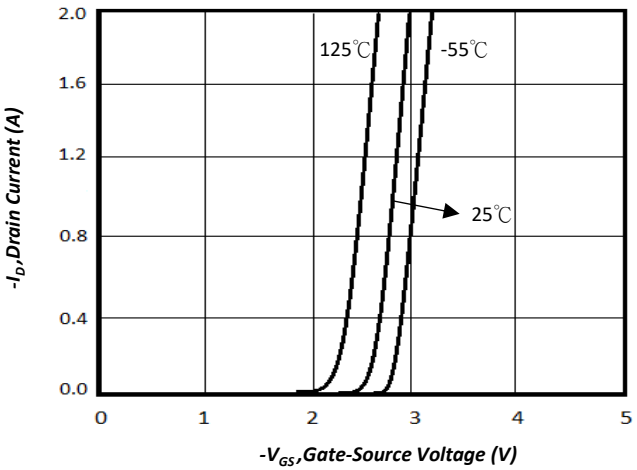


Fig.6 Transfer Characteristics

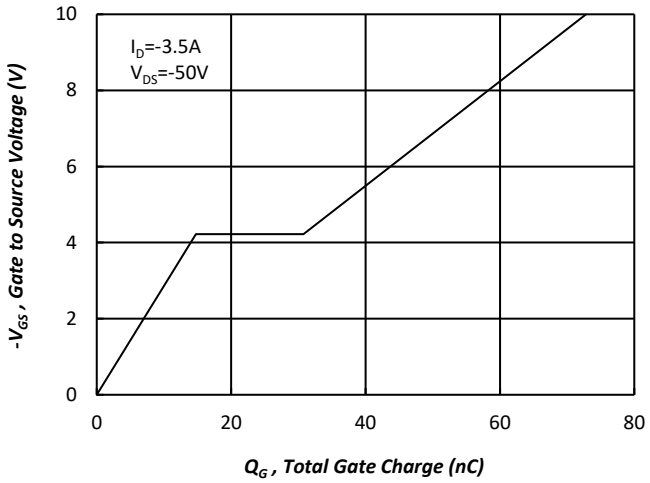


Fig.7 Gate Charge Characteristics

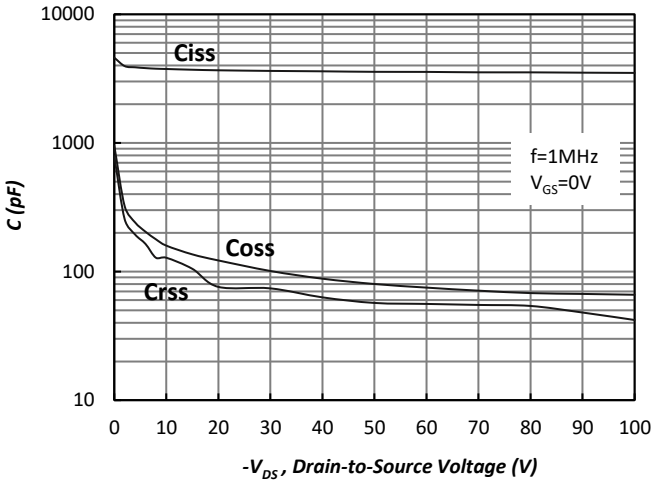


Fig.8 Typical Capacitance Characteristics

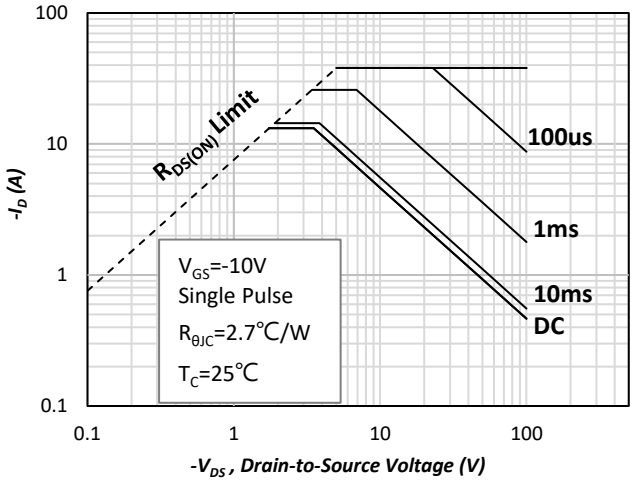


Fig 9. Maximum Safe Operating Area

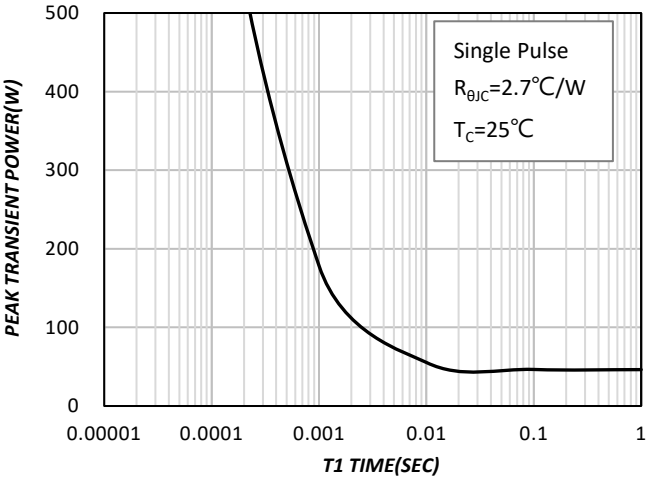


Fig 10. Single Pulse Maximum Power Dissipation

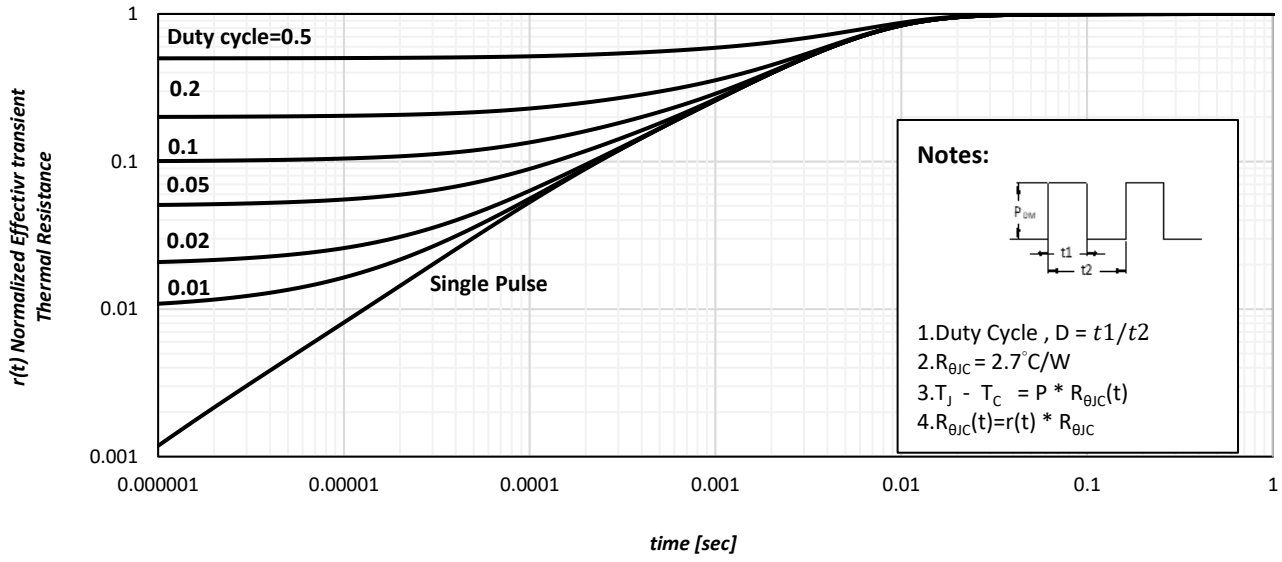


Fig 11. Effective Transient Thermal Impedance

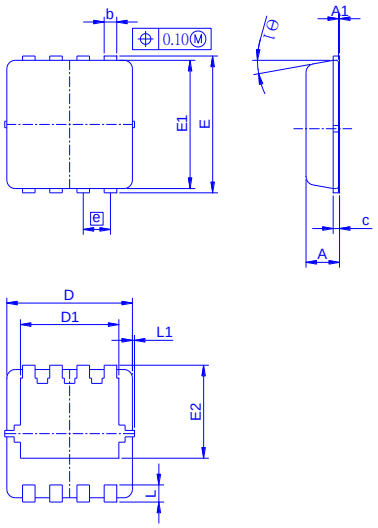
Ordering & Marking Information:

Device Name:EMDA0P10V for EDFN3X3

DA0P10: Device Name

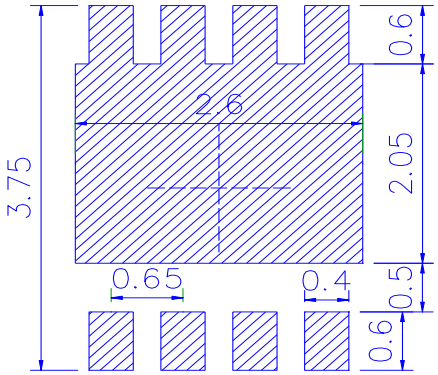
ABCDEFG: Date Code
A: Assembly House
B: Year(A:2008 B:2009 C:2010….)
C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)
DEFG: Serial No.

Outline Drawing

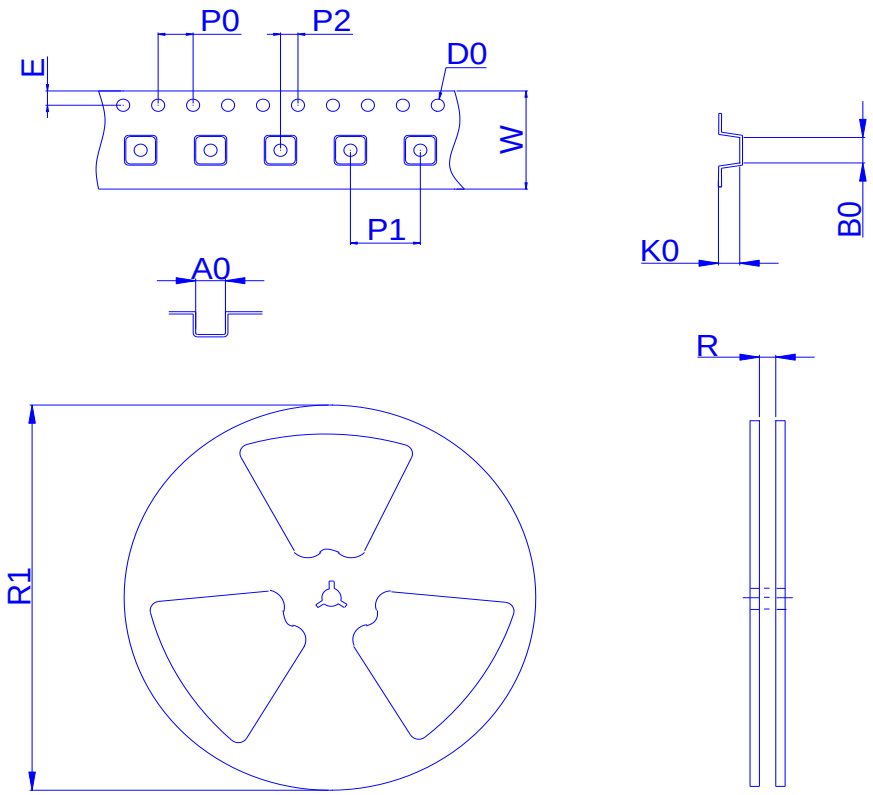


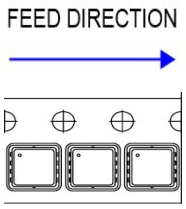
Dimension	A	A1	b	c	D	D1	E	E1	E2	e	L	L1	Θ1
Min.	0.65	0	0.2	0.1	2.9	2.15	3.1	2.9	1.53	0.55	0.25	-	0°
Typ.	0.75	-	0.3	0.15	3	2.45	3.2	3	1.97	0.65	0.4	0.075	10°
Max.	0.9	0.05	0.4	0.25	3.3	2.74	3.5	3.3	2.59	0.75	0.6	0.15	14°

Footprint



◆ **Tape&Reel Information:5000pcs/Reel**



Package	EDFN3X3
Reel	13”
Device orientation	

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	3.6	3.6	1.55	1.7	1.2	4	8	2	12	12.4	330
±	0.3	0.3	0.2	0.2	0.2	0.1	0.1	0.1	1	2	2