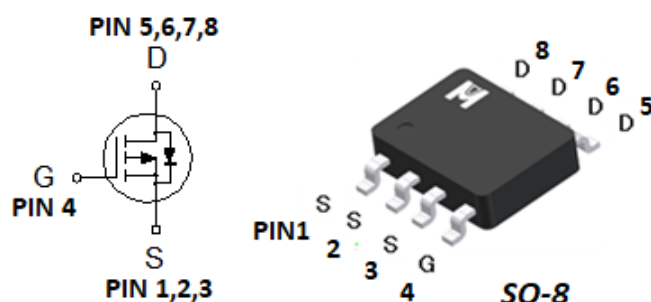


P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	P-CH
BV_{DSS}	-100V
$R_{DS(on)} (MAX.) @ V_{GS}=10V$	120m Ω
$I_D @ T_A=25^{\circ}C$	-3.4A



Single P Channel MOSFET

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_A = 25^{\circ}C$	I_D	-3.4	A
	$T_A = 70^{\circ}C$		-2.7	
Pulsed Drain Current ¹		I_{DM}	-13.6	
Power Dissipation	$T_A = 25^{\circ}C$	P_D	2.5	W
	$T_A = 70^{\circ}C$		1.6	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	$^{\circ}C$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	$^{\circ}C / W$
Junction-to-Ambient ³	$R_{\theta JA}$		50	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³50 $^{\circ}C / W$ when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-2.0	-3.0	-4.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -80V, V_{GS} = 0V$			-1	μA
		$V_{DS} = -70V, V_{GS} = 0V, T_J = 125\text{ }^{\circ}C$			-10	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = -5V, V_{GS} = -10V$	-3.4			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = -10V, I_D = -3.4A$		105	120	m Ω
Forward Transconductance ¹	g_{fs}	$V_{DS} = -5V, I_D = -3.4A$		8		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -25V, f = 1MHz$		3520		pF
Output Capacitance	C_{oss}			132		
Reverse Transfer Capacitance	C_{rss}			115		
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		5.5		Ω
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = -80V, V_{GS} = 10V,$ $I_D = -3.4A$		59		nC
Gate-Source Charge ^{1,2}	Q_{gs}			14		
Gate-Drain Charge ^{1,2}	Q_{gd}			11		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = -15V,$ $I_D = -1A, V_{GS} = -10V, R_{GS} = 6\Omega$		15		nS
Rise Time ^{1,2}	t_r			45		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			50		
Fall Time ^{1,2}	t_f			50		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)						
Continuous Current	I_S				-2.3	A
Pulsed Current ³	I_{SM}				-9.2	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			-1.3	V
Reverse Recovery Time	t_{rr}	$I_F = I_S, dI_F/dt = 100A / \mu S$		150		nS
Reverse Recovery Charge	Q_{rr}			830		nC

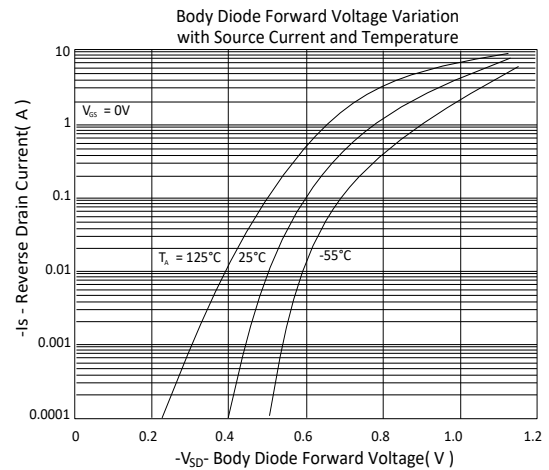
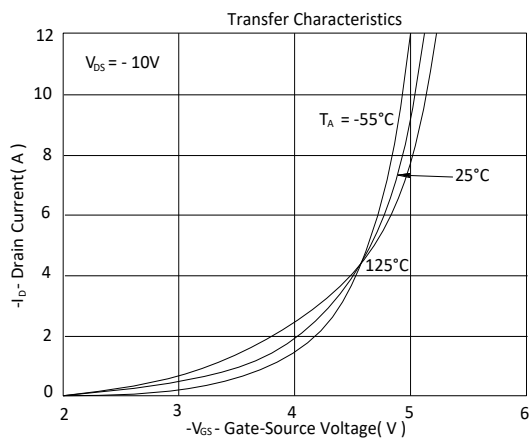
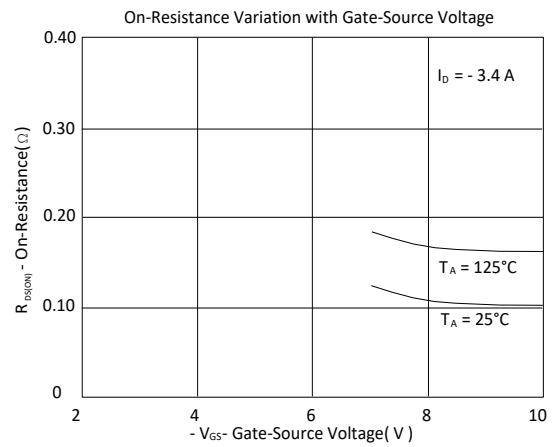
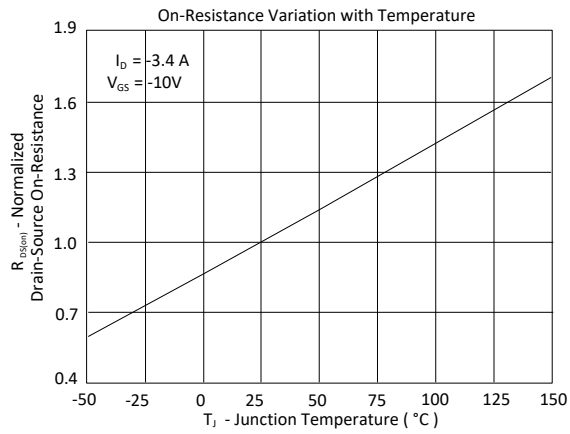
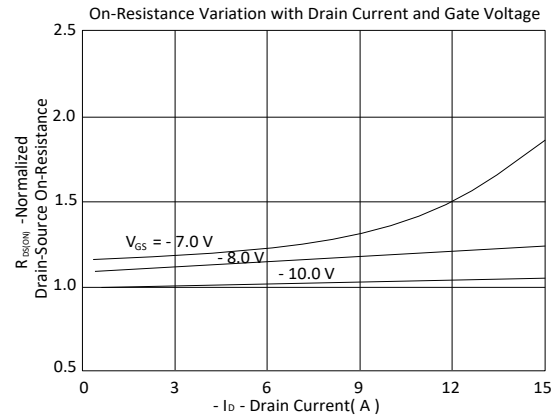
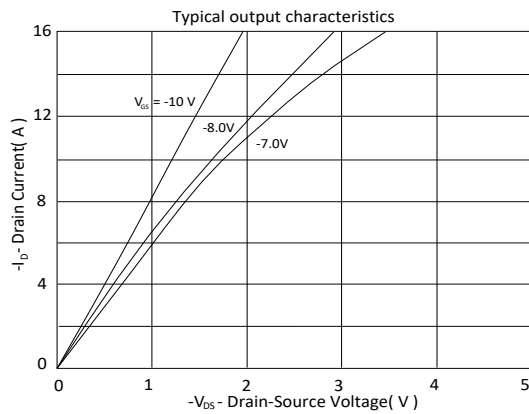


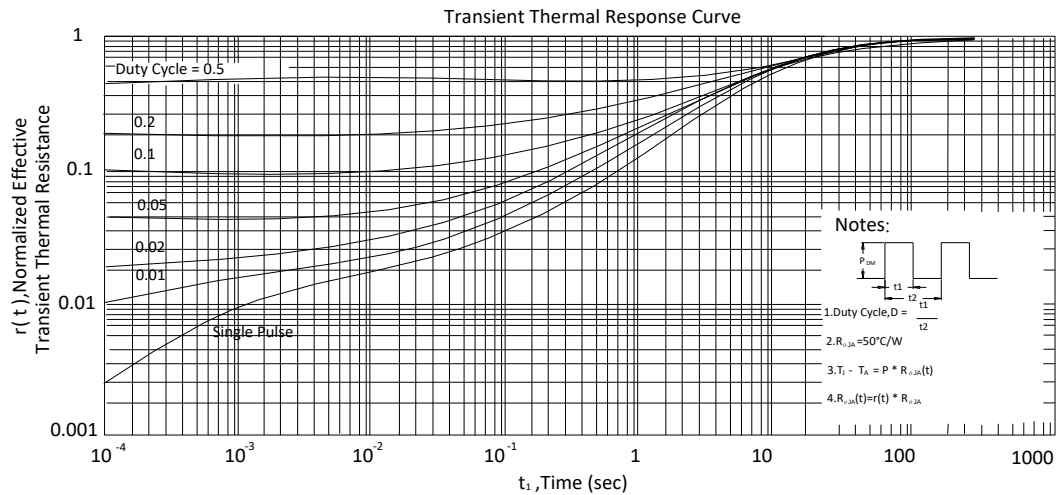
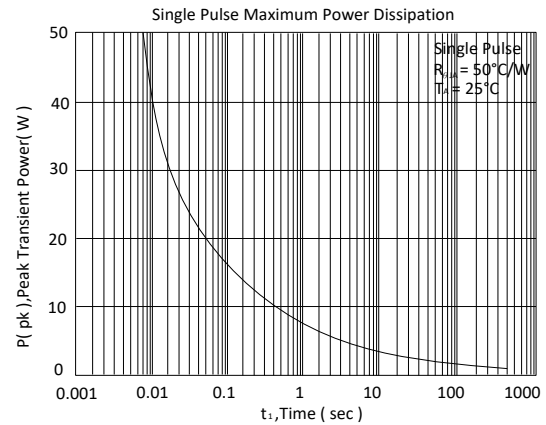
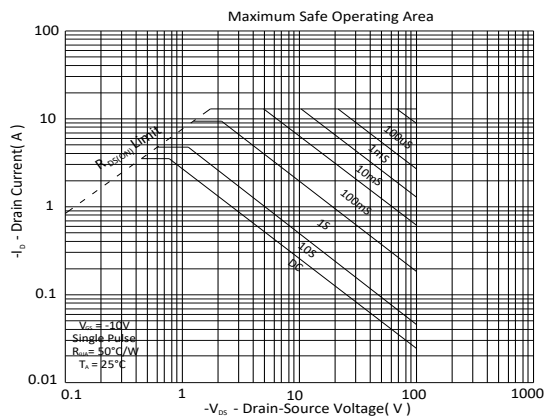
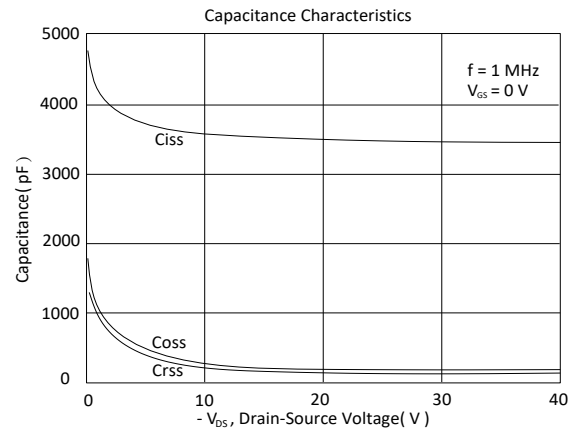
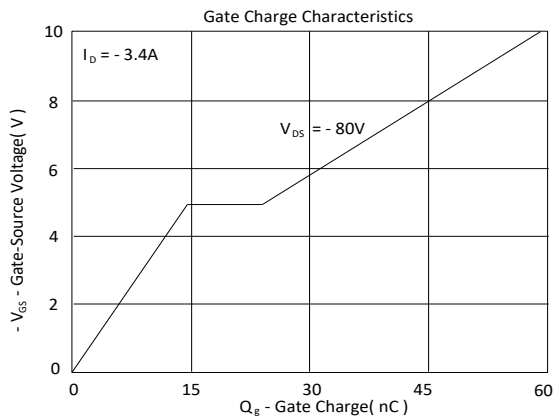
¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

EMC will review datasheet by quarter, and update new version.





Ordering & Marking Information:

Device Name: EMDA0P10G for SO-8



DA0P10: Device Name

ABCDEFG: Date Code

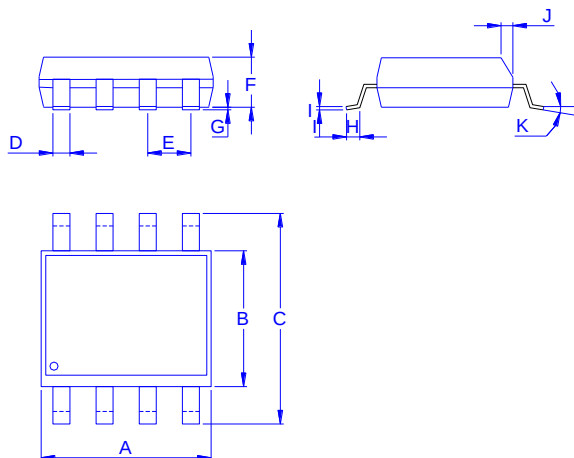
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

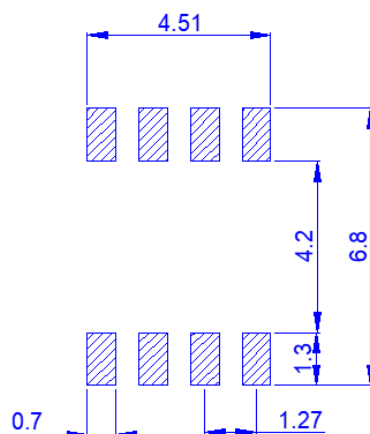
Outline Drawing



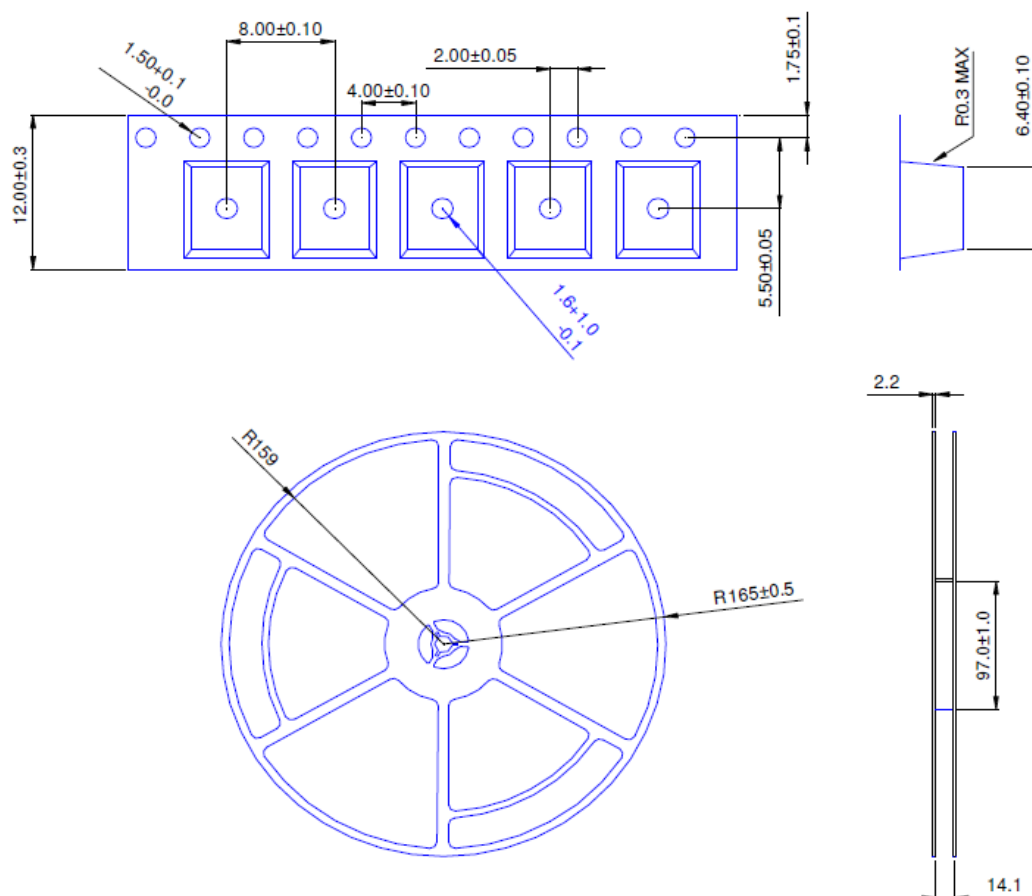
Dimension in mm

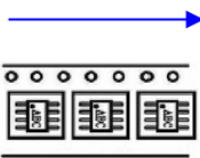
Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.80	5.80	0.31		1.35	0.01	0.40	0.10	0.25	0°
Typ.	4.90	3.90	6.00	0.41	1.27	1.55	0.18	0.60	0.20	0.30	
Max.	5.10	4.00	6.20	0.51		1.75	0.25	1.27	0.25	0.50	8°

Footprint:



◆ Tape&Reel Information:5000pcs/Reel (Dimension in millimeter)



產品別	SOP-8
Reel 尺寸	13"
編帶方式	FEED DIRECTION 
前空格	25
後空格	50
裝箱數	
滿捲數量	2.5K
捲/內盒比	1 : 1
內盒滿箱數	2.5K
內/外箱比	10 : 1
外箱滿箱數	25K