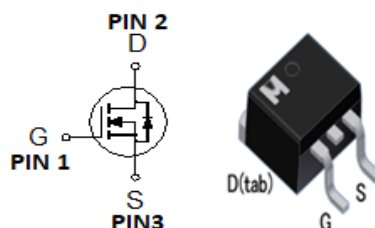


Single N-Channel Logic Level Enhancement Mode Field Effect Transistor
•Product Summary:

	N-CH
BV_{DSS}	100V
$R_{DS(on) (MAX.)}@V_{GS}=10V$	4.5m Ω
$R_{DS(on) (MAX.)}@V_{GS}=7V$	6.0m Ω
$I_D @T_C=25^{\circ}C$	145A
$I_D @T_A=25^{\circ}C$	20A

• Pin Description:

TO-263-2

Single N Channel MOSFET

UIS, Rg 100% Tested

RoHS & Halogen Free & TSCA Compliant


•ABSOLUTE MAXIMUM RATINGS ($T_C = 25^{\circ}C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^{\circ}C$	I_D	145	A
	$T_C = 100^{\circ}C$		92	
Continuous Drain Current	$T_A = 25^{\circ}C$	I_D	20	
	$T_A = 70^{\circ}C$		16	
Pulsed Drain Current ¹		I_{DM}	545	
Avalanche Current		I_{AS}	116	
Avalanche Energy	$L = 0.1mH$	EAS	672.8	mJ
Repetitive Avalanche Energy ²	$L = 0.05mH$	EAR	336.4	
Power Dissipation	$T_C = 25^{\circ}C$	P_D	178.6	W
	$T_C = 100^{\circ}C$		71.4	
Power Dissipation	$T_A = 25^{\circ}C$	P_D	3.4	W
	$T_A = 70^{\circ}C$		2.2	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	$^{\circ}C$

 • 100% UIS testing in condition of $V_D=50V$, $L=0.1mH$, $V_G=10V$, $I_L=70A$, Rated $V_{DS}=100V$ N-CH

•THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case		$R_{\theta JC}$		0.7	$^{\circ}C/W$
Junction-to-Ambient ^{3,4}	$t \leq 10s$	$R_{\theta JA}$		20.8	
	Steady-State	$R_{\theta JA}$		37	

¹Pulse width limited by maximum junction temperature.

²Duty cycle < 1%

³37 $^{\circ}C$ / W when mounted on a 1 in² pad of 2 oz copper.

⁴Guarantee by Engineering test

•ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	100			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	2	3	4	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 80V, V _{GS} = 0V			1	μA
		V _{DS} =70V, V _{GS} =0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	145			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A		3.5	4.5	mΩ
		V _{GS} = 7V, I _D = 20A		4.0	6.0	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 20A		90		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 50V, f = 1MHz		5853		pF
Output Capacitance ⁵	C _{oss}			1109		
Reverse Transfer Capacitance ⁵	C _{rss}			73		
Gate Resistance ^{4,5}	R _g	f = 1MHz		0.7		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 50V, V _{GS} = 10V, I _D = 20A		88		nC
	Q _g (V _{GS} =7V)			64		
Gate-Source Charge ^{1,2,5}	Q _{gs}			29		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			18		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 50V, V _{GS} = 10V, I _D = 5A , R _g = 6Ω		26		nS
Rise Time ^{1,2,5}	t _r			28.6		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			68.2		
Fall Time ^{1,2,5}	t _f			67.8		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				145	A
Pulsed Current ³	I _{SM}				545	
Forward Voltage ^{1,4}	V _{SD}	I _F = 30A, V _{GS} = 0V			1.2	V
Reverse Recovery Time ⁵	t _{rr}	I _F = 30A, dI _F /dt = 100A / μS		94		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			-2.94		A
Reverse Recovery Charge ⁵	Q _{rr}			156		nC

¹ Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

² Independent of operating temperature.

³ Pulse width limited by maximum junction temperature.

⁴ Guarantee by FT test Item

⁵ Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪ TYPICAL CHARACTERISTICS

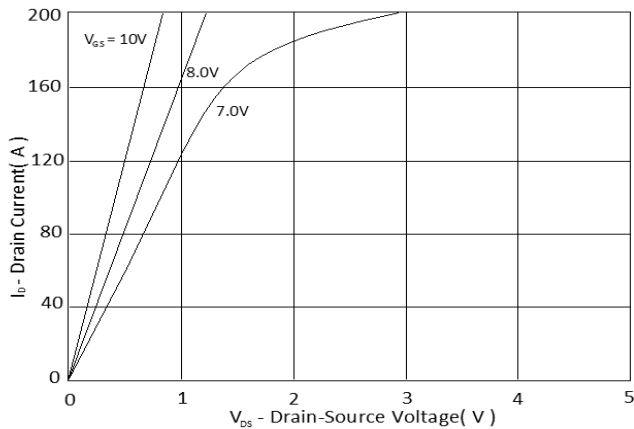


Fig.1 Typical Output Characteristics

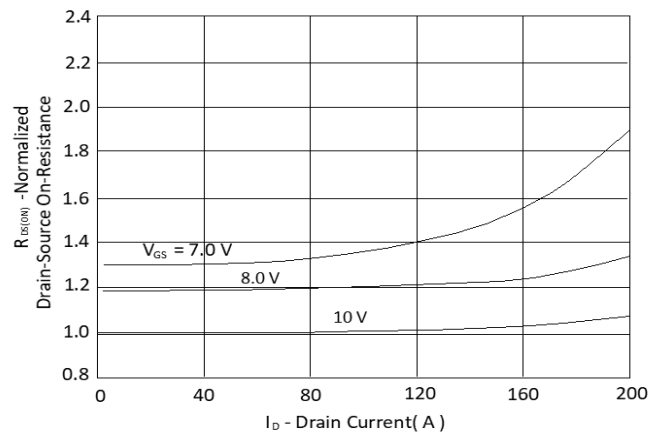


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

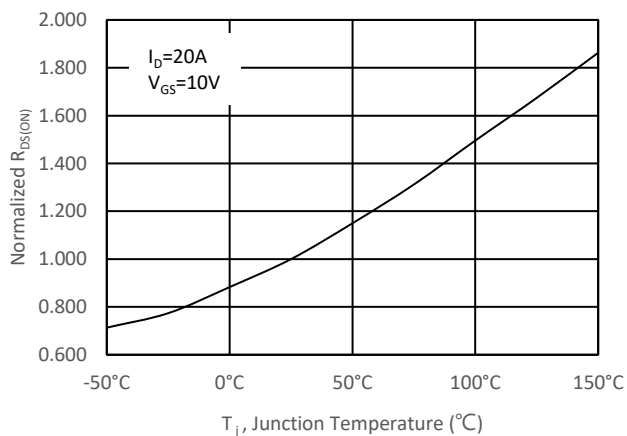


Fig.3 Normalized On-Resistance v.s. Junction Temperature

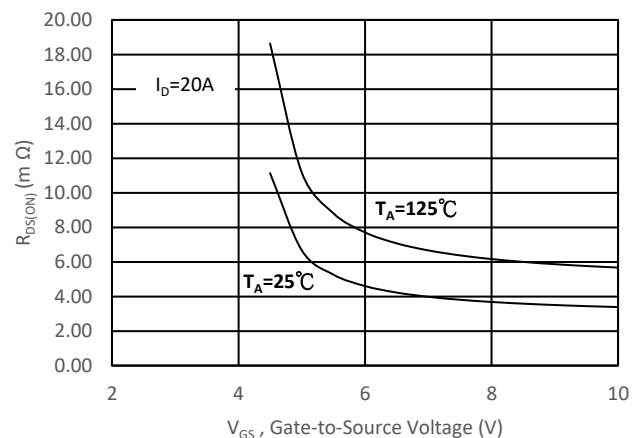


Fig.4 On-Resistance v.s. Gate Voltage

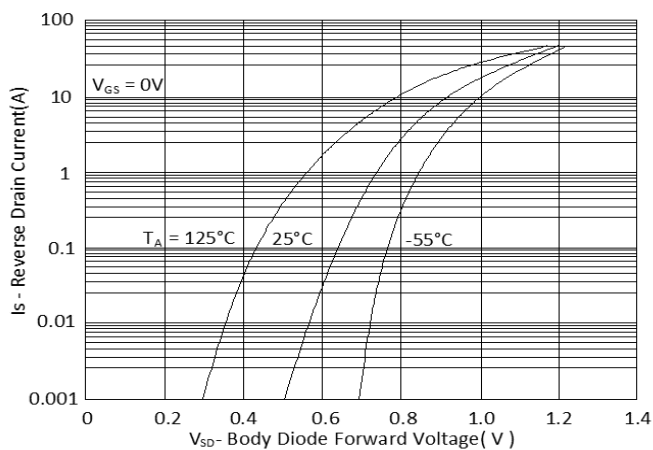


Fig.5 Forward Characteristic of Reverse Diode

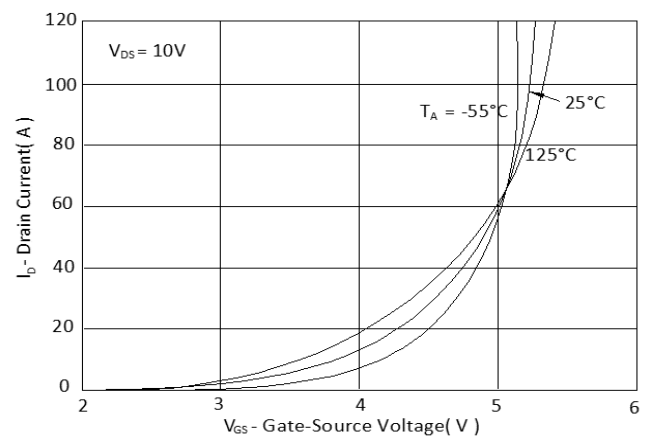


Fig.6 Transfer Characteristics

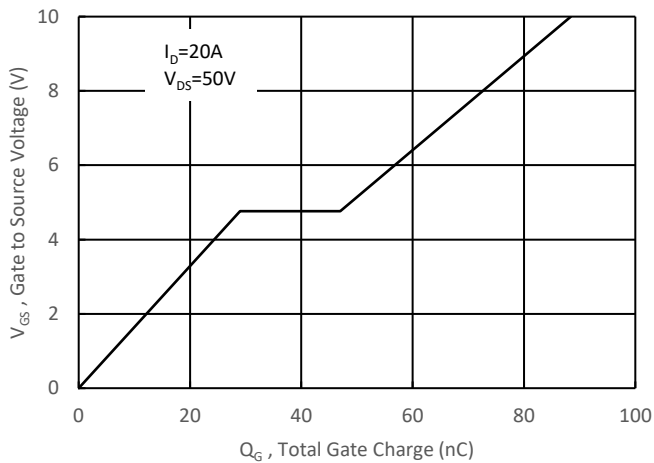


Fig.7 Gate Charge Characteristics

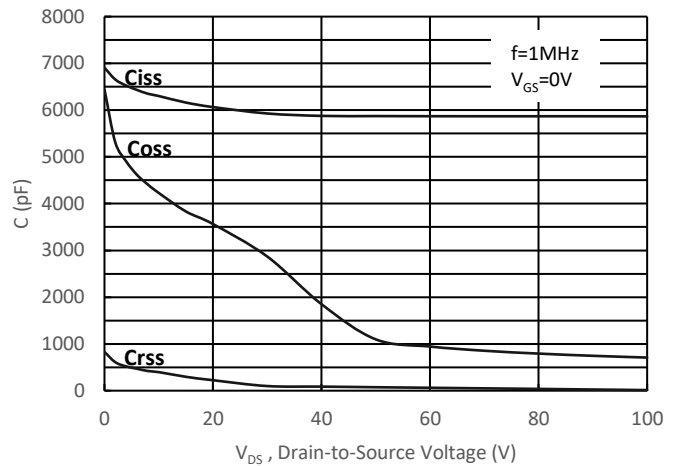


Fig.8 Typical Capacitance Characteristics

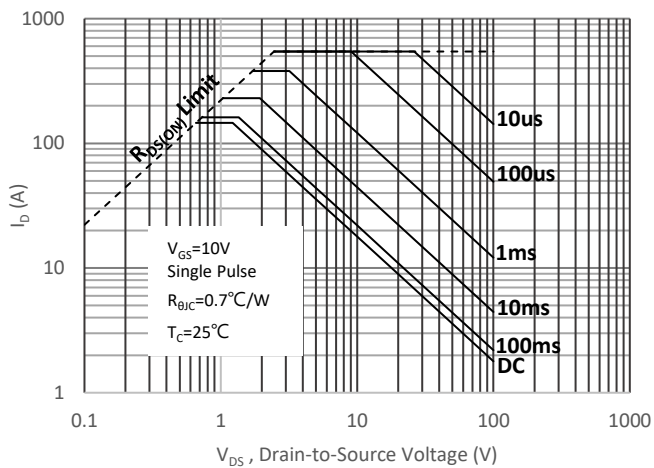


Fig.9. Maximum Safe Operating Area

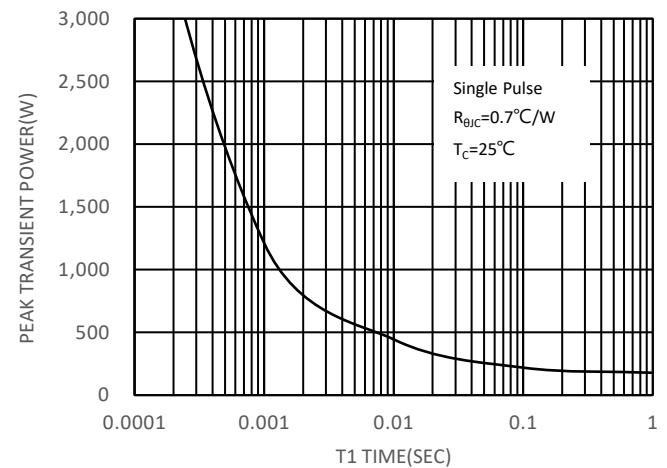


Fig.10. Single Pulse Maximum Power Dissipation

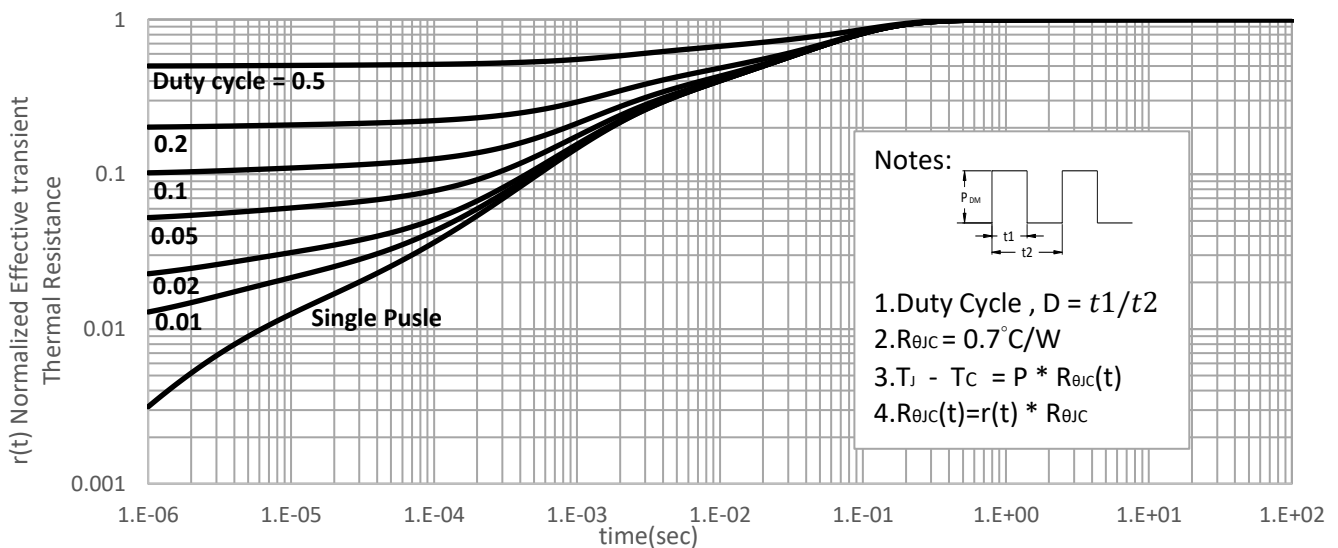
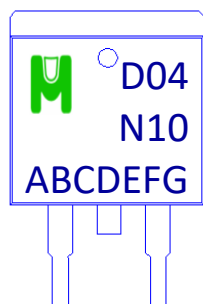


Fig.11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMD04N10B for TO-263-2



D04N10: Device Name

ABCDEFG: Date Code

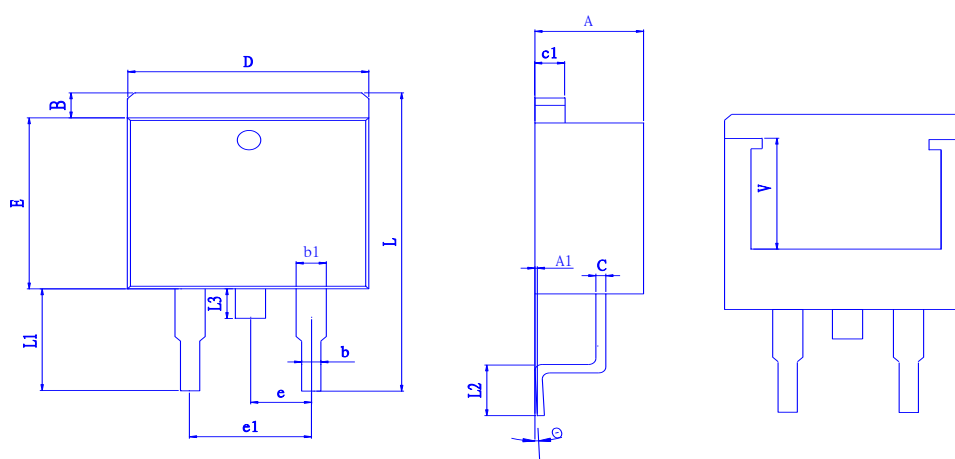
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

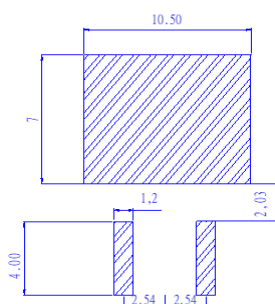
Outline Drawing



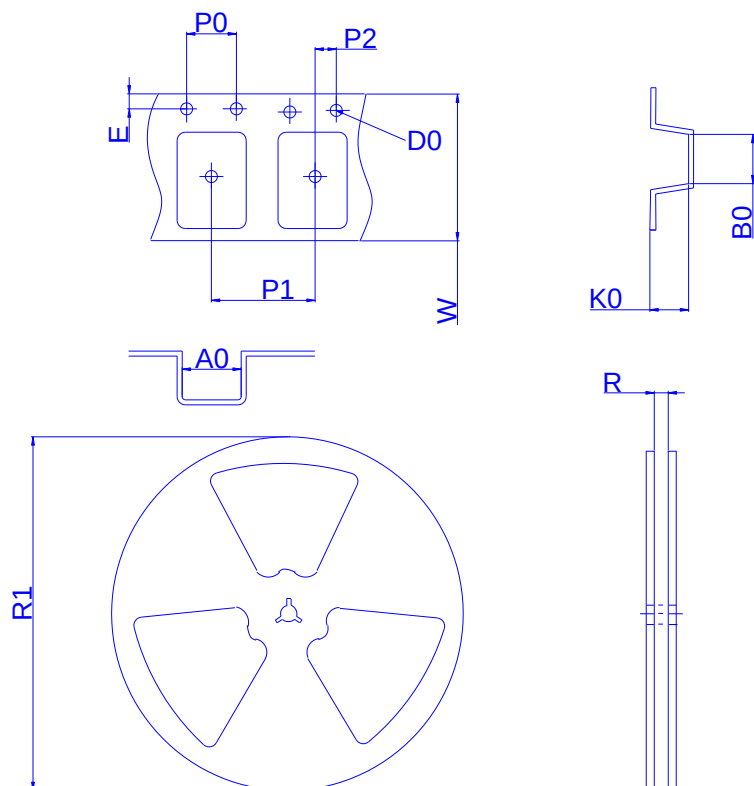
Dimension	A	A1	B	b	b1	c	c1	D	E	e	e1	L	L1
Min.	4.24	0	1.12	0.7	1.17	0.31	1.15	9.96	8.5	0	4.98	14.61	4.95
Typ.	4.44	0.1	1.27	0.8	1.45	0.5	1.27	10.16	8.92	2.54	0	15	0
Max.	4.7	0.25	1.42	0.91	1.7	0.6	1.4	10.36	9.25	0	5.18	15.88	5.45

Dimension	L2	L3	Θ	V
Min	1.78	1.3	0	6.86
Typ.	2.3	1.5	0	5.6
Max	2.79	1.75	8°	0

Footprint



◆ Tape&Reel Information:800pcs/Reel



產品別	TO-263-2
Reel尺寸	13"
編帶方式	FEED DIRECTION →

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	10.8	16.30	1.5	1.75	4.70	4	16	2	24	2.44	330
±	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.3	2	2