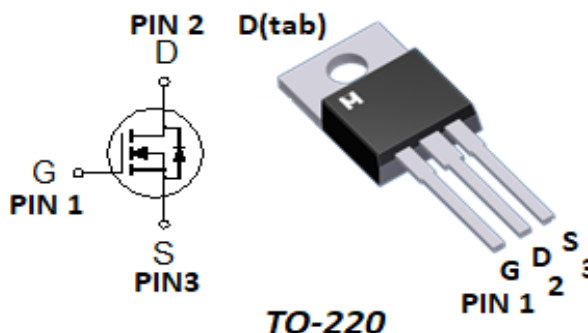


Single N-Channel Logic Level Enhancement Mode Field Effect Transistor

•Product Summary:

	N-CH
BV_{DSS}	100V
$R_{DS(on) (Max.)}@V_{GS}=10V$	3.0mΩ
$R_{DS(on) (Max.)}@V_{GS}=7V$	3.5mΩ
$I_D @T_C=25^{\circ}C$	278A
$I_D @T_A=25^{\circ}C$	22A

• Pin Description:



Single N Channel MOSFET

UIS, Rg 100% Tested

RoHS & Halogen Free & TSCA Compliant



•ABSOLUTE MAXIMUM RATINGS ($T_C = 25^{\circ}C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^{\circ}C$	I_D	278	A
	$T_C = 100^{\circ}C$		176	
Continuous Drain Current	$T_A = 25^{\circ}C$	I_D	22	
	$T_A = 70^{\circ}C$		17	
Pulsed Drain Current ¹		I_{DM}	845	
Avalanche Current		I_{AS}	90	mJ
Avalanche Energy	$L = 0.1mH$	EAS	405	
Repetitive Avalanche Energy ²	$L = 0.05mH$	EAR	202.5	
Power Dissipation	$T_C = 25^{\circ}C$	P_D	357	W
	$T_C = 100^{\circ}C$		143	
Power Dissipation	$T_A = 25^{\circ}C$	P_D	2.3	W
	$T_A = 70^{\circ}C$		1.5	
Operating Junction & Storage Temperature Range		T_{jv}, T_{stg}	-55 to 150	$^{\circ}C$

• 100% UIS testing in condition of $V_D=50V$, $L=0.1mH$, $V_G=10V$, $I_L=54A$, Rated $V_{DS}=100V$ N-CH

•THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case		$R_{\theta JC}$		0.35	$^{\circ}C/W$
Junction-to-Ambient ³	$t \leq 10s$	$R_{\theta JA}$		30	
	Steady-State	$R_{\theta JA}$		55	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $< 1\%$

³The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^{\circ}C$.

⁴Guarantee by Engineering test



▪ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	100			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	2	3	4	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 80V, V _{GS} = 0V			1	μA
		V _{DS} =70V, V _{GS} =0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 5V, V _{GS} = 10V	278			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 50A		2.3	3.0	mΩ
		V _{GS} =7V, I _D = 20A		2.6	3.5	
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 50V, f = 1MHz		9043		pF
Output Capacitance ⁵	C _{oss}			1702		
Reverse Transfer Capacitance ⁵	C _{rss}			99		
Gate Resistance ^{4,5}	R _g	f = 1MHz		0.9		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 50V, V _{GS} = 10V, I _D = 50A		141		nC
	Q _g (V _{GS} =7V)			104		
Gate-Source Charge ^{1,2,5}	Q _{gs}			43		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			37		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 50V, V _{GS} = 10V, I _D = 5A , R _g = 6Ω		34		nS
Rise Time ^{1,2,5}	t _r			44		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			117		
Fall Time ^{1,2,5}	t _f			114		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				278	A
Pulsed Current ³	I _{SM}				845	
Forward Voltage ^{1,4}	V _{SD}	I _F = 50A, V _{GS} = 0V			1.3	V
Reverse Recovery Time ⁵	t _{rr}	I _F = 50A, dI _F /dt = 100A / μS		133		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			3.68		A
Reverse Recovery Charge ⁵	Q _{rr}			296		nC

¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.



•TYPICAL CHARACTERISTICS

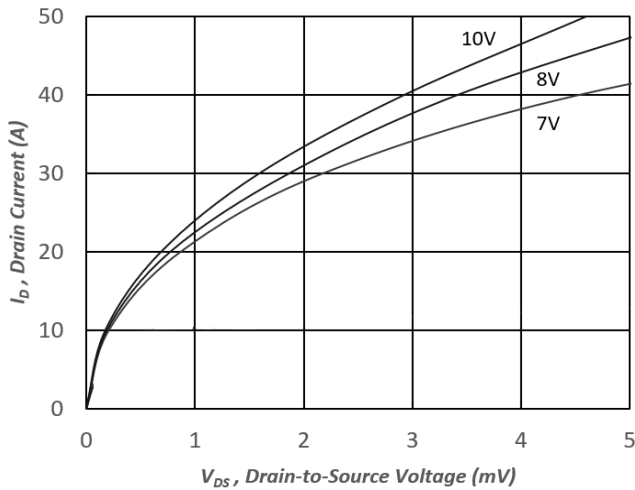


Fig.1 Typical Output Characteristics

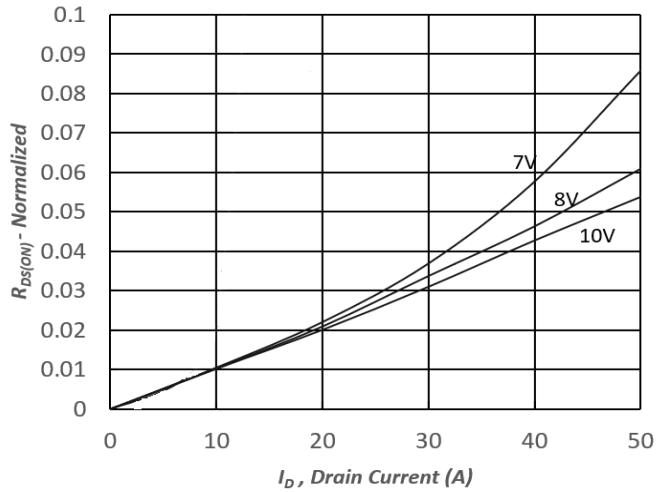


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

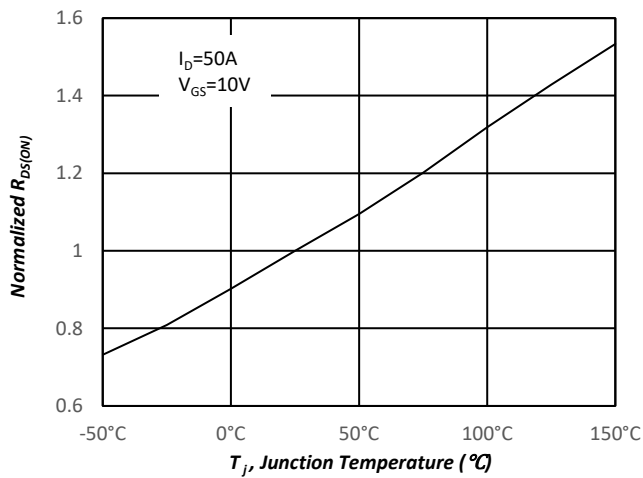


Fig.3 Normalized On-Resistance v.s. Junction Temperature

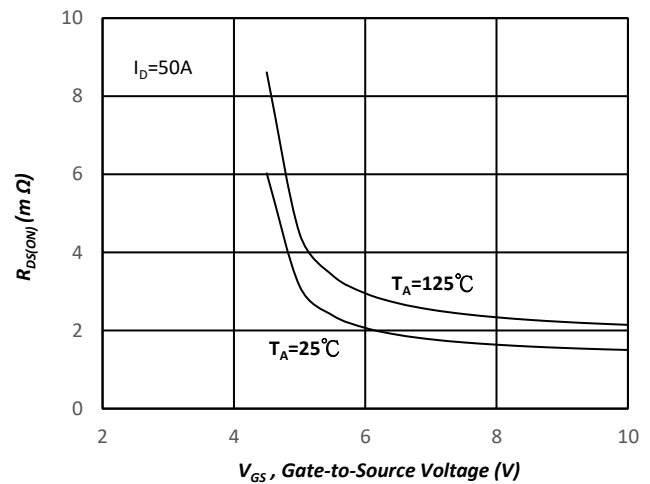


Fig.4 On-Resistance v.s. Gate Voltage

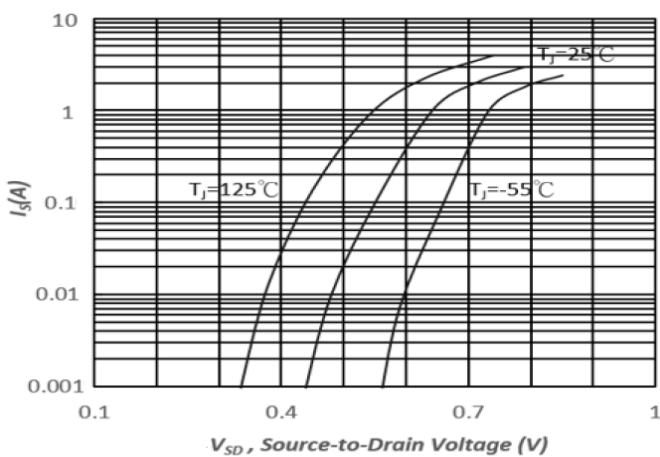


Fig.5 Forward Characteristic of Reverse Diode

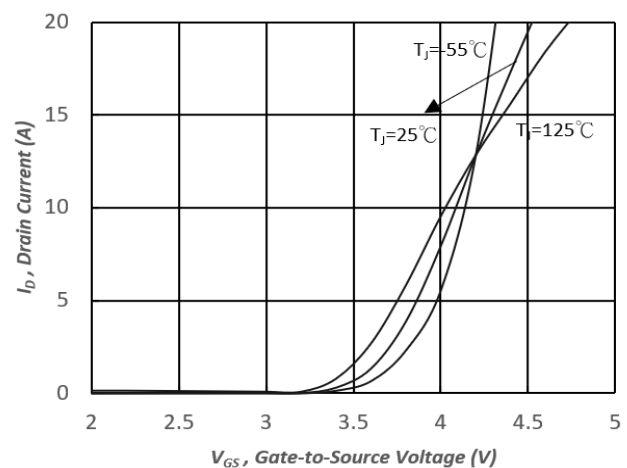


Fig.6 Transfer Characteristics

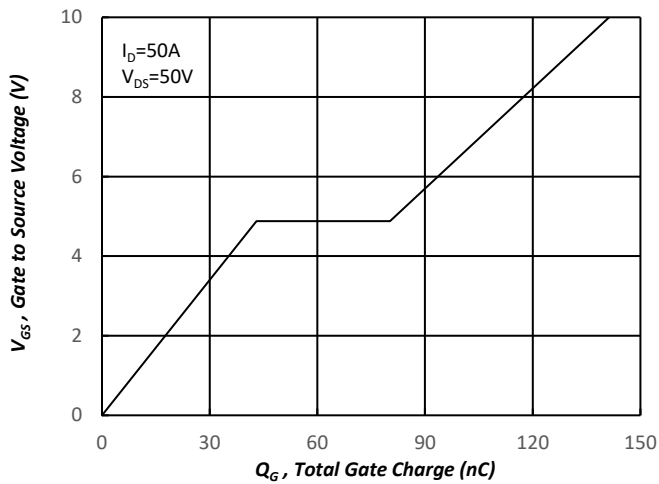


Fig.7 Gate Charge Characteristics

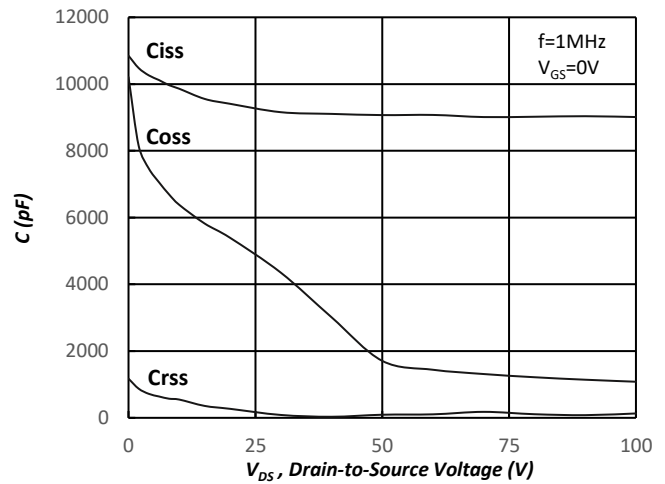


Fig.8 Typical Capacitance Characteristics

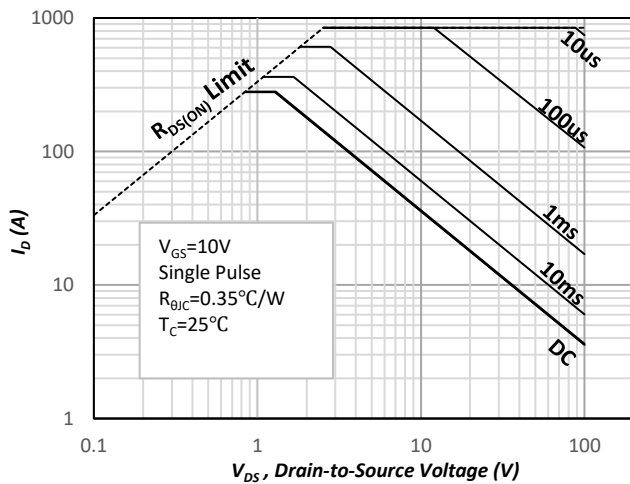


Fig.9. Maximum Safe Operating Area

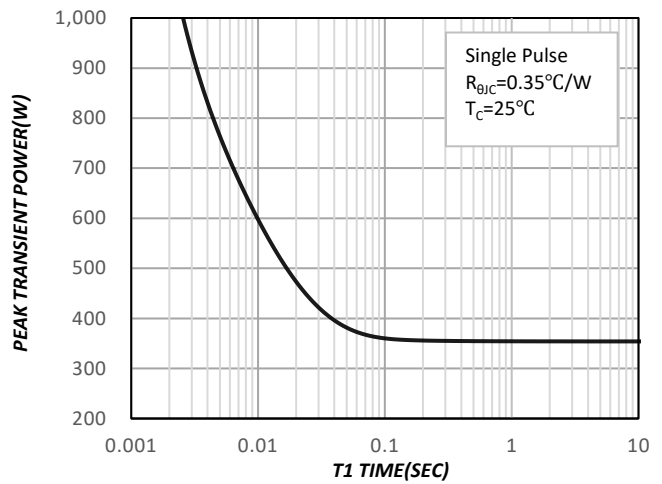


Fig.10. Single Pulse Maximum Power Dissipation

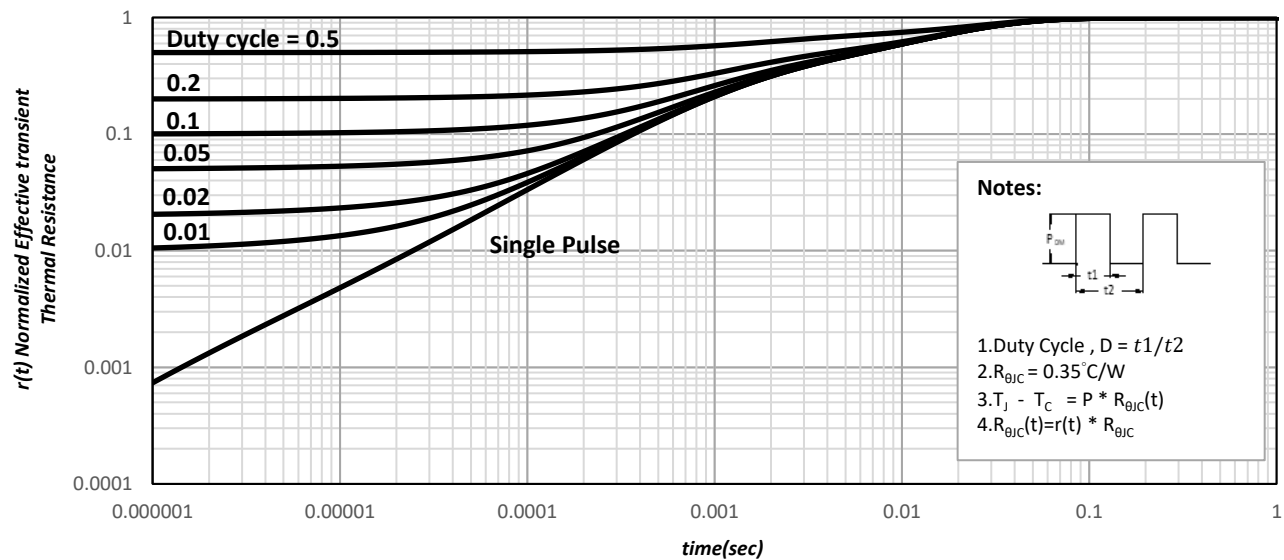
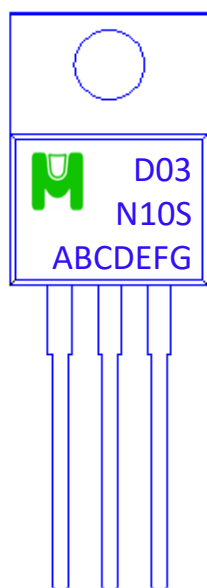


Fig.11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMD03N10ES for TO-220



D03N10S: Device Name

ABCDEFG: Date Code

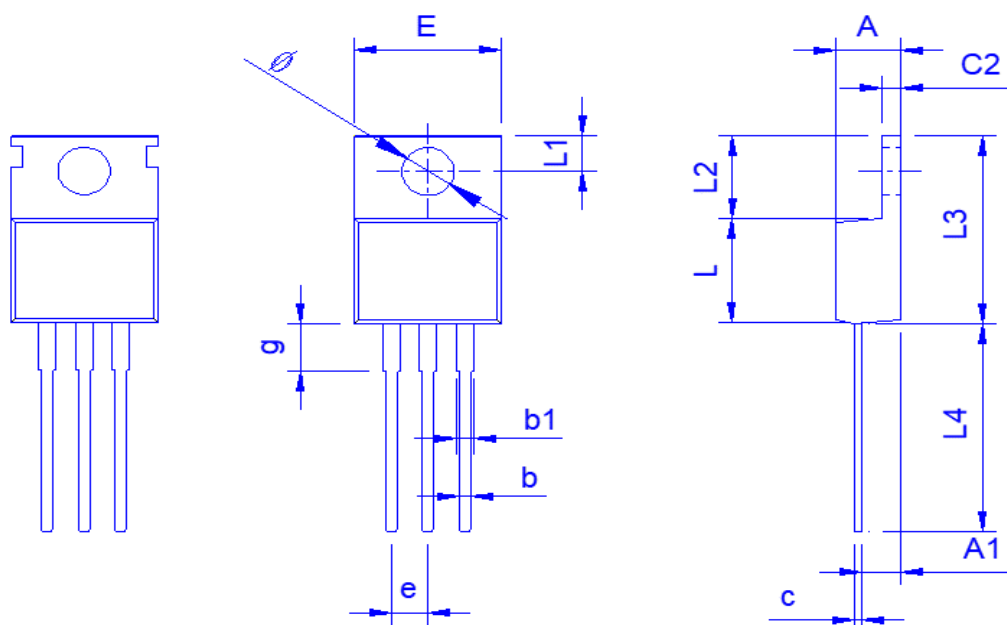
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

Outline Drawing



Dimension in mm

Dimension	A	A1	b	b1	c	c2	E	L	L1	L2	L3	L4	Ø	e	g
Min.	4.240	2.250	0.700	1.170	0.310	1.150	9.910	8.500	2.590	6.100	14.700	12.700	3.400	2.440	2.850
Typ.	4.440	2.400	0.800	1.550	0.500	1.270	10.160	8.920	2.800	6.300	15.370	13.720	3.840	2.540	3.800
Max.	4.700	2.820	0.910	1.750	0.650	1.400	10.360	9.750	3.250	6.800	16.900	13.970	3.935	2.640	4.000

◆ Tube Information: 50pcs/Tube (1000pcs/Box)

