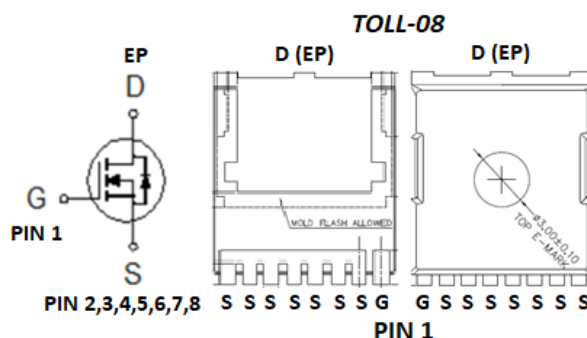


Single N-Channel Logic Level Enhancement Mode Field Effect Transistor

•Product Summary:

	N-CH
BV_{DSS}	60V
$R_{DS(on) (MAX.) @ V_{GS}=10V}$	1.9m Ω
$R_{DS(on) (MAX.) @ V_{GS}=7V}$	2.5m Ω
$I_D @ T_C=25^{\circ}C$	270A

• Pin Description:



Single N Channel MOSFET

UIS, Rg 100% Tested

RoHS Compliant & Halogen Free & TSCA Compliant



• ABSOLUTE MAXIMUM RATINGS ($T_C = 25^{\circ}C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ¹	$T_C = 25^{\circ}C$	I_D	270	A
	$T_C = 100^{\circ}C$		170	
	$T_A = 25^{\circ}C$		33	
	$T_A = 70^{\circ}C$		26	
Pulsed Drain Current ¹		I_{DM}	645	mJ
Avalanche Current ¹		I_{AS}	119	
Avalanche Energy ¹		E_{AS}	708	
Repetitive Avalanche Energy ²		E_{AR}	354	W
Power Dissipation ¹	$T_C = 25^{\circ}C$	P_D	208.3	
	$T_C = 100^{\circ}C$		83.3	W
Power Dissipation ¹	$T_A = 25^{\circ}C$	P_D	3.1	
	$T_A = 70^{\circ}C$		2	$^{\circ}C$
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	

• 100% UIS testing in condition of $V_D=30V$, $L=0.1mH$, $V_G=10V$, $I_L=72A$, Rated $V_{DS}=60V$ N-CH

•THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		0.6	$^{\circ}C / W$
Junction-to-Ambient ³	$R_{\theta JA}$		40	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³40 $^{\circ}C / W$ when mounted on a 1 in² pad of 2 oz copper.

⁴Guarantee by Engineering test

▪ ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	60			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	2	3	4	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			400	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 48V, V _{GS} = 0V			1	μA
		V _{DS} = 48V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 5V, V _{GS} = 10V	270			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 50A		1.3	1.9	mΩ
		V _{GS} =7V, I _D = 20A		1.9	2.5	
DYNAMIC						
Input Capacitance	C _{iSS}	V _{GS} = 0V, V _{DS} = 30V, f = 1MHz		7038		pF
Output Capacitance	C _{oSS}			1340		
Reverse Transfer Capacitance	C _{rSS}			50		
Gate Resistance	R _g	f = 1MHz		0.9		Ω
Total Gate Charge ^{1,2}	Q _g	V _{DS} = 30V, V _{GS} = 10V, I _D = 50A		133.1		nC
Gate-Source Charge ^{1,2}	Q _{gS}			26.8		
Gate-Drain Charge ^{1,2}	Q _{gd}			42.1		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = 30V, V _{GS} = 10V, I _D = 3A , R _g = 6Ω		27.6		nS
Rise Time ^{1,2}	t _r			29.6		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			125.3		
Fall Time ^{1,2}	t _f			80		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				270	A
Pulsed Current ³	I _{SM}				645	
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			1.3	V
Reverse Recovery Time	t _{rr}	I _F = I _S =60A, dI _F /dt = 100A / μS		64.9		nS
Peak Reverse Recovery Current	I _{RM(REC)}			2.0		A
Reverse Recovery Charge	Q _{rr}			74		nC

¹ Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

² Independent of operating temperature.

³ Pulse width limited by maximum junction temperature.

⁴ Guarantee by FT test Item

⁵ Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.



■ TYPICAL CHARACTERISTICS

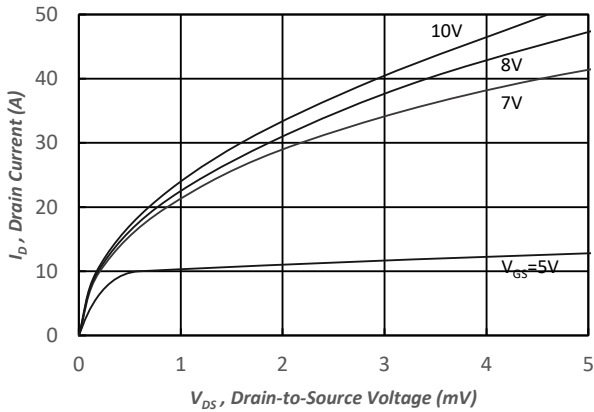


Fig.1 Typical Output Characteristics

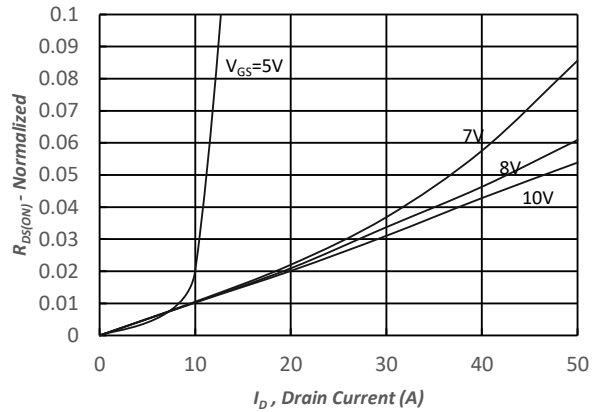


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

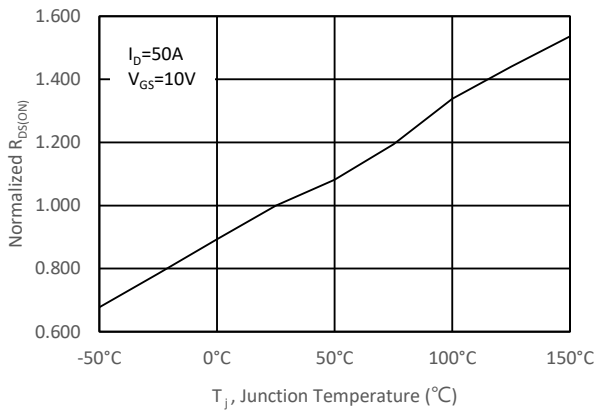


Fig.3 Normalized On-Resistance v.s. Junction Temperature

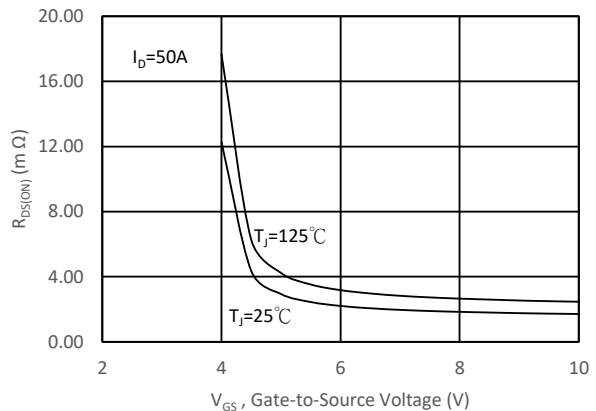


Fig.4 On-Resistance v.s. Gate Voltage

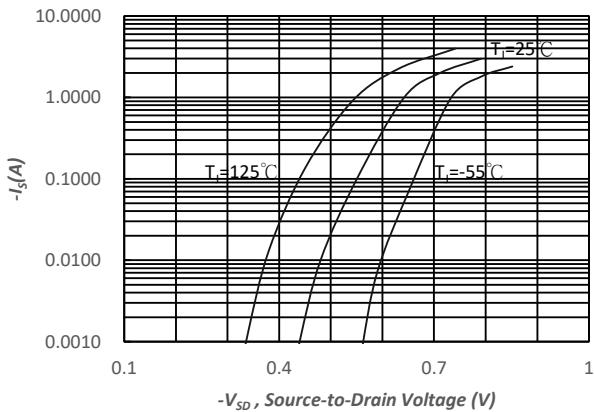


Fig.5 Forward Characteristic of Reverse Diode

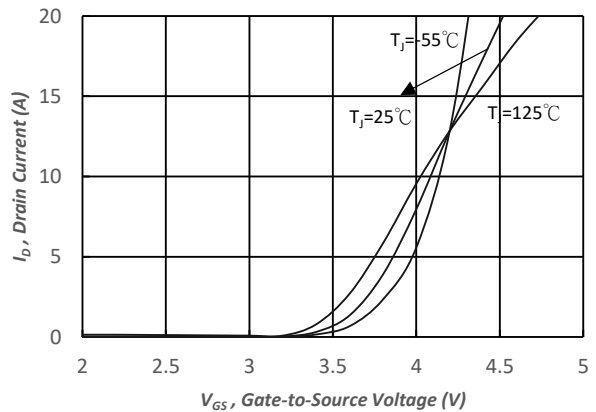


Fig.6 Transfer Characteristics

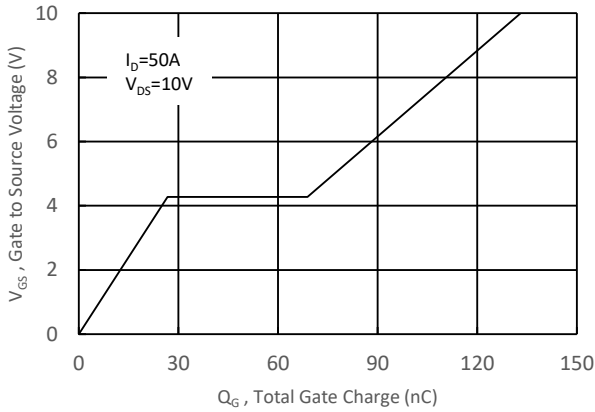


Fig.7 Gate Charge Characteristics

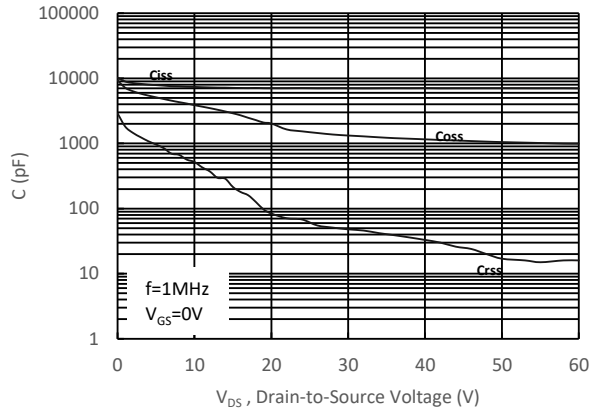


Fig.8 Typical Capacitance Characteristics

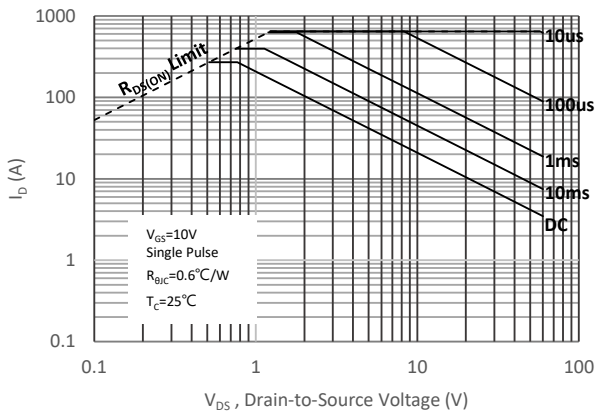


Fig.9. Maximum Safe Operating Area

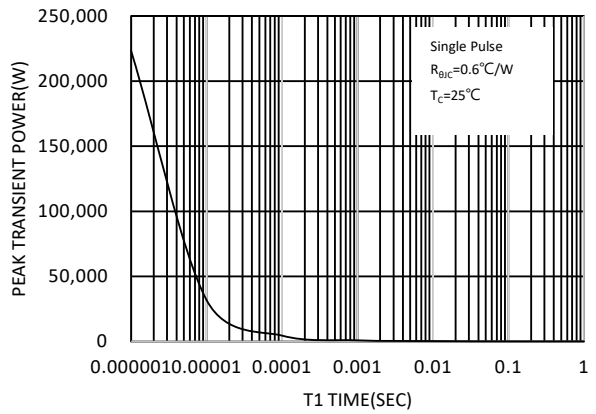


Fig.10. Single Pulse Maximum Power Dissipation

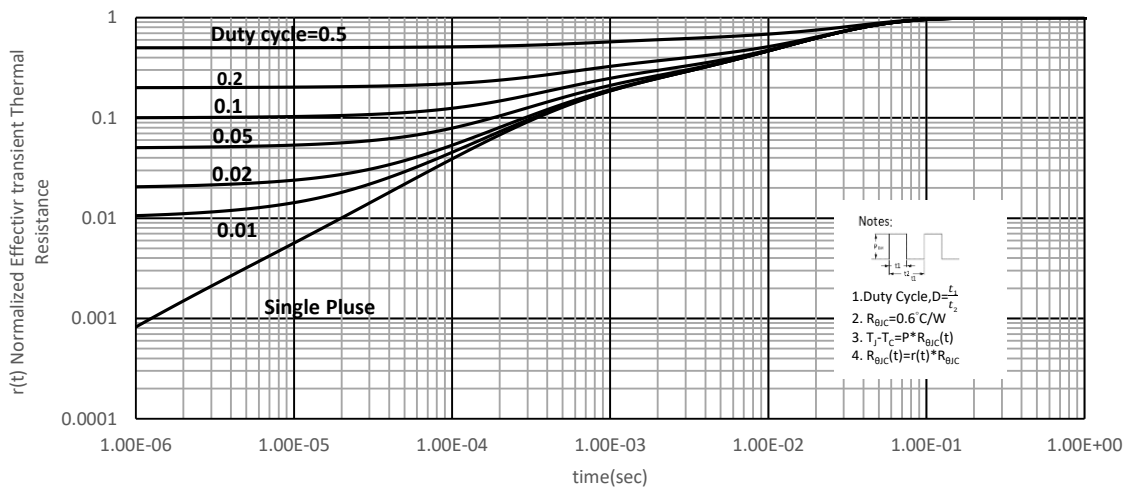
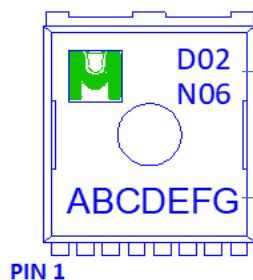


Fig.11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMD02N06TL8 for TOLL-08



D02N06: Device Name

ABCDEFGH: Date Code

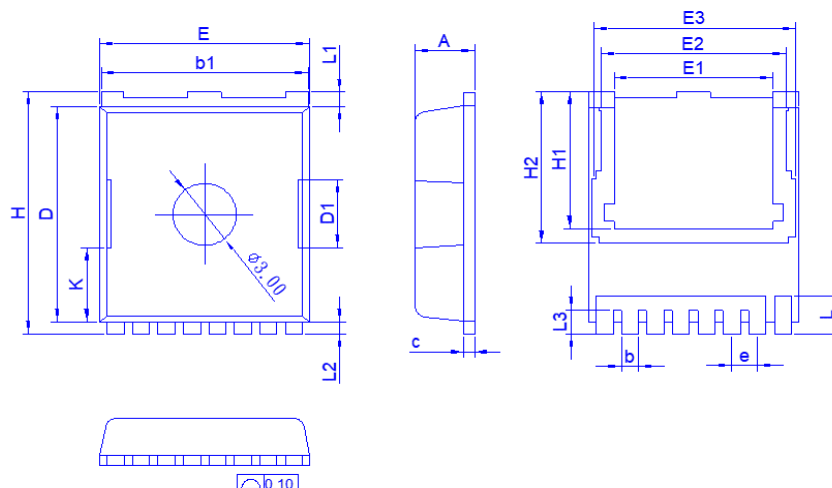
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

Outline Drawing

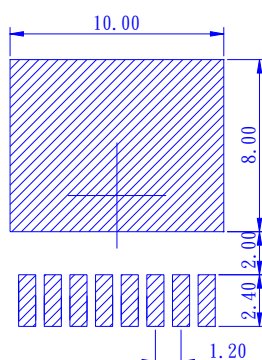


Dimension in mm

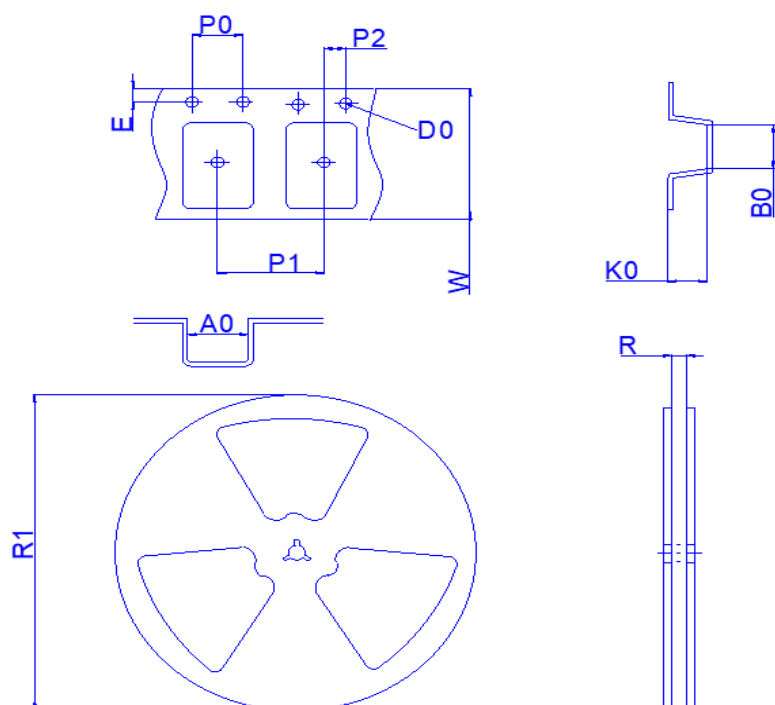
Dimension	A	b	b1	c	D	D1	E	E1	E2	E3	e	H	H1
Min	2.15	0.65	9.70	0.40	10.18	2.85	9.70	7.25	8.00	9.30	1.10	11.48	6.03
Typ.	2.30	0.75	9.80	0.50	10.38	3.00	9.90	7.40	8.10	9.40	1.20	11.68	6.18
Max	2.45	0.90	9.90	0.60	10.58	3.45	10.10	8.40	9.25	9.95	1.30	11.88	7.10

Dimension	H2	K	L	L1	L2	L3
Min	6.85	4.03	1.40	0.50	0.45	1.00
Typ.	7.00	4.18	1.70	0.70	0.60	1.15
Max	7.50	4.55	2.10	0.90	0.75	1.30

Footprint



◆ Tape&Reel Information:2000 pcs/Reel(Dimension in millimeter)



產品別	TOLL-08
Reel尺寸	13"
編帶方式	

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	10.5	12.28	1.5	1.75	2.7	4	12	2	24	24	330
±	0.2	0.2	0.1	0.1	0.2	0.1	0.2	0.1	0.3	2	2