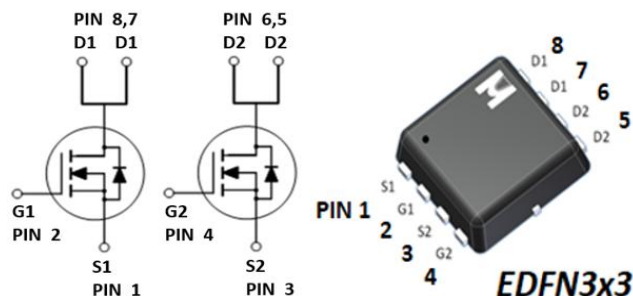


Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

•Product Summary:

	Q1	Q2
BV_{DSS}	80V	80V
$R_{DS(on)(MAX)} V_{GS}=10V$	85mΩ	85mΩ
$R_{DS(on)(MAX)} V_{GS}=4.5V$	110mΩ	110mΩ
$I_D @ T_C=25^{\circ}C$	13A	13A

• Pin Description:



Dual N Channel MOSFET

UIS, Rg 100% Tested

RoHS & Halogen Free & TSCA Compliant



• ABSOLUTE MAXIMUM RATINGS ($T_C = 25^{\circ}C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
			Q1	Q2	
Gate-Source Voltage		V_{GS}	± 20	± 20	V
Continuous Drain Current	$T_C = 25^{\circ}C$	I_D	13	13	A
	$T_C = 100^{\circ}C$		8	8	
Pulsed Drain Current ¹		I_{DM}	27	27	
Avalanche Current		I_{AS}	6	6	mJ
Avalanche Energy	$L = 0.1mH$	EAS	1.8	1.8	
Repetitive Avalanche Energy ²	$L = 0.05mH$	EAR	0.9	0.9	
Power Dissipation	$T_C = 25^{\circ}C$	P_D	31	31	W
	$T_C = 100^{\circ}C$		13	13	
Power Dissipation	$T_A = 25^{\circ}C$	P_D	2.8	2.8	W
	$T_A = 70^{\circ}C$		1.8	1.8	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		$^{\circ}C$

• 100% UIS testing in condition of $V_D=40V$, $L=0.1mH$, $V_G=10V$, $I_L=4A$, $R_G=25\Omega$, Rated $V_{DS}=80V$ N-CH_Q1

• 100% UIS testing in condition of $V_D=40V$, $L=0.1mH$, $V_G=10V$, $I_L=4A$, $R_G=25\Omega$, Rated $V_{DS}=80V$ N-CH_Q2

•THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM		UNIT
				Q1	Q2	
Junction-to-Case		$R_{\theta JC}$		4	4	$^{\circ}C/W$
Junction-to-Ambient ^{3,4}	$t \leq 10s$	$R_{\theta JA}$		44	44	
	Steady-State	$R_{\theta JA}$		87	87	

¹Pulse width limited by maximum junction temperature.

²Duty cycle < 1%

³The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}C$.

⁴Guarantee by Engineering test

▪ Q1 ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	80			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.2	1.8	2.5	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 80V, V _{GS} = 0V			1	μA
		V _{DS} =80V, V _{GS} =0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	13			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 4.5A		65	85	mΩ
		V _{GS} = 4.5V, I _D = 2.5A		76	110	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 10A		17		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 40V, f = 1MHz		338		pF
Output Capacitance ⁵	C _{oss}			39		
Reverse Transfer Capacitance ⁵	C _{rss}			19		
Gate Resistance ^{4,5}	R _g	f = 1MHz		6.0		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 40V, V _{GS} = 10V, I _D = 4.5A		7		nC
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =4.5V)			3.3		
Gate-Source Charge ^{1,2,5}	Q _{gs}			2		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			1		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 40V, V _{GS} = 10V, I _D = 4.5A , R _g = 3Ω		4.9		nS
Rise Time ^{1,2,5}	t _r			6.6		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			15		
Fall Time ^{1,2,5}	t _f			14		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				26	A
Pulsed Current ³	I _{SM}				27	
Forward Voltage ^{1,4}	V _{SD}	I _F = 4.5A, V _{GS} = 0V			1.2	V
Reverse Recovery Time ⁵	t _{rr}	I _F = 10A, dI _F /dt = 100A / μS		17		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			1.6		A
Reverse Recovery Charge ⁵	Q _{rr}			14		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

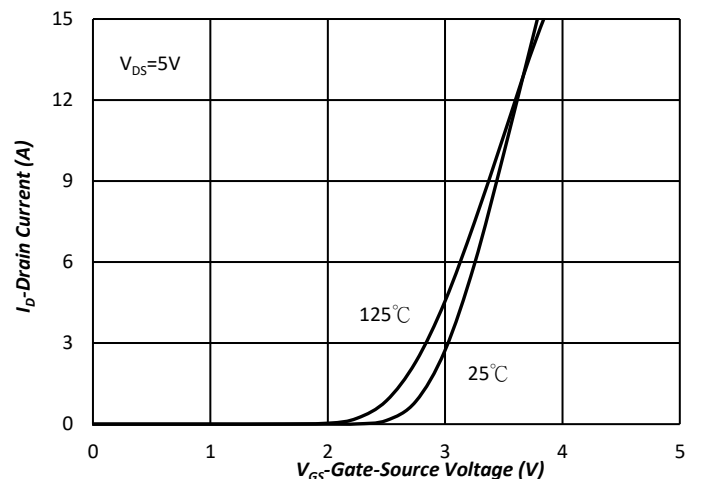
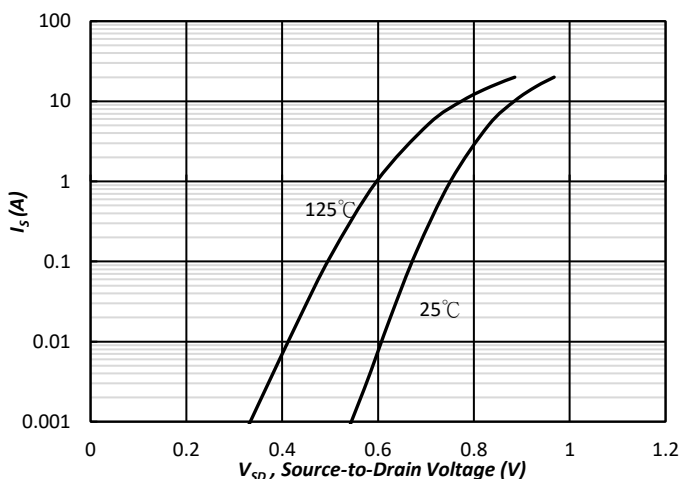
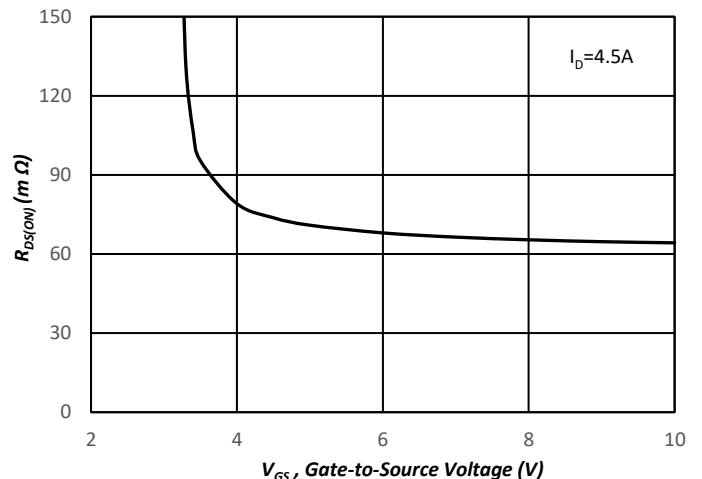
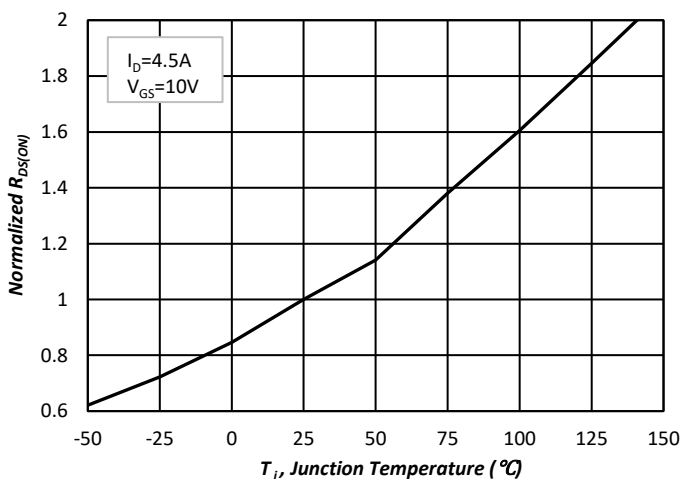
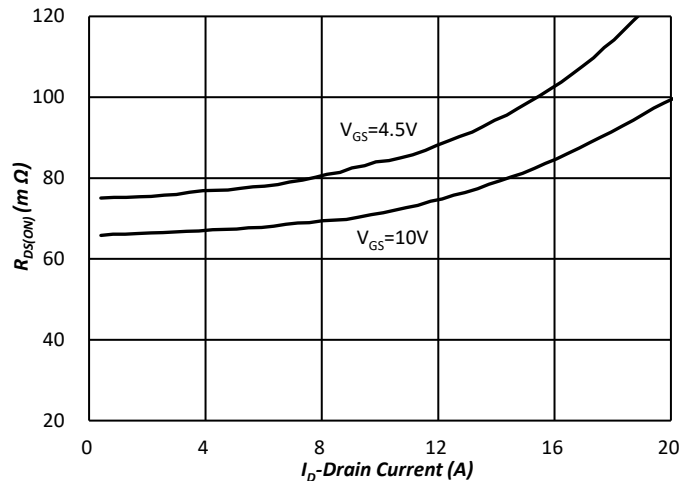
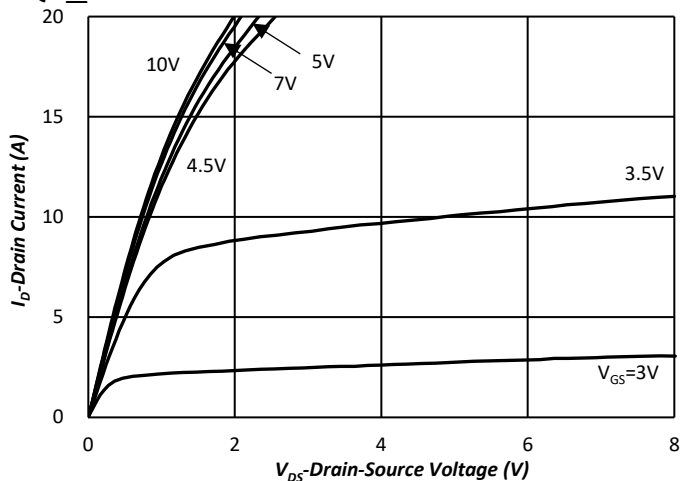
³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

Q1_TYPICAL CHARACTERISTICS



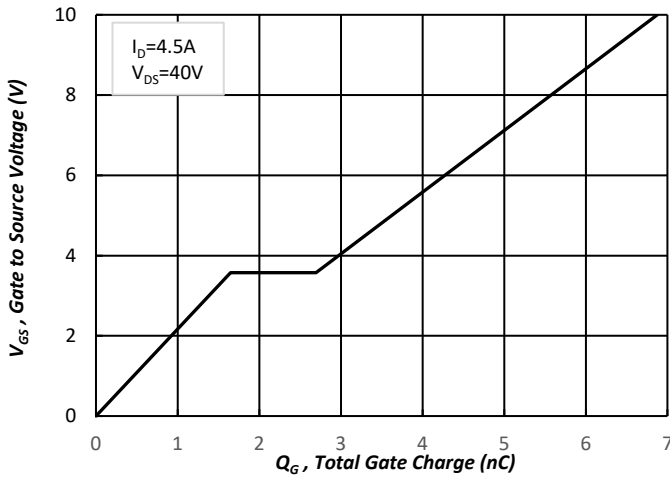


Fig.7 Gate Charge Characteristics

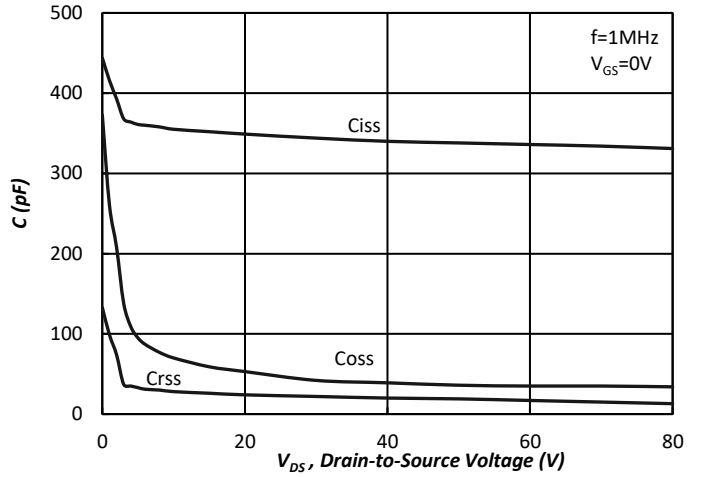


Fig.8 Typical Capacitance Characteristics

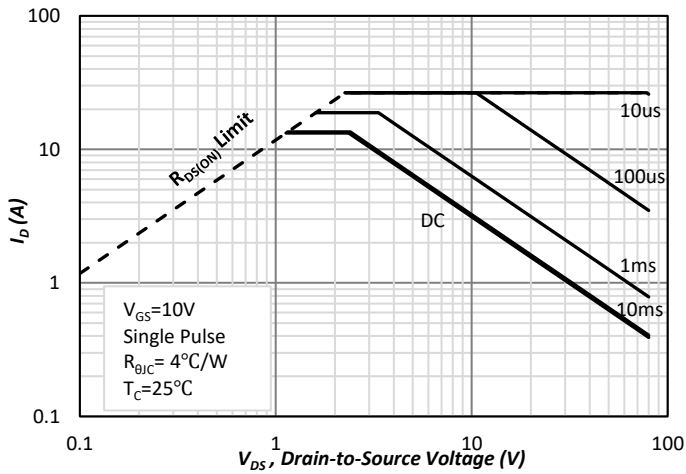


Fig 9. Maximum Safe Operating Area

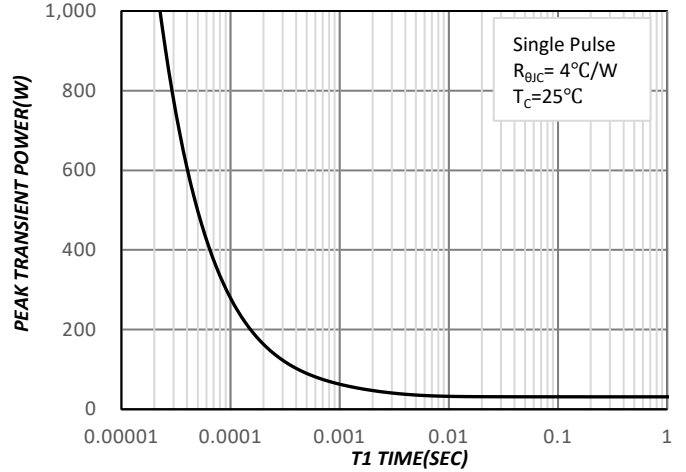


Fig 10. Single Pulse Maximum Power Dissipation

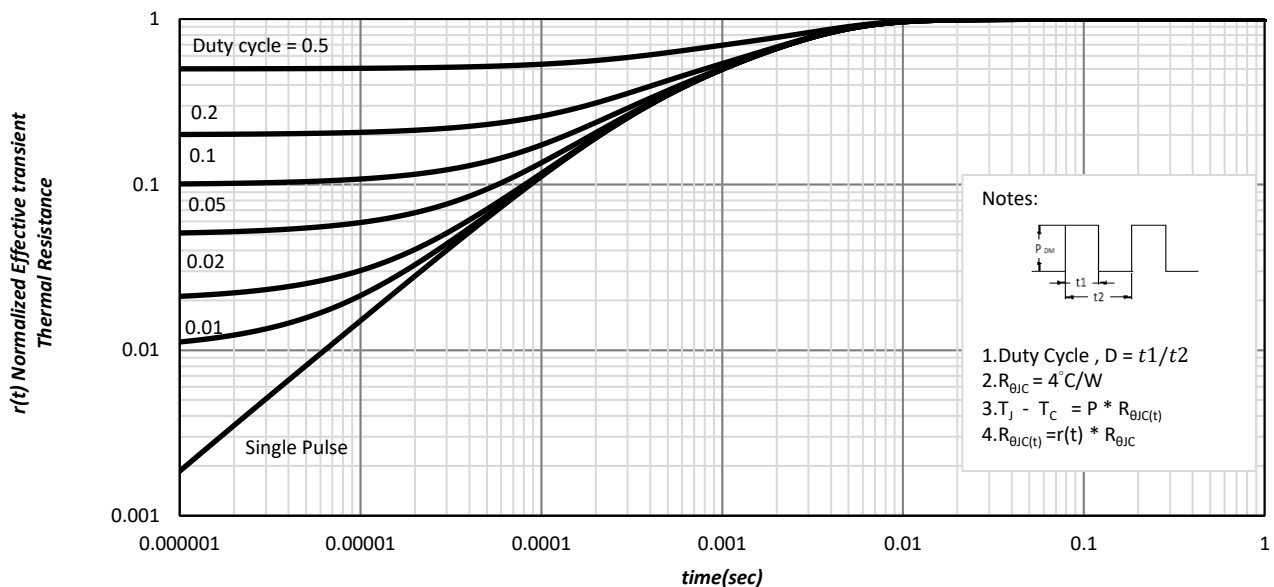


Fig 11. Effective Transient Thermal Impedance

▪ Q2 ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	80			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.2	1.8	2.5	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 80V, V _{GS} = 0V			1	μA
		V _{DS} =80V, V _{GS} =0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	13			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 4.5A		65	85	mΩ
		V _{GS} = 4.5V, I _D = 2.5A		76	110	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 10A		17		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 40V, f = 1MHz		338		pF
Output Capacitance ⁵	C _{oss}			39		
Reverse Transfer Capacitance ⁵	C _{rss}			19		
Gate Resistance ^{4,5}	R _g	f = 1MHz		6.0		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 40V, V _{GS} = 10V, I _D = 4.5A		7		nC
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =4.5V)			3.3		
Gate-Source Charge ^{1,2,5}	Q _{gs}			2		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			1		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 40V, V _{GS} = 10V, I _D = 4.5A , R _g = 3Ω		4.9		nS
Rise Time ^{1,2,5}	t _r			6.6		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			15		
Fall Time ^{1,2,5}	t _f			14		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				26	A
Pulsed Current ³	I _{SM}				27	
Forward Voltage ^{1,4}	V _{SD}	I _F = 4.5A, V _{GS} = 0V			1.2	V
Reverse Recovery Time ⁵	t _{rr}	I _F = 10A, dI _F /dt = 100A / μS		17		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			1.6		A
Reverse Recovery Charge ⁵	Q _{rr}			14		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

Q2_TYPICAL CHARACTERISTICS

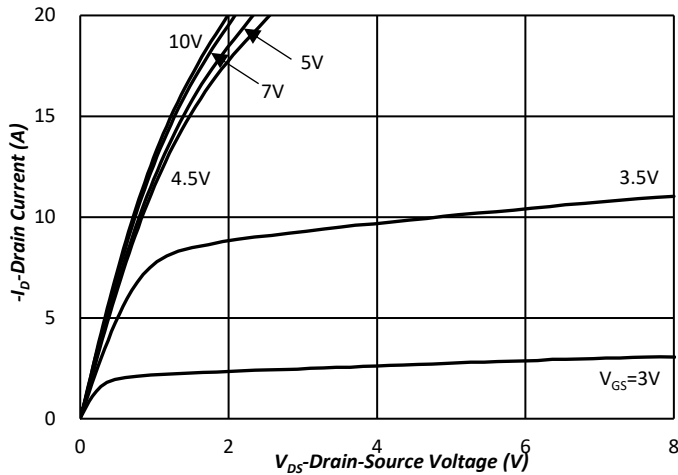


Fig.1 Typical Output Characteristics

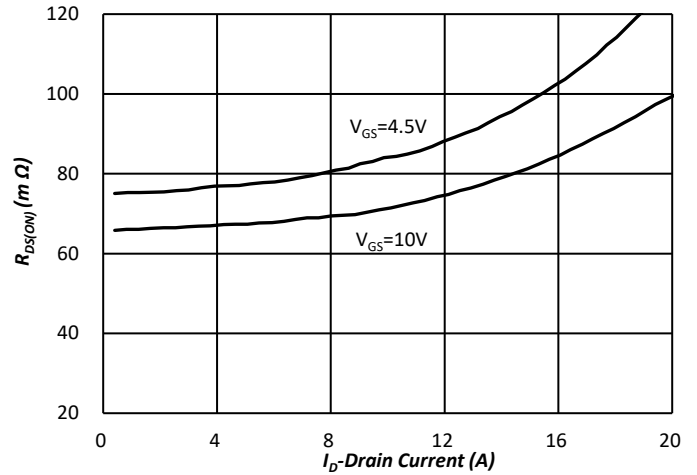


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

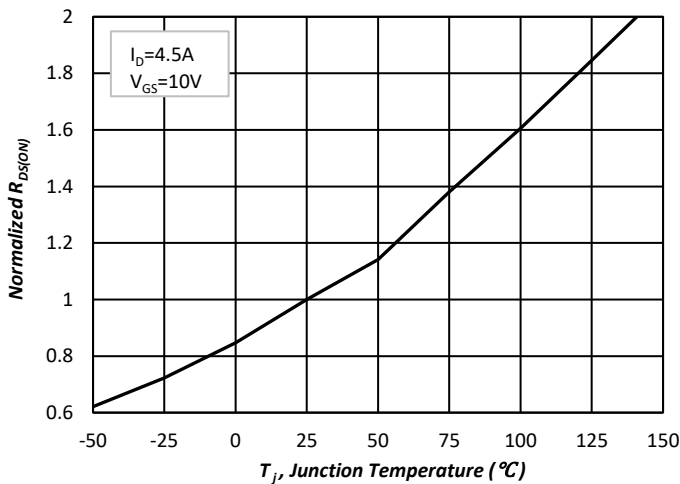


Fig.3 Normalized On-Resistance v.s. Junction Temperature

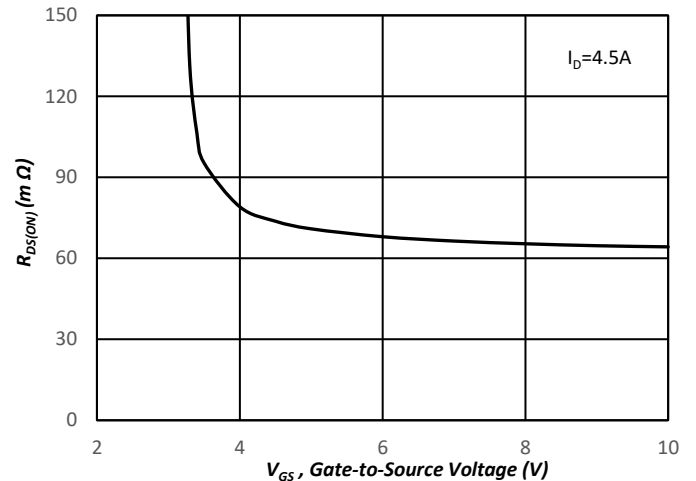


Fig.4 On-Resistance v.s. Gate Voltage

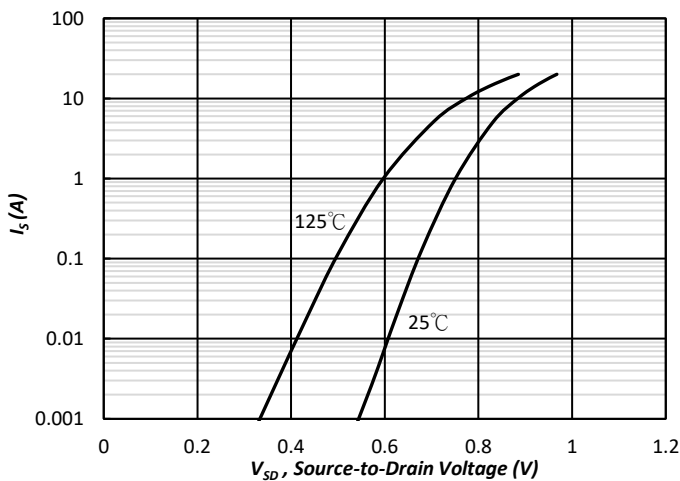


Fig.5 Forward Characteristic of Reverse Diode

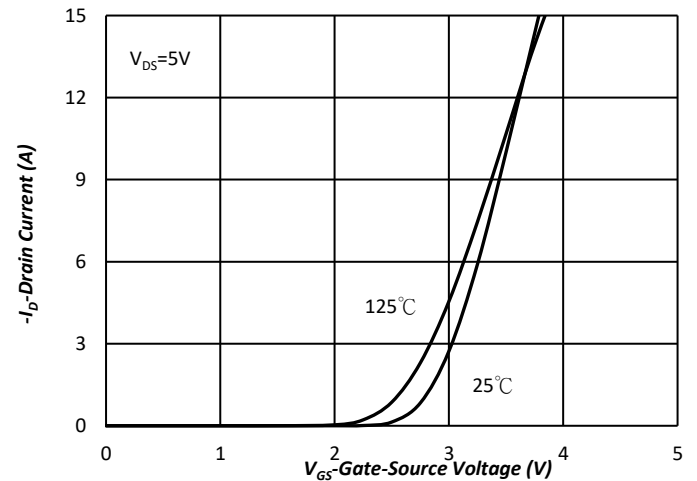


Fig.6 Transfer Characteristics

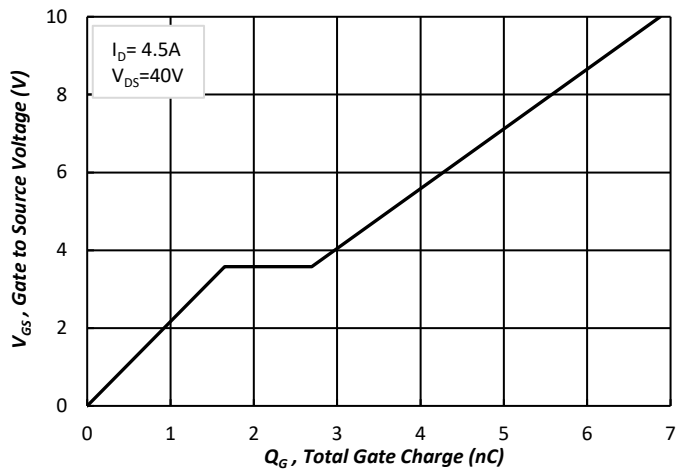


Fig.7 Gate Charge Characteristics

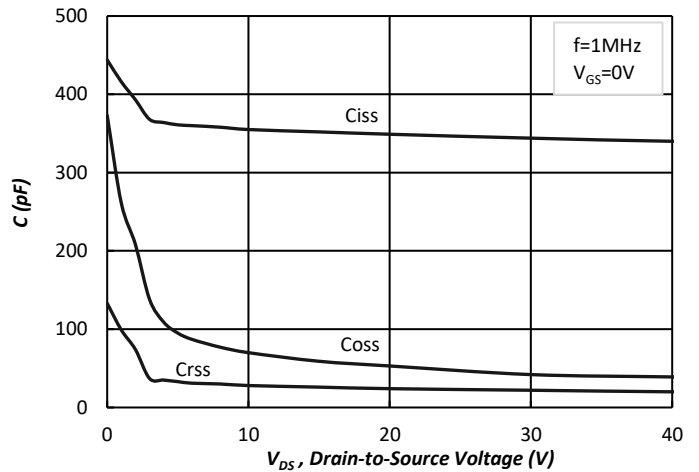


Fig.8 Typical Capacitance Characteristics

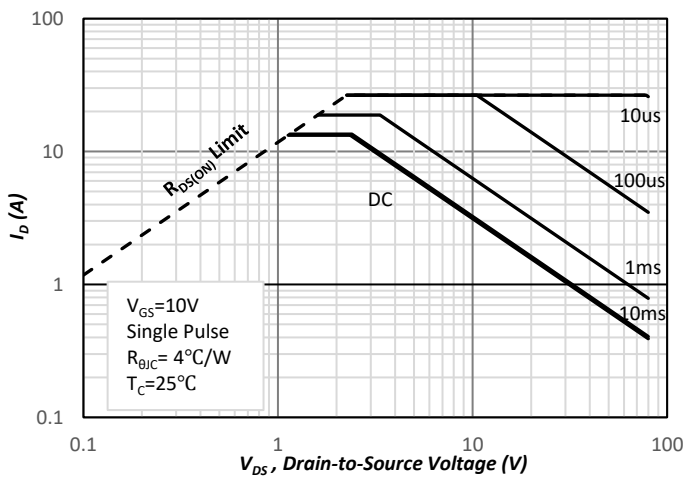


Fig.9. Maximum Safe Operating Area

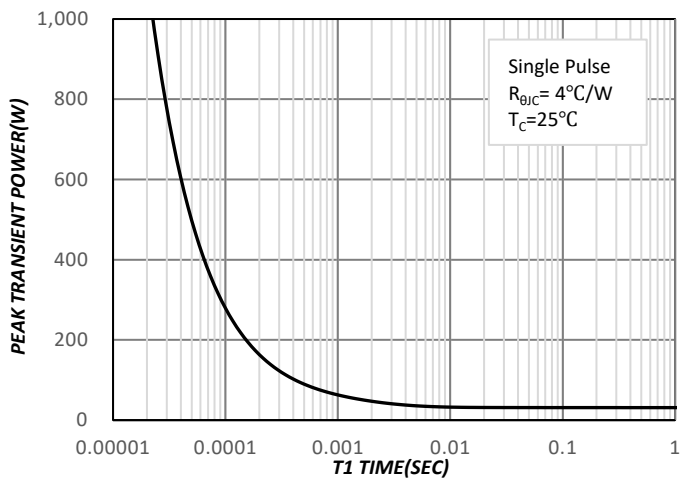


Fig.10. Single Pulse Maximum Power Dissipation

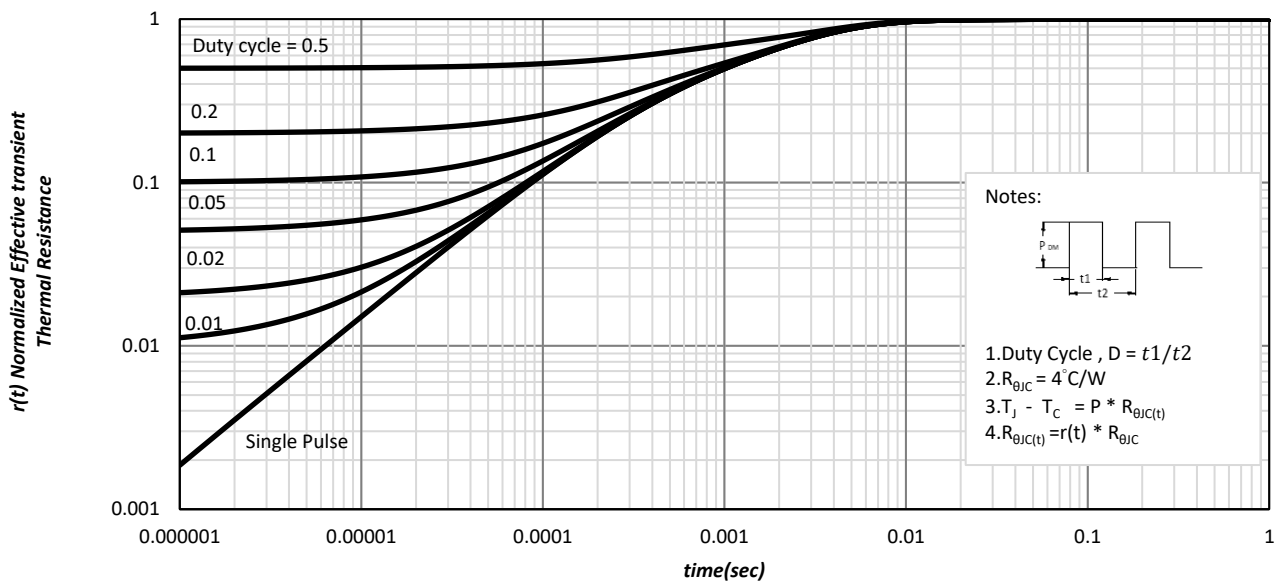
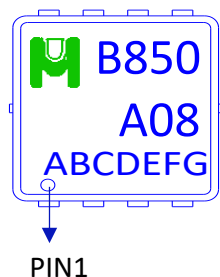


Fig.11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMCB850A08V for EDFN3X3



→ B850A08: Device Name

→ ABCDEFGH: Date Code

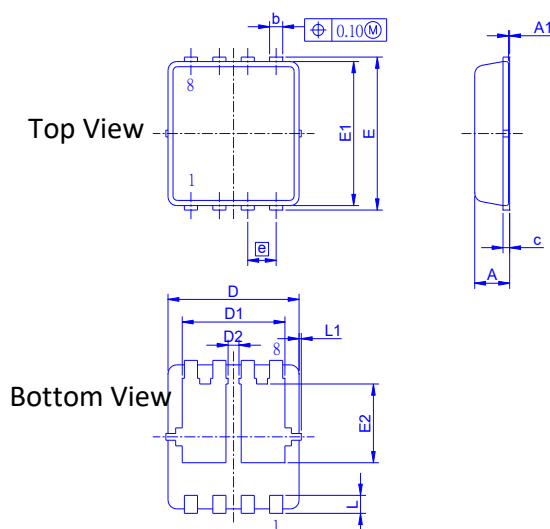
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

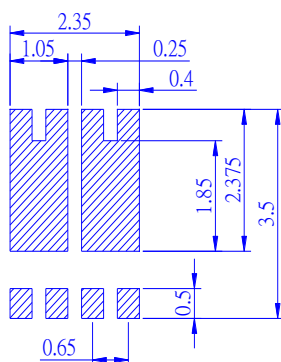
Outline Drawing



Dimension in mm

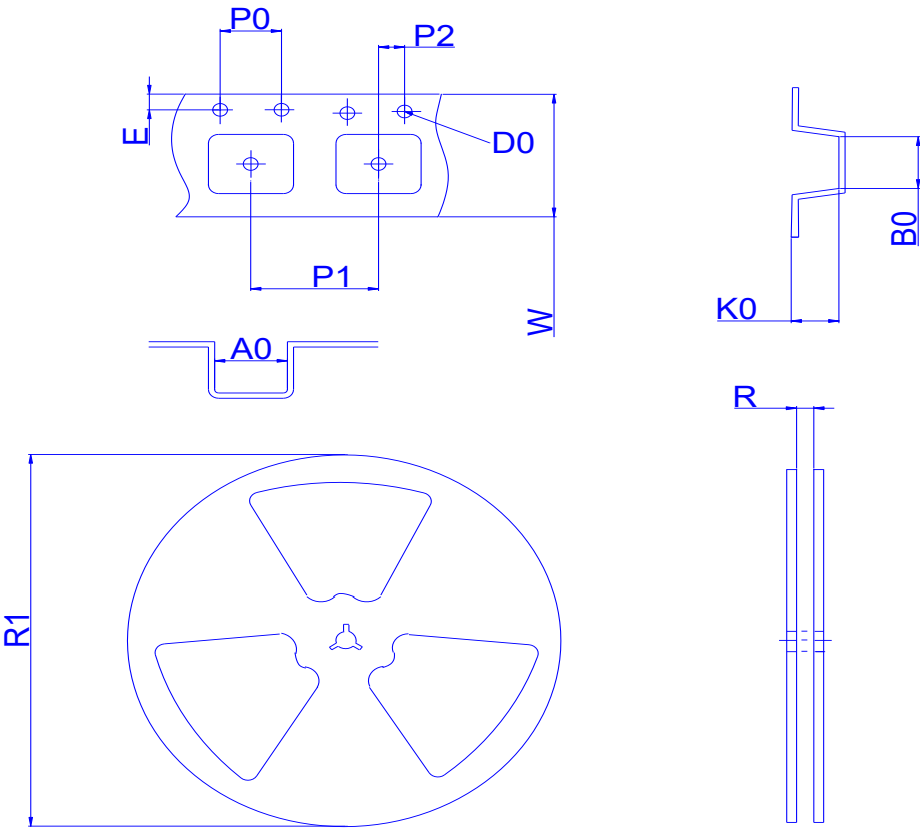
Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	e	L	L1	θ1
Min.	0.65	0	0.20	0.10	2.90	2.15	0.28	3.10	2.90	1.53	0.55	0.30	-	0°
Typ.	0.75	-	0.30	0.15	3.00	2.47	0.38	3.20	3.00	1.81	0.65	0.40	0.075	10°
Max.	0.90	0.05	0.40	0.25	3.30	2.75	-	3.50	3.30	1.98	0.75	0.50	0.15	14°

Footprint





◆ Tape&Reel Information:5000pcs/Reel



Package	EDFN3X3
Reel	13"
Device orientation	FEED DIRECTION

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	3.6	3.6	1.55	1.7	1.2	4	8	2	12	12.4	330
±	0.3	0.3	0.2	0.2	0.2	0.1	0.1	0.1	1	2	2