杰力科技股份有限公司
Excelliance MOS Corporation

EMCB070N08VSCS

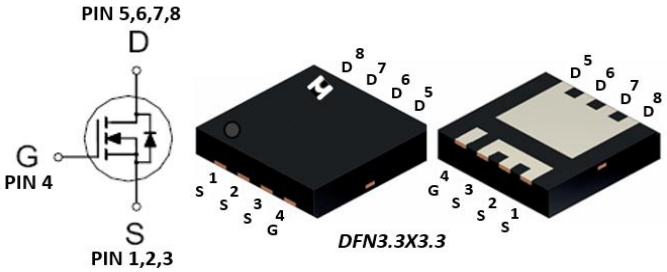
Single N-Channel Logic Level Enhancement Mode Field Effect Transistor

▪Product Summary:

	N-CH
BV_{DSS}	80V
$R_{DSON(MAX)}V_{GS}$=10V	7mΩ
$R_{DSON(MAX)}V_{GS}$=4.5V	10mΩ
I_D @T_C=25°C	113A
I_D @T_A=25°C	20A

Single N Channel MOSFET
UIS, Rg 100% Tested
RoHS & Halogen Free & TSCA Compliant

▪ Pin Description:



▪ ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	113	A
	T_C = 100 °C		71	
Continuous Drain Current	T_A = 25 °C	I_D	20	
	T_A = 70 °C		16	
Pulsed Drain Current[1]		I_{DM}	274	
Avalanche Current		I_{AS}	50	
Avalanche Energy	L = 0.1mH	EAS	125	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	EAR	63	
Power Dissipation	T_C = 25 °C	P_D	178	W
	T_C = 100 °C		71	
Power Dissipation	T_A = 25 °C	P_D	6.0	W
	T_A = 70 °C		4	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

▪ 100% UIS testing in condition of VD=60V, L=0.1mH, VG=10V, IL= 30A,RG=25Ω,Rated VDS=80V N-CH

▪THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case		$R_{\theta JC}$		0.7	°C/W
Junction-to-Ambient[3,4]	t≦10s	$R_{\theta JA}$		21	
	Steady-State	$R_{\theta JA}$		54	

[1]Pulse width limited by maximum junction temperature.
[2]Duty cycle < 1%
[3]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C.
[4]Guarantee by Engineering test

▪ ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage[4]	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250uA	80			V
Gate Threshold Voltage[4]	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.2	1.8	2.5	
Gate-Body Leakage[4]	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current[4]	I_{DSS}	V_{DS} = 80V, V_{GS} = 0V			1	μA
		V_{DS} =80V, V_{GS} =0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	113			A
Drain-Source On-State Resistance[1,4]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 20A		6.5	7	mΩ
Drain-Source On-State Resistance[1,4]	$R_{DS(ON)}$	V_{GS} = 4.5V, I_D = 10A		8.5	10	mΩ
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 20A		72		S
DYNAMIC						
Input Capacitance[5]	C_{iss}	V_{GS} = 0V, V_{DS} = 40V, f = 1MHz		1570		pF
Output Capacitance[5]	C_{oss}			272		
Reverse Transfer Capacitance[5]	C_{rss}			45		
Gate Resistance[4,5]	R_g	f = 1MHz		1.6		Ω
Total Gate Charge[1,2,5]	Q_g(V_{GS}=10V)	V_{DS} = 40V, V_{GS} = 10V, I_D = 20A		29		nC
Total Gate Charge[1,2,5]	Q_g(V_{GS}=4.5V)			14		
Gate-Source Charge[1,2,5]	Q_{gs}			7		
Gate-Drain Charge[1,2,5]	Q_{gd}			6		
Turn-On Delay Time[1,2,5]	$t_{d(on)}$	V_{DS} = 40V, V_{GS} = 10V, I_D = 5A , Rg = 3Ω		8		nS
Rise Time[1,2,5]	t_r			8		
Turn-Off Delay Time[1,2,5]	$t_{d(off)}$			37		
Fall Time[1,2,5]	t_f			20		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				148	A
Pulsed Current[3]	I_{SM}				274	
Forward Voltage[1,4]	V_{SD}	I_F = 20A, V_{GS} = 0V			1.2	V
Reverse Recovery Time[5]	t_{rr}	I_F = 20A, dI_F/dt = 100A / μS		36		nS
Peak Reverse Recovery Current[5]	$I_{RM(REC)}$			2		A
Reverse Recovery Charge[5]	Q_{rr}			33		nC

[1]Pulse test : Pulse Width ≦ 300 usec, Duty Cycle ≦ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

[4]Guarantee by FT test Item

[5]Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪ N-CH_TYPICAL CHARACTERISTICS

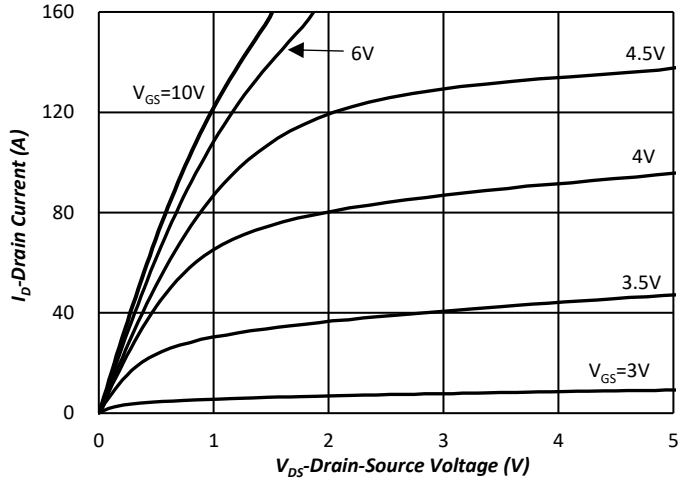


Fig.1 Typical Output Characteristics

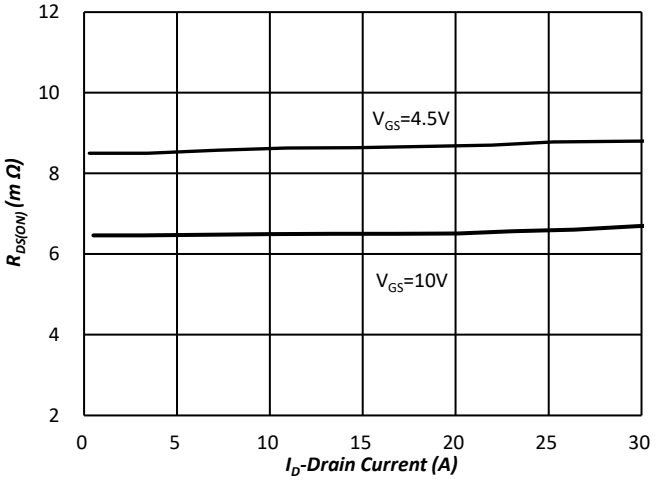


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

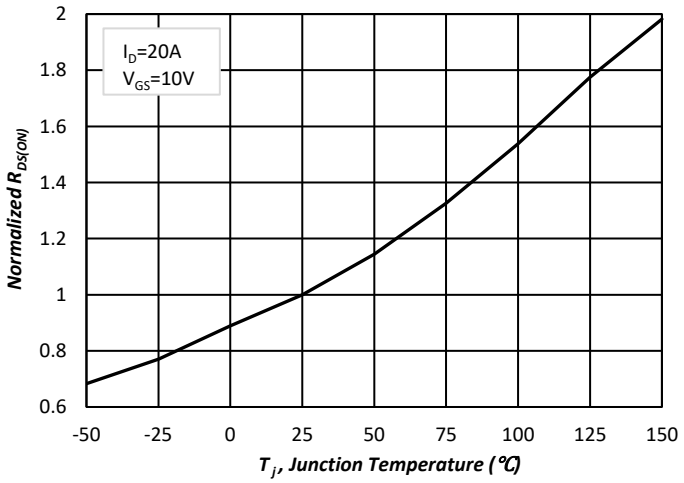


Fig.3 Normalized On-Resistance v.s. Junction Temperature

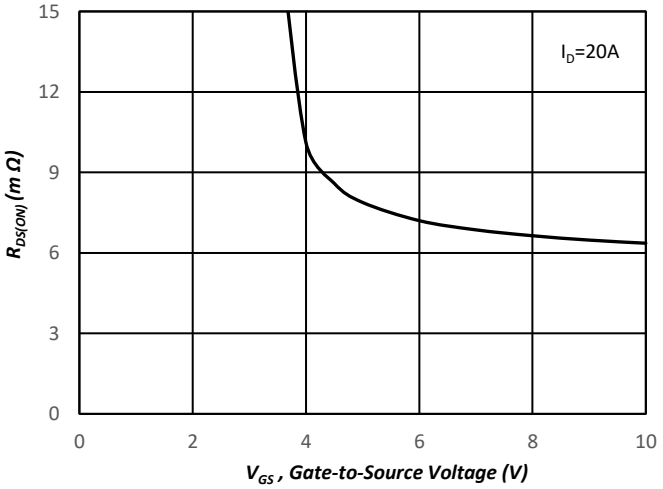


Fig.4 On-Resistance v.s. Gate Voltage

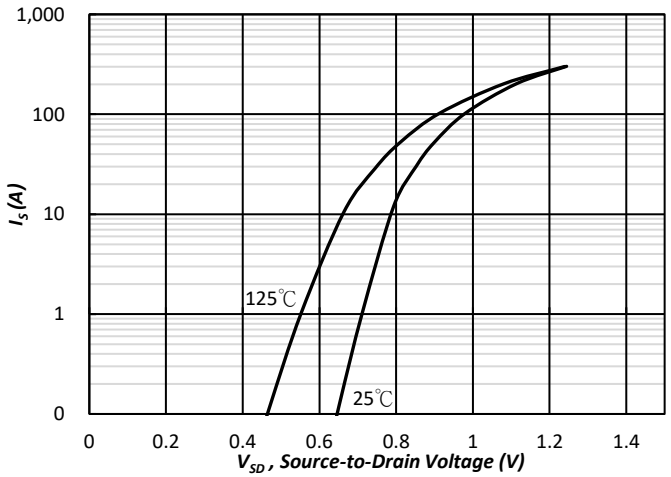


Fig.5 Forward Characteristic of Reverse Diode

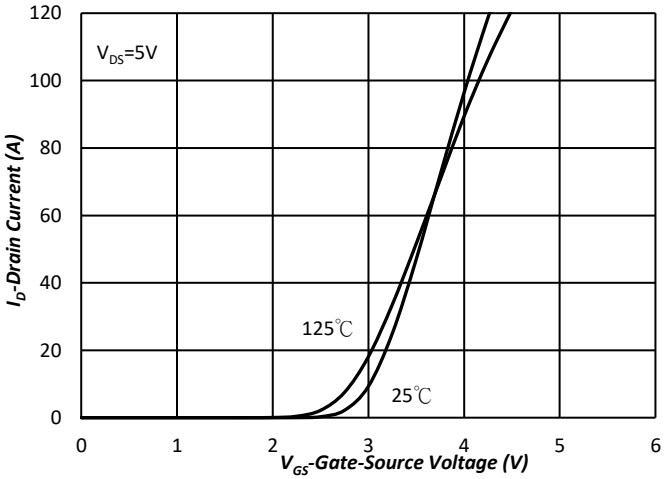


Fig.6 Transfer Characteristics

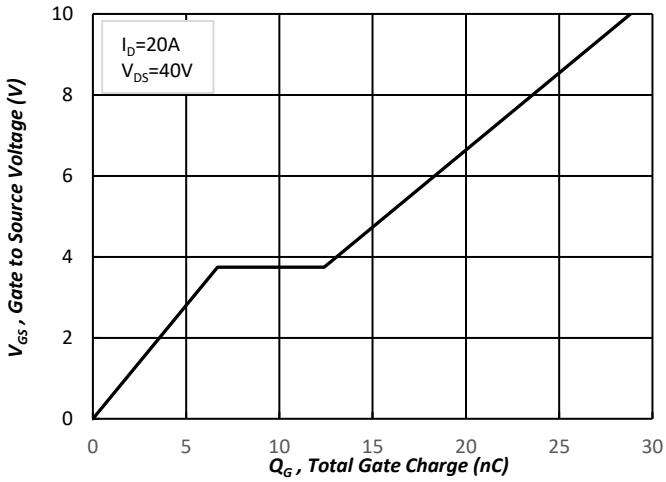


Fig.7 Gate Charge Characteristics

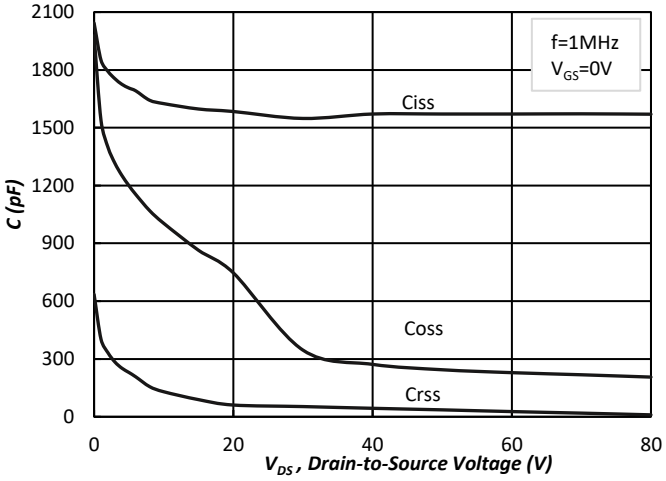


Fig.8 Typical Capacitance Characteristics

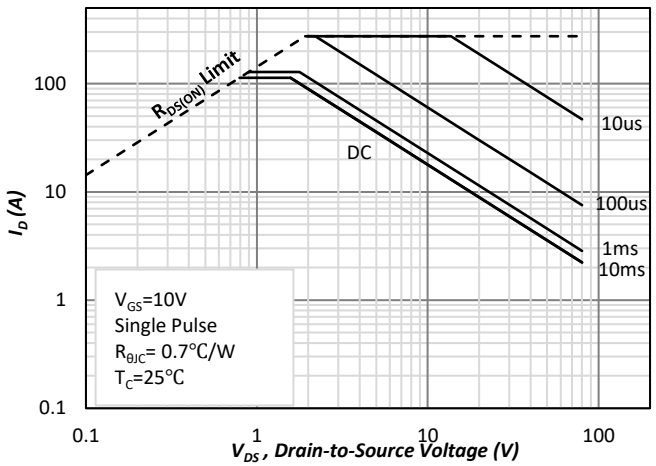


Fig 9. Maximum Safe Operating Area

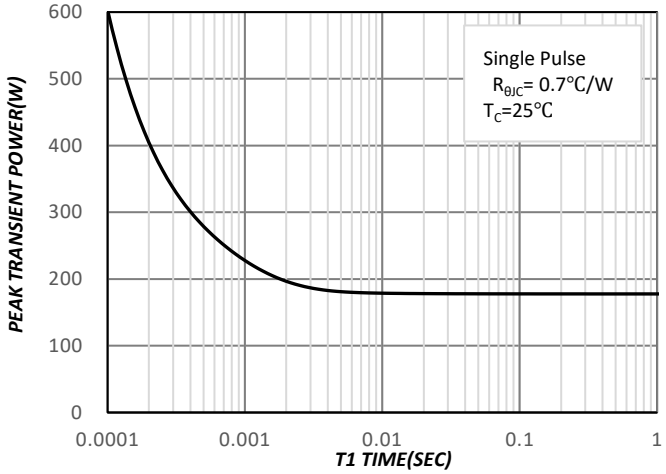


Fig 10. Single Pulse Maximum Power Dissipation

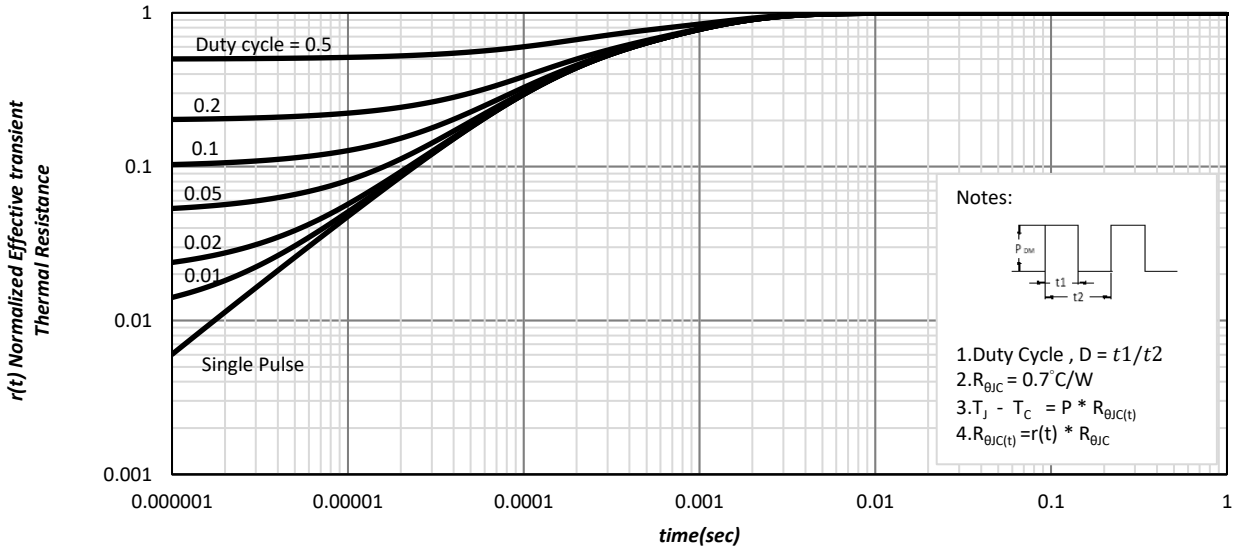


Fig 11. Effective Transient Thermal Impedance

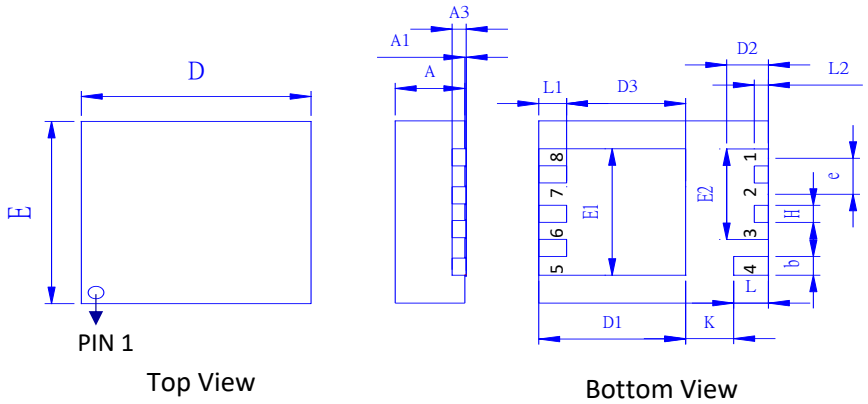
Ordering & Marking Information:

Device Name: EMCB070N08VSCS for DFN 3.3X3.3

B070N08S: Device Name

ABCDEFG: Date Code
A: Assembly House
B: Year(A:2008 B:2009 C:2010….)
C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)
DEFG: Serial No.

Outline Drawing



Top View

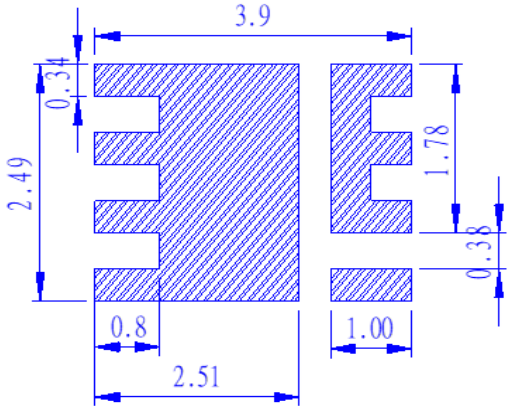
Bottom View

Dimension in mm

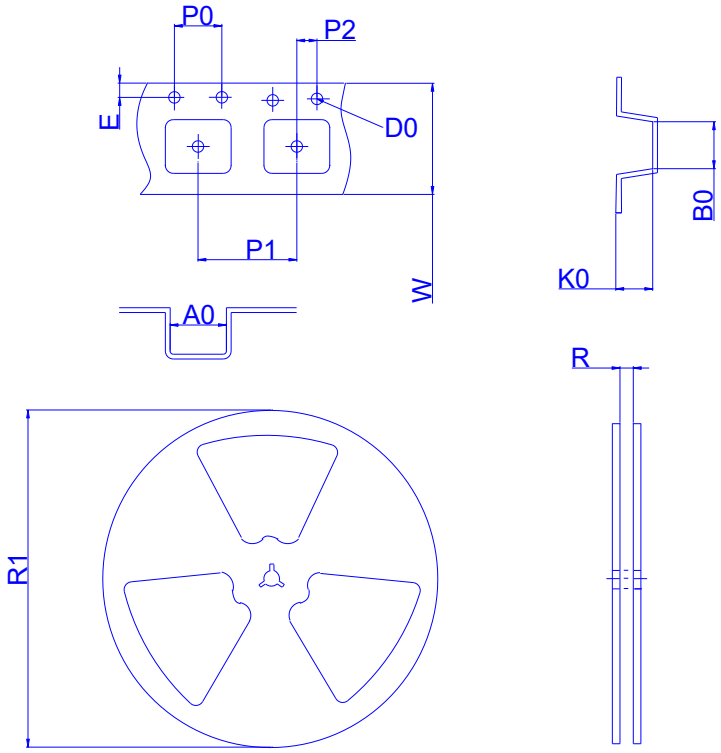
Dimension	A	A1	A3	b	D	E	D1	E1	E2	D3	e	H	L
Min	0.90	-	0.10	0.24	3.20	3.20	2.01	2.19	1.54	1.61	-	0.21	0.40
Typ.	1.00	0.02	-	-	3.30	3.30	2.11	2.29	1.64	-	0.65	0.31	0.55
Max	1.10	0.05	0.30	0.44	3.40	3.40	2.21	2.39	1.74	1.81	-	0.41	0.70

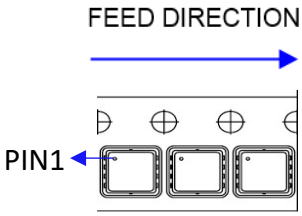
Dimension	L1	L2
Min	0.30	0.10
Typ.	0.40	0.20
Max	0.51	0.30

Footprint



◆ Tape&Reel Information: 5000pcs/Reel



Package	DFN3.3X3.3
Reel	13”
Device orientation	

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	3.6	3.6	1.55	1.7	1.2	4	8	2	12	12.4	330
±	0.3	0.3	0.2	0.2	0.2	0.1	0.1	0.1	1	2	2