

Single N-Channel Logic Level Enhancement Mode Field Effect Transistor

•Product Summary:

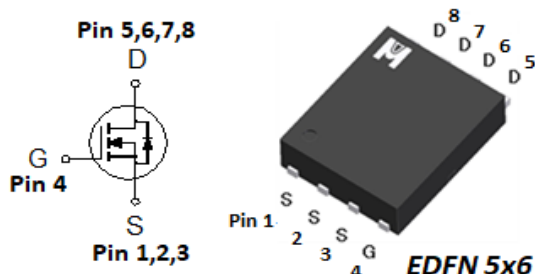
	N-CH
BV_{DSS}	60V
$R_{DS(on) (MAX.) @ V_{GS}=10V}$	3.8mΩ
$I_D @ T_C=25^{\circ}C$	178A
$I_D @ T_A=25^{\circ}C$	33A

Single N Channel MOSFET

UIS, Rg 100% Tested

RoHS & Halogen Free & TSCA Compliant

• Pin Description:



•ABSOLUTE MAXIMUM RATINGS ($T_C = 25^{\circ}C$ Unless Otherwise Noted)



PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^{\circ}C$	I_D	178	A
	$T_C = 100^{\circ}C$		112	
Continuous Drain Current	$T_A = 25^{\circ}C$	I_D	33	
	$T_A = 70^{\circ}C$		26	
Pulsed Drain Current ¹		I_{DM}	482	
Avalanche Current		I_{AS}	36	
Avalanche Energy	$L = 0.1mH$	EAS	65	mJ
Avalanche Energy	$L = 0.01mH$	EAS	6	
Repetitive Avalanche Energy ²	$L = 0.05mH$	EAR	32	
Power Dissipation	$T_C = 25^{\circ}C$	P_D	208	W
	$T_C = 100^{\circ}C$		83	
Power Dissipation	$T_A = 25^{\circ}C$	P_D	7.4	W
	$T_A = 70^{\circ}C$		5	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^{\circ}C$

¹ 100% UIS testing in condition of $V_D=30V$, $L=0.1mH$, $V_G=10V$, $I_L=22A$, $R_G=25\Omega$, Rated $V_{DS}=60V$ N-CH

•THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case		$R_{\theta JC}$		0.6	$^{\circ}C/W$
Junction-to-Ambient ^{3,4}	$t \leq 10s$	$R_{\theta JA}$		17	
	Steady-State	$R_{\theta JA}$		50	

¹ Pulse width limited by maximum junction temperature.

² Duty cycle $< 1\%$

³ The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}C$.

⁴ Guarantee by Engineering test



■ ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250uA	60			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.2	1.8	2.5	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 60V, V _{GS} = 0V			1	μA
		V _{DS} =60V, V _{GS} =0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	178			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A		3.1	3.8	mΩ
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 4.5V, I _D = 20A		4.8	5.5	mΩ
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 20A		67		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 30V, f = 1MHz		1944		pF
Output Capacitance ⁵	C _{oss}			522		
Reverse Transfer Capacitance ⁵	C _{rss}			38		
Gate Resistance ^{4,5}	R _g	f = 1MHz		2.0		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 30V, V _{GS} = 10V, I _D = 20A		35		nC
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =4.5V)			17		
Gate-Source Charge ^{1,2,5}	Q _{gs}			9		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			7		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 30V, V _{GS} = 10V, I _D = 5A , R _g = 3Ω		9		nS
Rise Time ^{1,2,5}	t _r			10		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			42		
Fall Time ^{1,2,5}	t _f			26		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				174	A
Pulsed Current ³	I _{SM}				366	
Forward Voltage ^{1,4}	V _{SD}	I _F = 20A, V _{GS} = 0V			1.2	V
Reverse Recovery Time ⁵	t _{rr}	I _F = 20A, dI _F /dt = 400A / μS		21		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			4		A
Reverse Recovery Charge ⁵	Q _{rr}			53		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

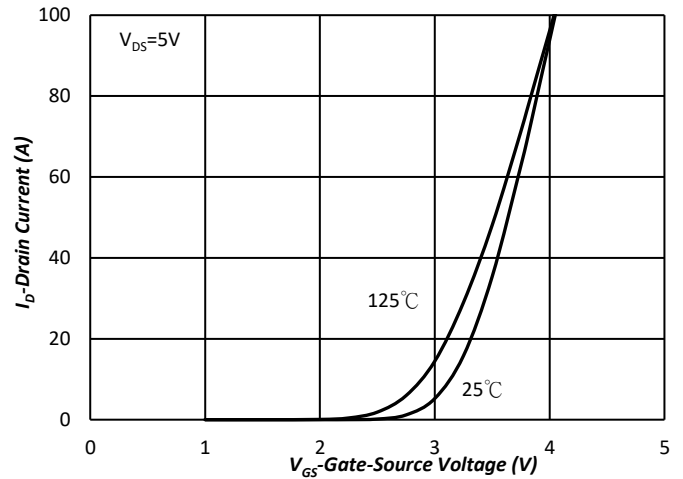
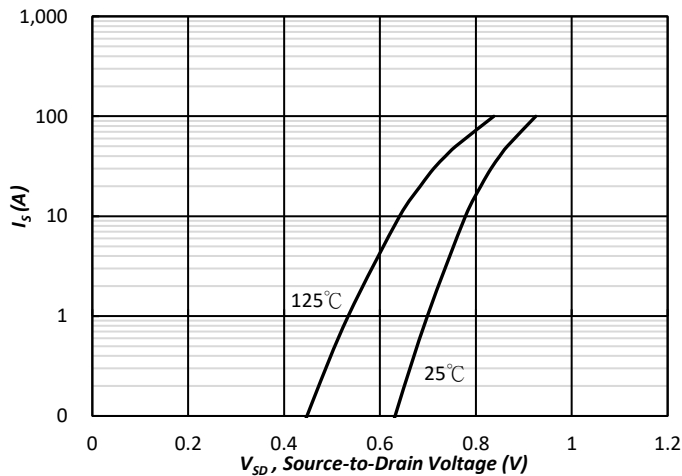
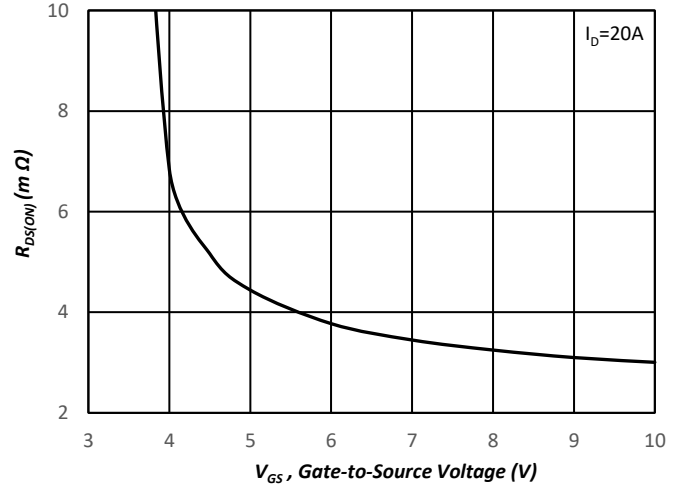
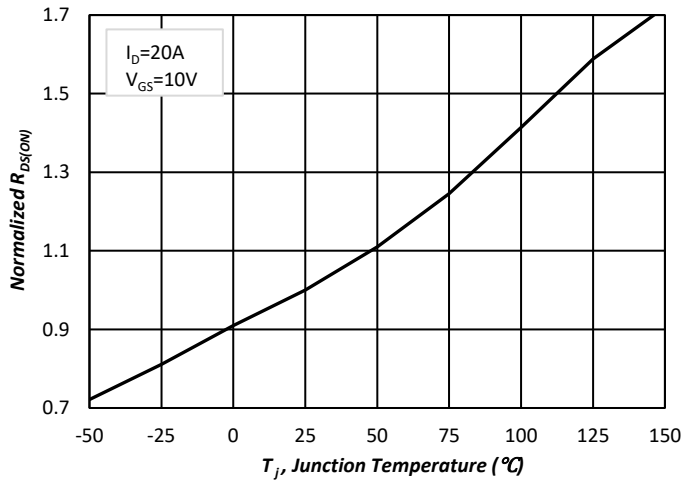
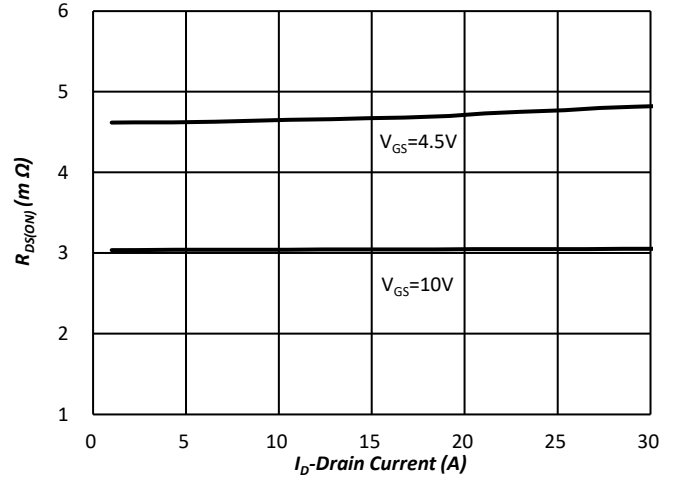
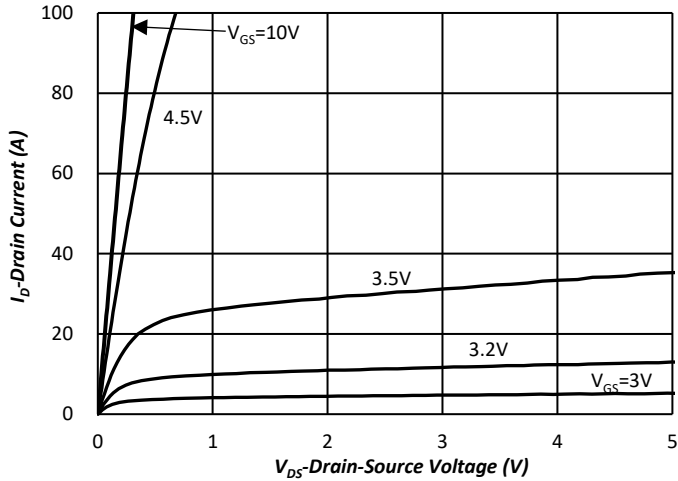
³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

■ **N-CH_TYPICAL CHARACTERISTICS**



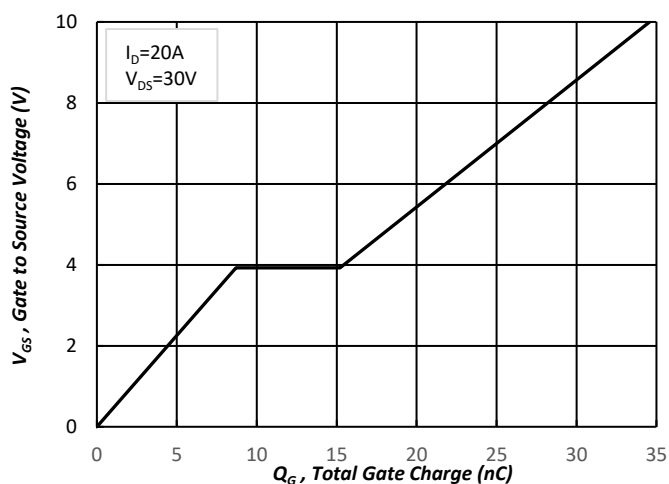


Fig.7 Gate Charge Characteristics

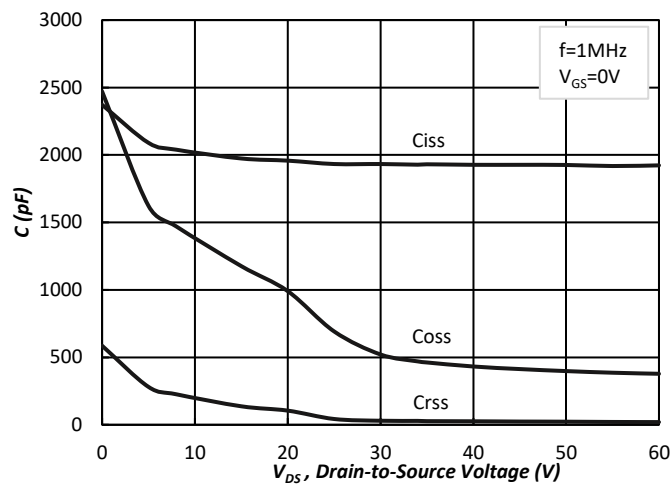


Fig.8 Typical Capacitance Characteristics

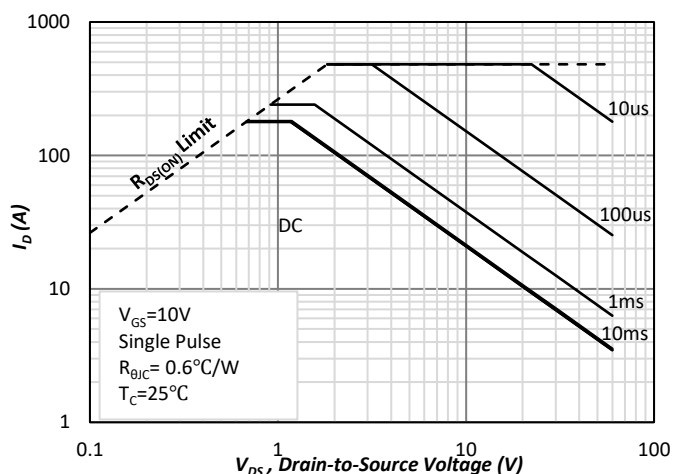


Fig.9. Maximum Safe Operating Area

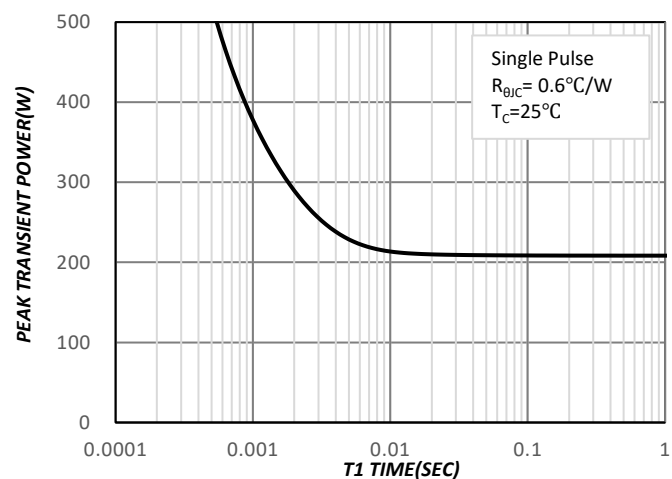


Fig.10. Single Pulse Maximum Power Dissipation

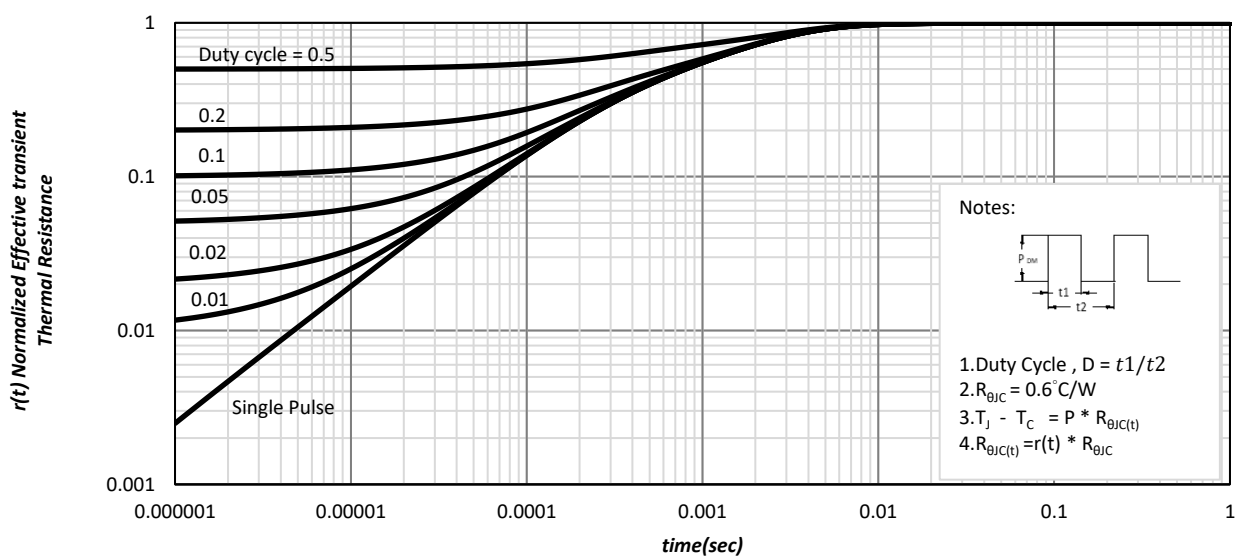


Fig.11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMCB038N06HCS for EDFN 5x6-A



B038N06S: Device Name

ABCDEFGH: Date Code

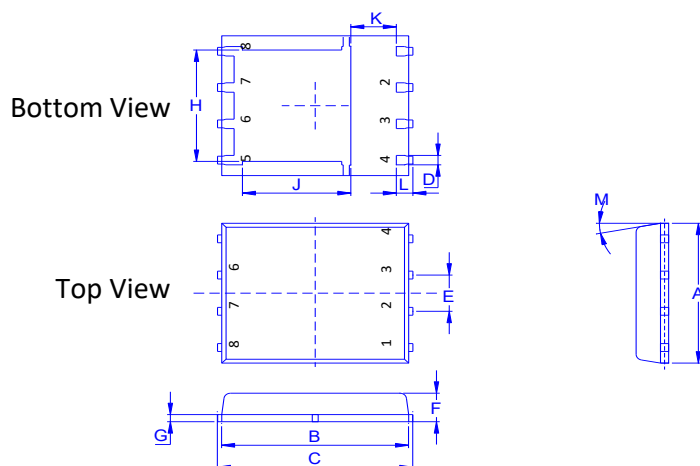
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

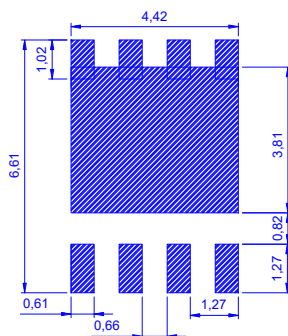
Outline Drawing



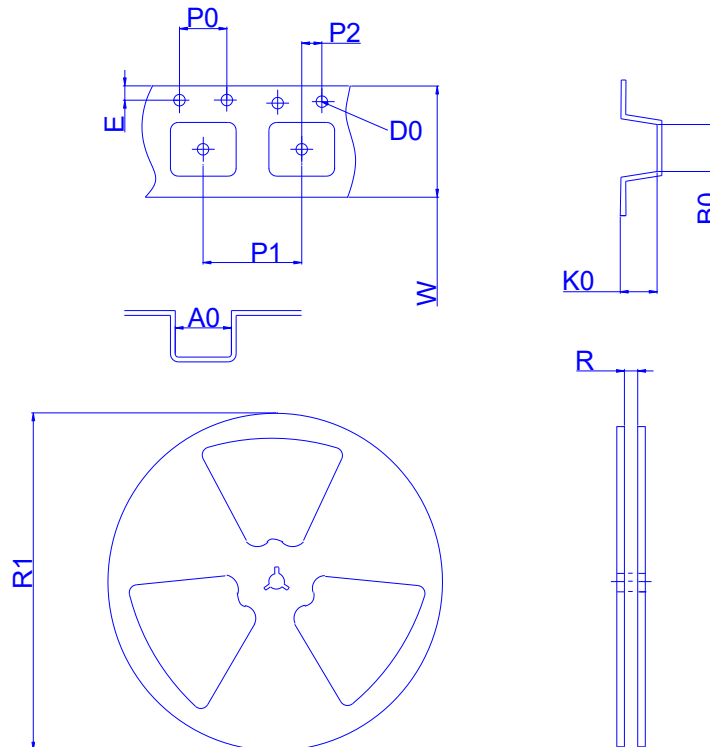
Dimension in mm

Dimension	A	B	C	D	E	F	G	H	J	K	L	M
Min	4.80	5.70	5.90	0.33	1.17	0.90	0.20	3.67	3.38	1.10	0.51	0°
Typ.	4.90	5.75	6.00	0.40	1.27	0.95	0.25	3.87	3.48	-	0.61	-
Max	5.00	5.80	6.10	0.51	1.37	1.10	0.34	4.02	3.78	-	0.71	12°

Footprint



◆ **Tape&Reel Information:2500pcs/Reel**



Package	EDFN5X6-A
Reel	13"
Device orientation	FEED DIRECTION

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	6.4	5.3	1.5	1.8	1.3	4	8	2	12	12.4	330
±	0.2	0.2	0.1	0.1	0.2	0.1	0.1	0.1	0.3	2	2