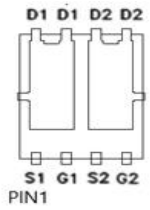
Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

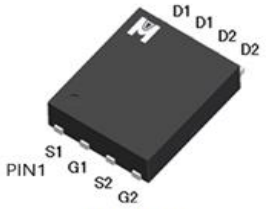
▪Product Summary:

	N-CH
BVDSS	60V
$R_{DSON\ (MAX.)}$@V_{GS}=10V	120mΩ
$R_{DSON\ (MAX.)}$@V_{GS}=4.5V	180mΩ
I_D @T_C=25°C	11A

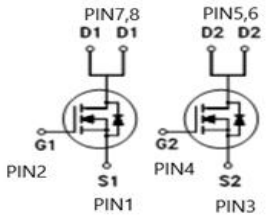
Dual N Channel MOSFET
UIS, Rg 100% Tested
RoHS & Halogen Free & TSCA Compliant

▪ Pin Description:





EDFN5X6



▪ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	11	A
	T_C = 100 °C		7.3	
Pulsed Drain Current[1]		I_{DM}	44	
Avalanche Current		I_{AS}	5	
Avalanche Energy	L = 0.1mH	EAS	1.25	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	EAR	0.63	
Power Dissipation	T_C = 25 °C	P_D	25	W
	T_C = 100 °C		10	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

100% UIS testing in condition of VD=30V, L=0.1mH, VG=10V, IL=3A, Rated VDS=60V N-CH
100% UIS testing in condition of VD=30V, L=0.1mH, VG=10V, IL=3A, Rated VDS=60V N-CH

▪THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		5	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$		62.5	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle < 1%

[3]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C.

[4]Guarantee by Engineering test

▪ ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250uA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250uA	1	1.7	2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48V, V_{GS} = 0V			1	uA
		V_{DS} = 48V, V_{GS} = 0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 10V	8			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 5A		100	120	mΩ
		V_{GS} = 4.5V, I_D = 4A		150	180	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 5A		8		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 30V, f = 1MHz		112		pF
Output Capacitance	C_{oss}			57		
Reverse Transfer Capacitance	C_{rss}			13		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz		3.5		Ω
Total Gate Charge[1,2]	Q_g(V_{GS}=10V)	V_{DS} = 30V, V_{GS} = 10V, I_D = 5A		3.2		nC
	Q_g(V_{GS}=4.5V)			2.1		
Gate-Source Charge[1,2]	Q_{gs}			0.5		
Gate-Drain Charge[1,2]	Q_{gd}			2.1		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 30V, V_{GS} = 10V, I_D = 5A , Rg = 6Ω		3.2		nS
Rise Time[1,2]	t_r			3		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			7.2		
Fall Time[1,2]	t_f			18.4		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
100% UIS testing in condition of VD=30V, L=0.1mH, VG=10V, IL=3A	I_S				11	A
Pulsed Current[3]	I_{SM}				44	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.3	V
Reverse Recovery Time	t_{rr}	I_F = I_S=5A, dI_F/dt = 100A / mS		7.2		nS
Reverse Recovery Charge	Q_{rr}			0.26		nC

[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

EMC will review datasheet by quarter, and update new version.

▪ TYPICAL CHARACTERISTICS

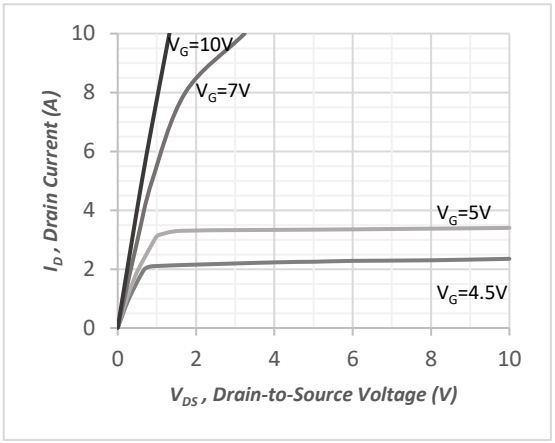


Fig.1 Typical Output Characteristics

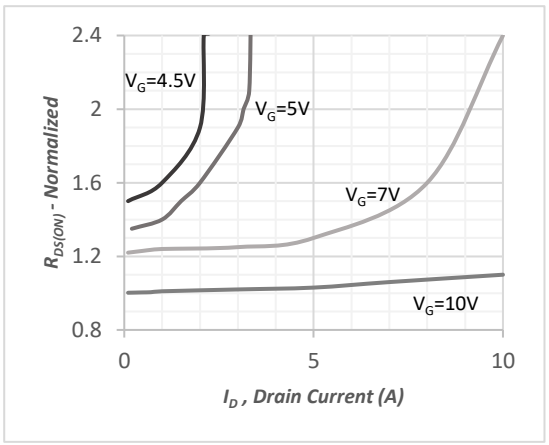


Fig.2 On-Resistance vs. Drain Current

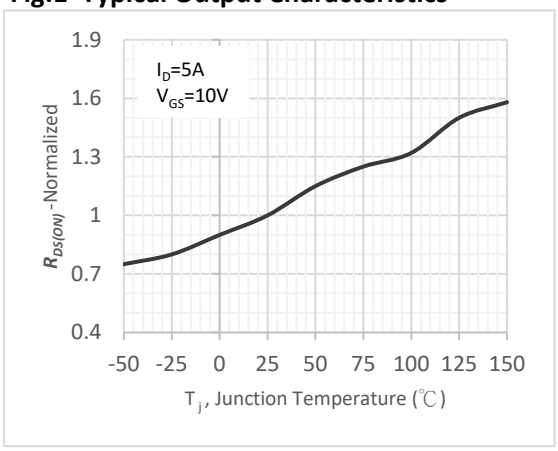


Fig.3 Normalized On-Resistance v.s. Junction Temperature

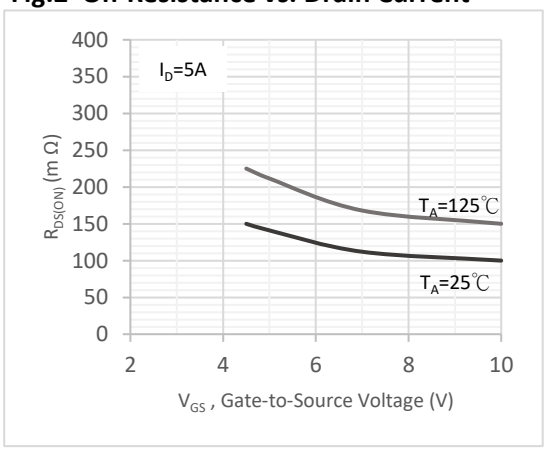


Fig.4 On-Resistance v.s. Gate Voltage

L=0.1mH, V

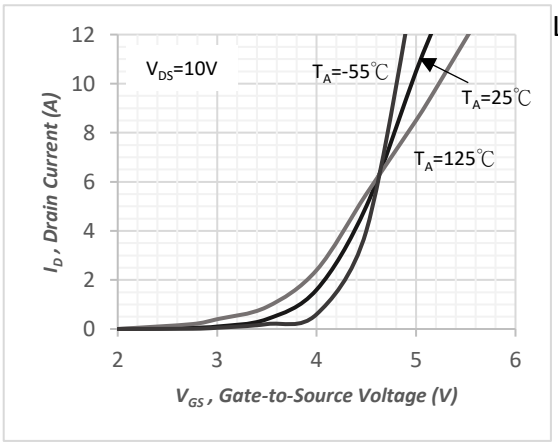


Fig.5 Forward Characteristic of Reverse Diode

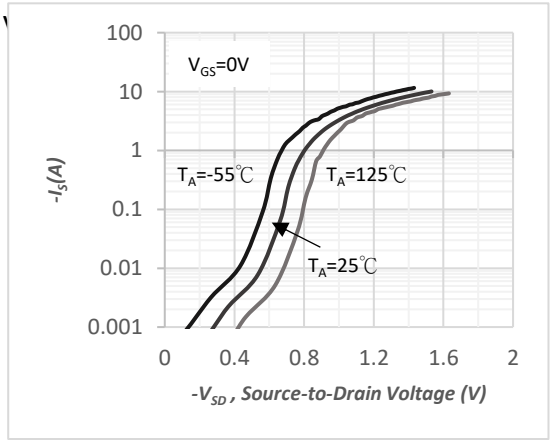


Fig.6 Transfer Characteristics

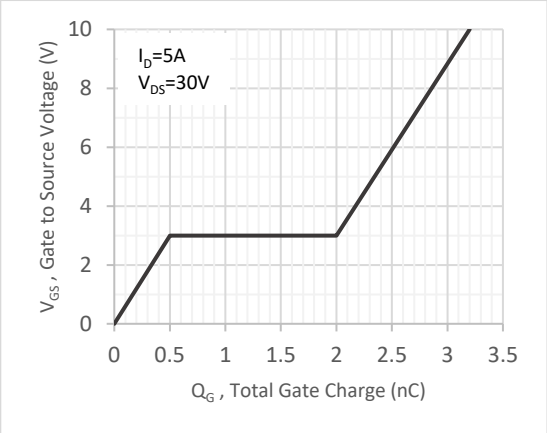


Fig.7 Gate Charge Characteristics

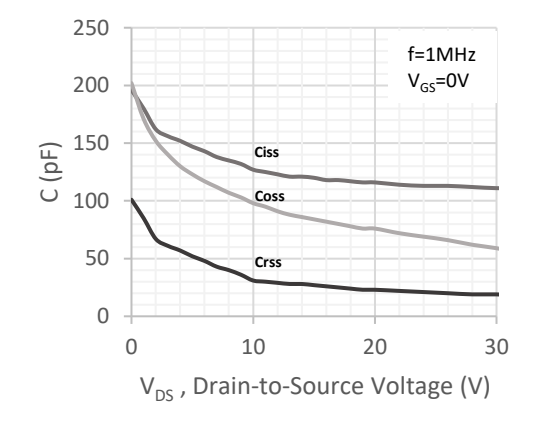


Fig.8 Typical Capacitance Characteristics

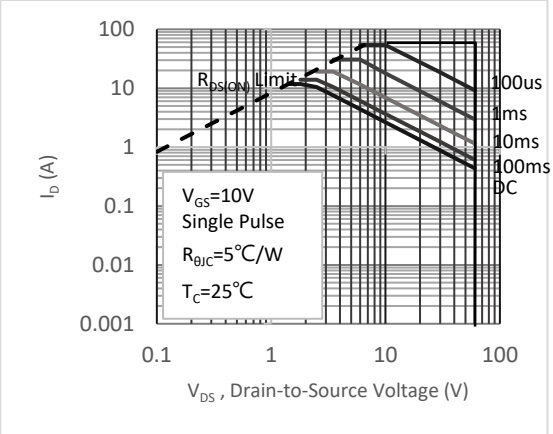


Fig 9. Maximum Safe Operating Area

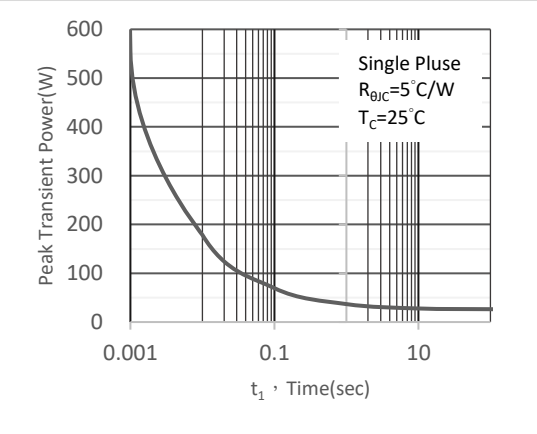


Fig 10. Single Pulse Maximum Power Dissipation

100% UIS testing in condition of VD=30V, L=0.1mH, VG=10V, IL=3A, Rated VDS=60V N-CH

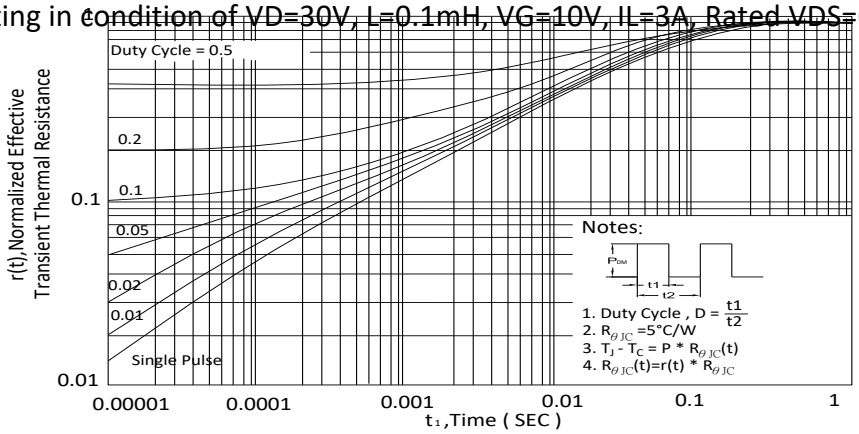


Fig 11. Effective Transient Thermal Impedance

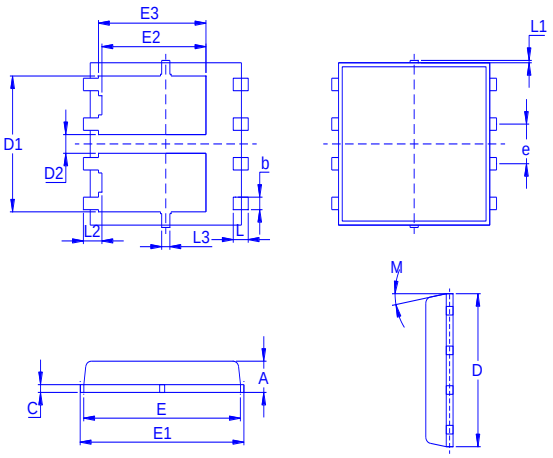
Ordering & Marking Information:

Device Name: EMBA2A06HS for EDFN 5x6

BA2A06S: Device Name

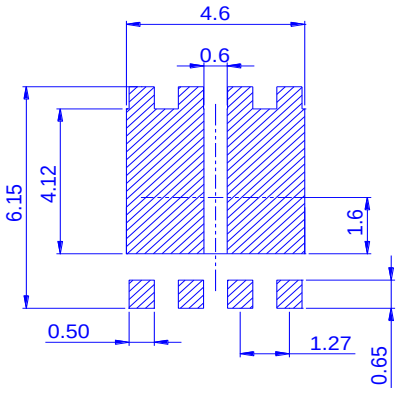
ABCDEFG: Date Code
A: Assembly House
B: Year(A:2008 B:2009 C:2010….)
C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)
DEFG: Serial No.

Outline Drawing

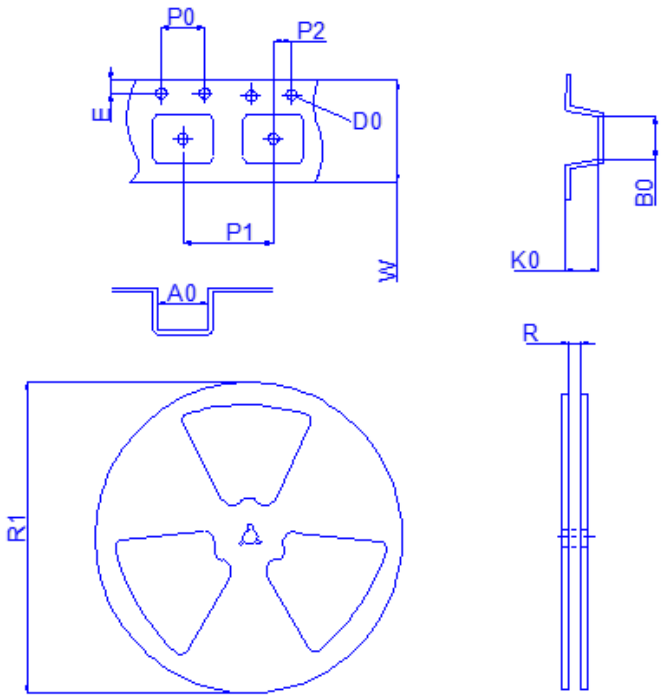


Dimension	A	b	c	D	D1	D2	E	E1	E2	e	L	L1	L2	M
Min	0.85	0.3	0.15			0.5					0.45	0		0°
0V, L=0.1mH	0.95	0.4	0.2	5.2	4.35	0.6	5.55	6.05	3.82	1.27	0.55		0.68	
Max	1	0.5	0.25			0.75					0.65	0.15		10°

Footprint



◆ **Tape&Reel Information:2500pcs/Reel(Dimension in millimeter)**



Package	EDFN5X6
Reel	13”
Device orientation	FEED DIRECTION

100% UIS testing in

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	6.4	5.3	1.5	1.8	1.6	4	8	2	12	12.4	330
±	0.2	0.2	0.1	0.1	0.6	0.1	0.1	0.1	0.3	2	2