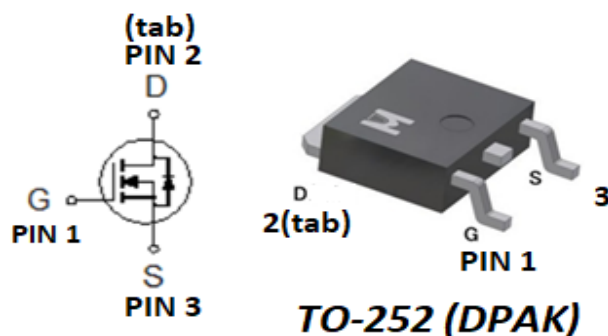


Single N-Channel Logic Level Enhancement Mode Field Effect Transistor

•Product Summary:

	N-CH
BVDSS	80V
$R_{DS(on)} (MAX.) @ V_{GS}=10V$	85.0m Ω
$R_{DS(on)} (MAX.) @ V_{GS}=4.5V$	110.0m Ω
$I_D @ T_C=25^{\circ}C$	14.0A
$I_D @ T_A=25^{\circ}C$	3.0A

• Pin Description:



Single N Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

•ABSOLUTE MAXIMUM RATINGS ($T_C = 25^{\circ}C$ Unless Otherwise Noted)



PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^{\circ}C$	I_D	14	A
	$T_C = 100^{\circ}C$		9	
Continuous Drain Current	$T_A = 25^{\circ}C$	I_D	3	
	$T_A = 70^{\circ}C$		2	
Pulsed Drain Current ¹		I_{DM}	35.0	
Avalanche Current		I_{AS}	27	mJ
Avalanche Energy	$L = 0.1mH$	EAS	36.5	
Repetitive Avalanche Energy ²	$L = 0.05mH$	EAR	18.2	
Power Dissipation	$T_C = 25^{\circ}C$	P_D	35.7	W
	$T_C = 100^{\circ}C$		14.3	
Power Dissipation	$T_A = 25^{\circ}C$	P_D	1.7	W
	$T_A = 70^{\circ}C$		1.1	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	$^{\circ}C$

• 100% UIS testing in condition of $V_D=40V$, $L=0.1mH$, $V_G=10V$, $I_L=16A$, Rated $V_{DS}=80V$ N-CH

•THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		3.5	$^{\circ}C/W$
Junction-to-Ambient ³	$R_{\theta JA}$		75	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $< 1\%$

³ $75^{\circ}C / W$ when mounted on a 1 in² pad of 2 oz copper.

⁴Guarantee by Engineering test

▪ ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250uA	80			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	1	2	3	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 64V, V _{GS} = 0V			1	uA
		V _{DS} =60V, V _{GS} =0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	14			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 10A		73	85	mΩ
		V _{GS} = 4.5V, I _D = 6A		90	110	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 6A		10		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 40V, f = 1MHz		495		pF
Output Capacitance ⁵	C _{oss}			48		
Reverse Transfer Capacitance ⁵	C _{rss}			29		
Gate Resistance ^{4,5}	R _g	f = 1MHz		4.1		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 40V, V _{GS} = 10V, I _D = 10A		11.4		nC
	Q _g (V _{GS} =4.5V)			5.7		
Gate-Source Charge ^{1,2,5}	Q _{gs}			2.1		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			2.7		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 40V, V _{GS} = 10V, I _D = 5A , R _g = 6Ω		6.1		nS
Rise Time ^{1,2,5}	t _r			10.5		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			21.2		
Fall Time ^{1,2,5}	t _f			20.6		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				14	A
Pulsed Current ³	I _{SM}				35	
Forward Voltage ^{1,4}	V _{SD}	I _F = 10A, V _{GS} = 0V			1.3	V
Reverse Recovery Time ⁵	t _{rr}	I _F = 10A, dI _F /dt = 100A / uS		20.7		nS
Reverse Recovery Charge ⁵	Q _{rr}			20.9		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪ TYPICAL CHARACTERISTICS

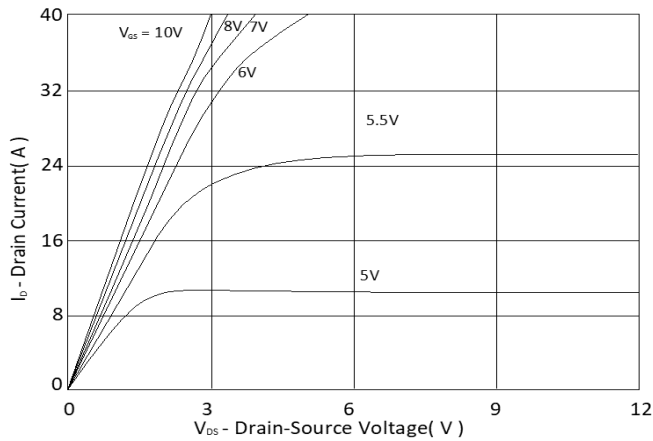


Fig.1 Typical Output Characteristics

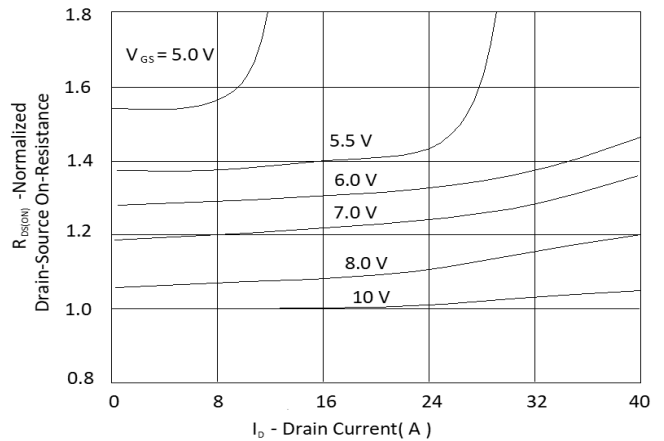


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

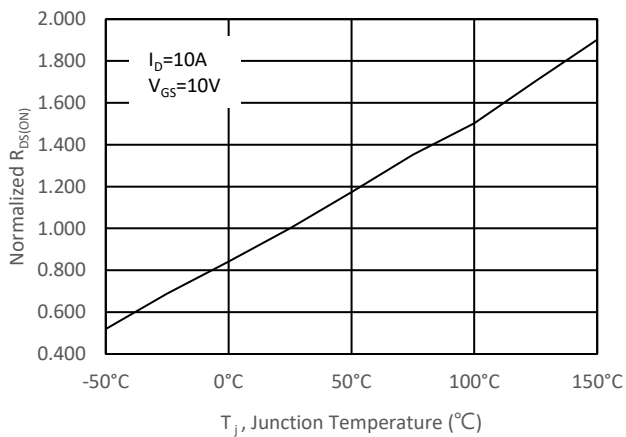


Fig.3 Normalized On-Resistance v.s. Junction Temperature

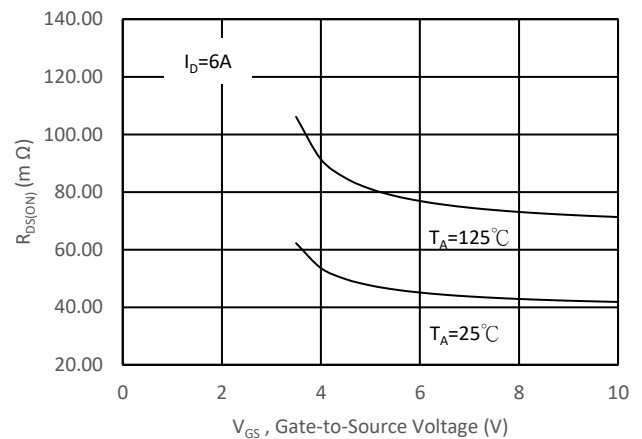


Fig.4 On-Resistance v.s. Gate Voltage

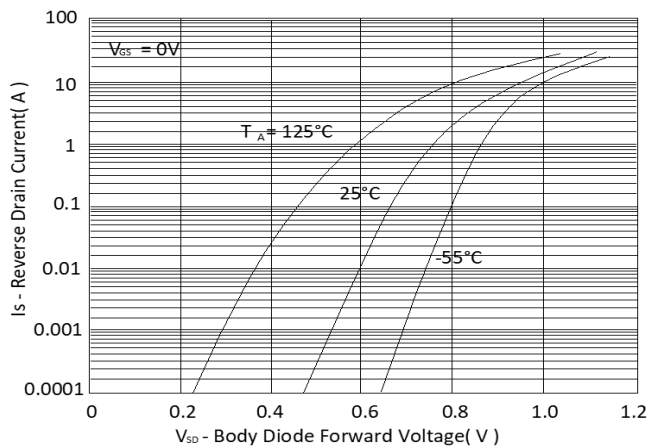


Fig.5 Forward Characteristic of Reverse Diode

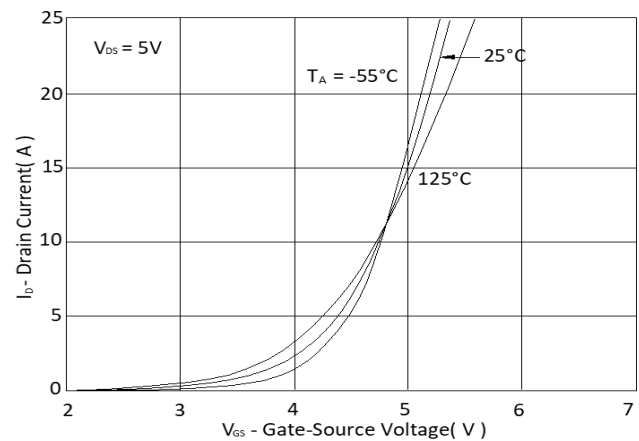


Fig.6 Transfer Characteristics

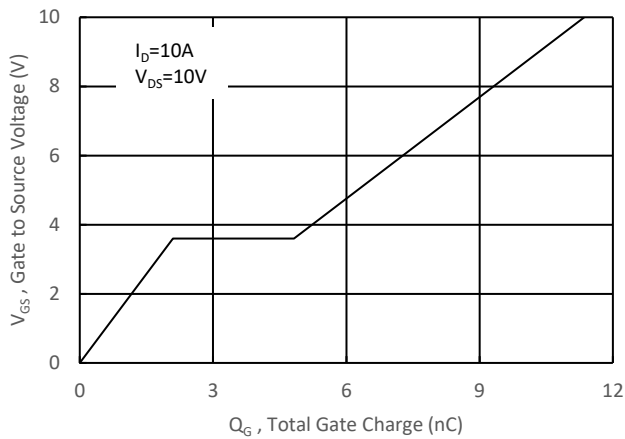


Fig. 7 Gate Charge Characteristics

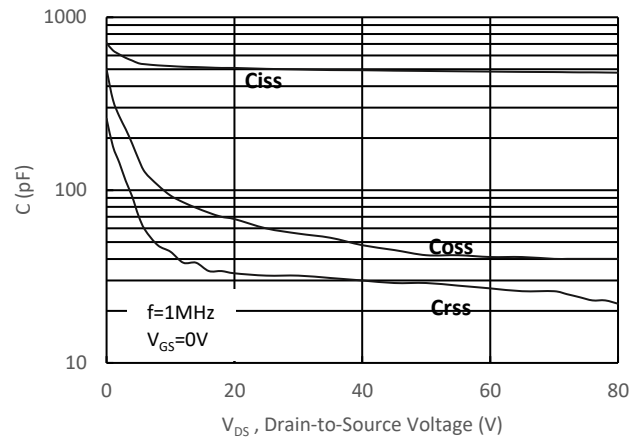


Fig. 8 Typical Capacitance Characteristics

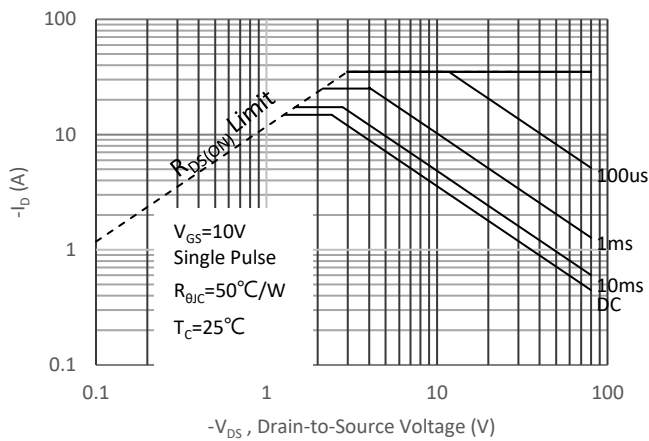


Fig. 9. Maximum Safe Operating Area

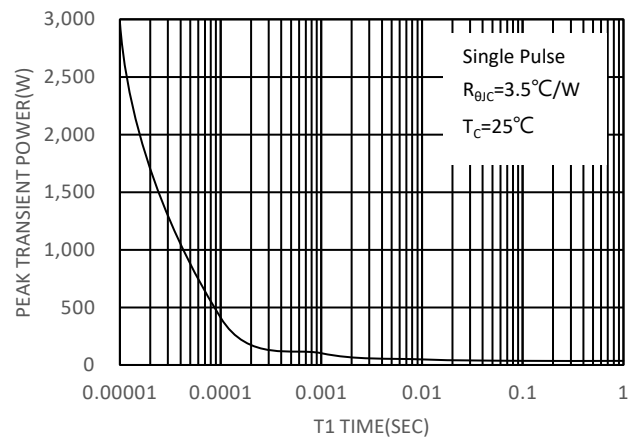


Fig 10. Single Pulse Maximum Power Dissipation

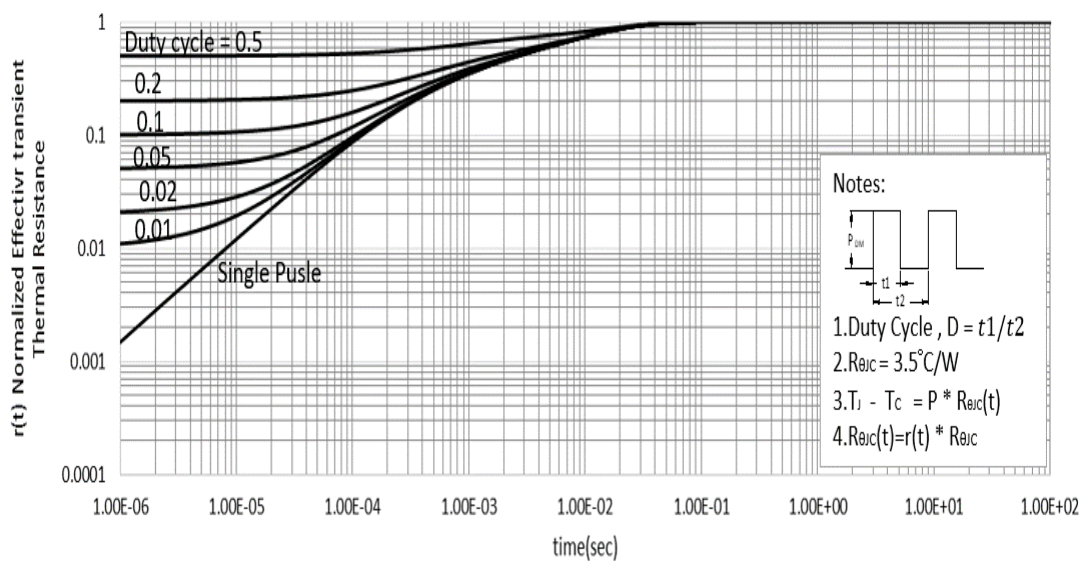


Fig 11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMB90N08A for TO-252 (DPAK)



B090N08: Device Name

ABCDEFGH: Date Code

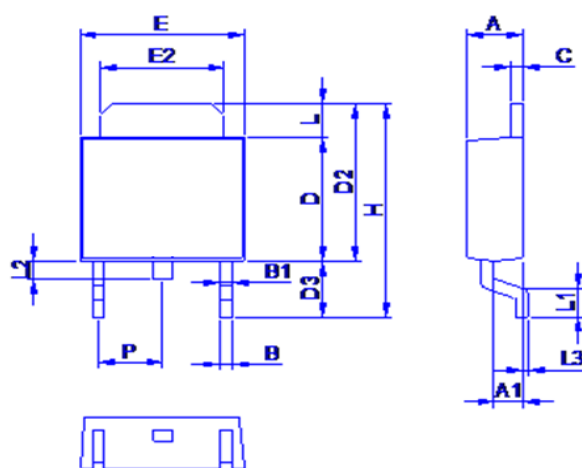
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

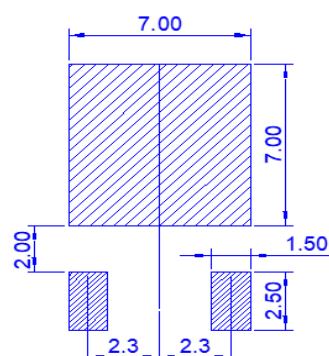
Outline Drawing



Dimension	A	A1	B	B1	C	D	D2	D3	E	E2	H	L	L1
Min.	2.1	0.95	0.62	0.65	0.45	5.96	6.8	2.6	6.3	4.9	9.3	0.8	1.2
Typ.	2.25	1.125	0.76	0.9	0.67	6.1	7.15	2.8	6.5	5.2	9.9	1.1	1.65
Max.	2.4	1.3	0.9	1.15	0.89	6.24	7.5	3	6.7	5.5	10.5	1.4	2.1

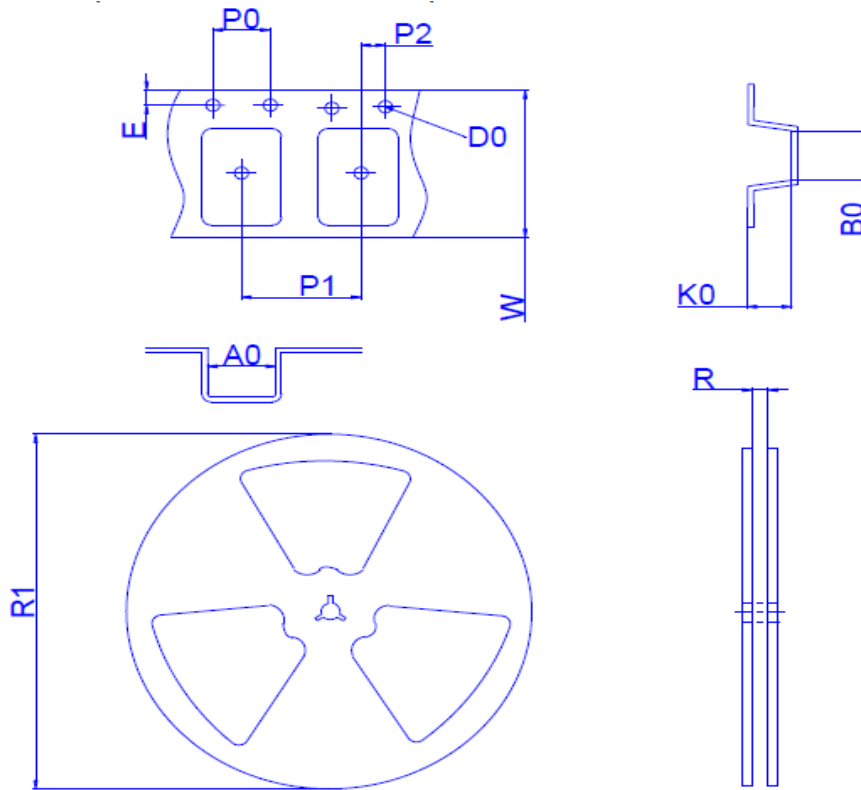
Dimension	L2	L3	P
Min.	0.5	0	2.1
Typ.	0.8	0.1	2.25
Max.	1.1	0.2	2.4

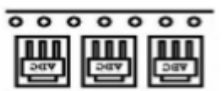
Footprint





◆ Tape&Reel Information:2500pcs/Reel



產品別	TO252-2
Reel 尺寸	13"
編帶 方式	FEED DIRECTION 

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	6.9	10.5	1.55	1.75	2.7	4	8	2	16	17	330
±	1	1	0.2	0.1	0.2	0.2	0.1	0.1	0.3	2	2



★Datasheet Latest version specification :

	Revision History	Prepared	Approved	Date
A.0	Initial Datasheet	Johnson	Sam	2020/11/24