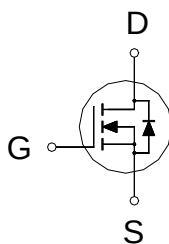


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	80V
$R_{DS(on)} (MAX.)$	65m Ω
I_D	12A



UIS, 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^\circ\text{C}$	I_D	12	A
	$T_A = 25^\circ\text{C}$		6	
	$T_C = 100^\circ\text{C}$		9	
Pulsed Drain Current ¹		I_{DM}	48	
Avalanche Current		I_{AS}	12	
Avalanche Energy	$L = 0.1\text{mH}$, $I_{AS}=12\text{A}$, $R_G=25\Omega$	E_{AS}	7.2	mJ
Repetitive Avalanche Energy ²	$L = 0.05\text{mH}$	E_{AR}	3.6	
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	21	W
	$T_C = 100^\circ\text{C}$		8.3	
Power Dissipation	$T_A = 25^\circ\text{C}$	P_D	2.5	W
	$T_A = 100^\circ\text{C}$		1	
Operating Junction & Storage Temperature Range		$T_{j, T_{stg}}$	-55 to 150	$^\circ\text{C}$

100% UIS testing in condition of $V_D=40\text{V}$, $L=0.1\text{mH}$, $V_G=10\text{V}$, $I_L=7\text{A}$, Rated $V_{DS}=80\text{V}$ N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		6	$^\circ\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		50	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³50°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	80			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.0	1.7	3.0	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 64V, V _{GS} = 0V			1	μA
		V _{DS} = 60V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 5V, V _{GS} = 10V	12			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 6A		55	65	mΩ
		V _{GS} = 5V, I _D = 4A		68	85	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 6A		12		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 30V, f = 1MHz		1110		pF
Output Capacitance	C _{OSS}			60		
Reverse Transfer Capacitance	C _{rss}			51		
Total Gate Charge ^{1,2}	Q _g	V _{DS} = 40V, V _{GS} = 10V, I _D = 6A		15		nC
Gate-Source Charge ^{1,2}	Q _{gs}			1.7		
Gate-Drain Charge ^{1,2}	Q _{gd}			4.1		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = 40V, I _D = 1A, V _{GS} = 10V, R _{GS} = 6Ω		10		nS
Rise Time ^{1,2}	t _r			8		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			18		
Fall Time ^{1,2}	t _f			6		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)						
Continuous Current	I _S				12	A
Pulsed Current ³	I _{SM}				48	
Forward Voltage ¹	V _{SD}	I _F = 6A, V _{GS} = 0V			1.2	V

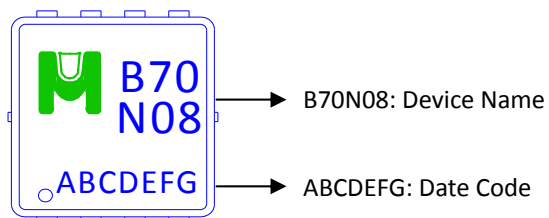
¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

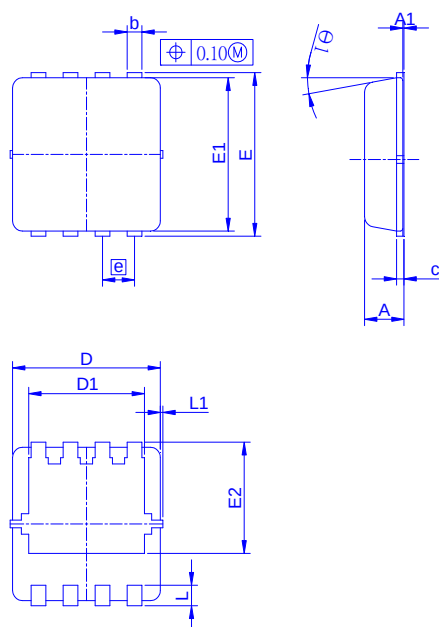
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB70N08V for EDFN 3 x 3



Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	D1	E	E1	E2	e	L	L1	θ1
Min.	0.65	0	0.20	0.10	2.90	2.15	3.10	2.90	1.53	0.55	0.25	-	0°
Typ.	0.75	-	0.30	0.15	3.00	2.45	3.20	3.00	1.97	0.65	0.40	0.075	10°
Max.	0.90	0.05	0.40	0.25	3.30	2.74	3.50	3.30	2.59	0.75	0.60	0.150	14°

Recommended minimum pads

