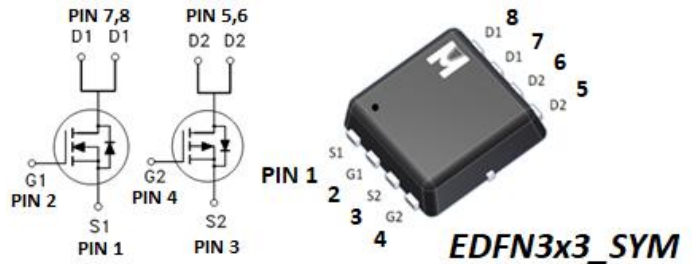


N-Channel + P-Channel Logic Level Enhancement Mode Field Effect Transistor

•Product Summary:

	N-CH	P-CH
BVDSS	60V	-60V
$R_{DS(on)} (MAX.) @ V_{GS}=10V$	60.0mΩ	90.0mΩ
$R_{DS(on)} (MAX.) @ V_{GS}=4.5V$	85.0mΩ	135.0mΩ
$I_D @ T_C=25^{\circ}C$	13.0A	-10.0A
$I_D @ T_A=25^{\circ}C$	4.0A	-4.0A

• Pin Description:



N + P Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

• ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}C$ Unless Otherwise Noted)



PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
			N-CH	P-CH	
Gate-Source Voltage		V_{GS}	± 20	± 20	V
Continuous Drain Current	$T_C = 25^{\circ}C$	I_D	13	-10	A
	$T_C = 100^{\circ}C$		8	-6	
Continuous Drain Current	$T_A = 25^{\circ}C$	I_D	4	-4	
	$T_A = 70^{\circ}C$		3	-3	
Pulsed Drain Current ¹		I_{DM}	52	-40	
Avalanche Current		I_{AS}	25	-26	mJ
Avalanche Energy		EAS	31.3	33.8	
Repetitive Avalanche Energy ²		EAR	15.6	16.9	W
Power Dissipation	$T_C = 25^{\circ}C$	P_D	16.7	16.7	
	$T_C = 100^{\circ}C$		6.7	6.7	W
Power Dissipation	$T_A = 25^{\circ}C$	P_D	2.3	2.3	
	$T_A = 70^{\circ}C$		1.5	1.5	W
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		$^{\circ}C$

• 100% UIS testing in condition of $V_D=30V$, $L=0.1mH$, $V_G=10V$, $I_L=15A$, Rated $V_{DS}=60V$ N-CH

• 100% UIS testing in condition of $V_D=30V$, $L=0.1mH$, $V_G=10V$, $I_L=16A$, Rated $V_{DS}=-60V$ P-CH

•THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM		UNIT
			N-CH	P-CH	
Junction-to-Case	$R_{\theta JC}$		7.5	7.5	$^{\circ}C/W$
Junction-to-Ambient ³	$R_{\theta JA}$		55	55	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $< 1\%$

³ $55^{\circ}C / W$ when mounted on a 1 in² pad of 2 oz copper.

⁴Guarantee by Engineering test

▪ N-CH_ELECTRICAL CHARACTERISTICS (T_j = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250uA	60			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	1	1.6	3	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 48V, V _{GS} = 0V			1	uA
		V _{DS} =42V, V _{GS} =0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	13			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 10A		50	60	mΩ
		V _{GS} = 4.5V, I _D = 8A		60	85	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 10A		13		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 30V, f = 1MHz		602		pF
Output Capacitance ⁵	C _{OSS}			72		
Reverse Transfer Capacitance ⁵	C _{rss}			40		
Gate Resistance ^{4,5}	R _g	f = 1MHz		1.3		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 30V, V _{GS} = 10V, I _D = 10A		15.3		nC
	Q _g (V _{GS} =4.5V)			8.0		
Gate-Source Charge ^{1,2,5}	Q _{gs}			2.1		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			4.9		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 30V, V _{GS} = 10V, I _D = 5A , R _g = 6Ω		5.7		nS
Rise Time ^{1,2,5}	t _r			6.7		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			14.2		
Fall Time ^{1,2,5}	t _f			1.8		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				13	A
Pulsed Current ³	I _{SM}				52	
Forward Voltage ^{1,4}	V _{SD}	I _F = I _S , V _{GS} = 0V			1.3	V
Reverse Recovery Time ⁵	t _{rr}	I _F = I _S , dI _F /dt = 100A / uS		19.2		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			2.16		A
Reverse Recovery Charge ⁵	Q _{rr}			18.7		nC

¹ Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

² Independent of operating temperature.

³ Pulse width limited by maximum junction temperature.

⁴ Guarantee by FT test Item

⁵ Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪ N-CH_TYPICAL CHARACTERISTICS

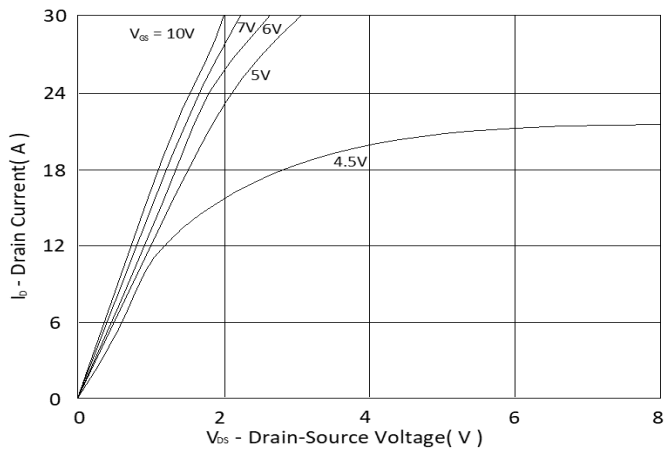


Fig.1 Typical Output Characteristics

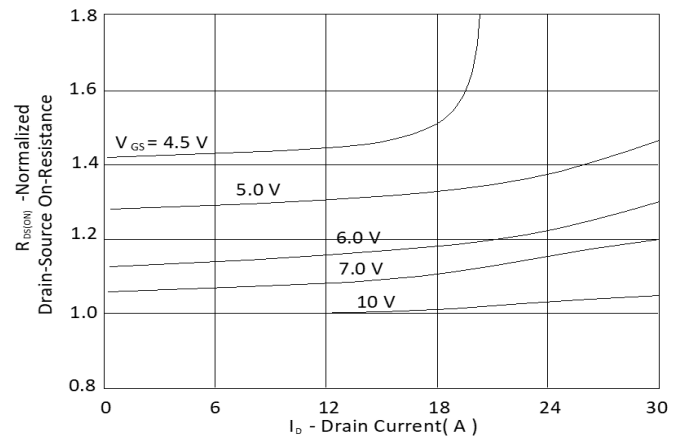


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

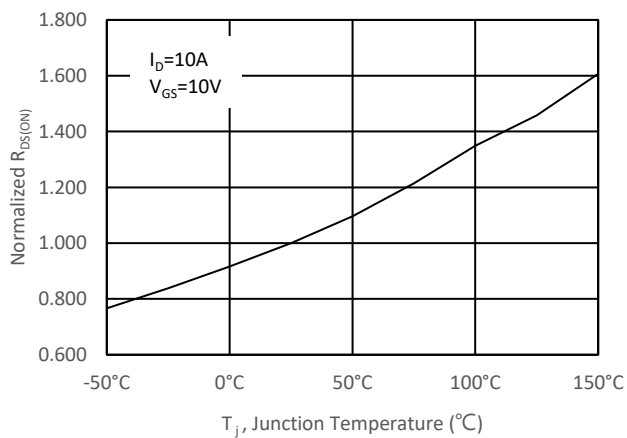


Fig.3 Normalized On-Resistance v.s. Junction Temperature

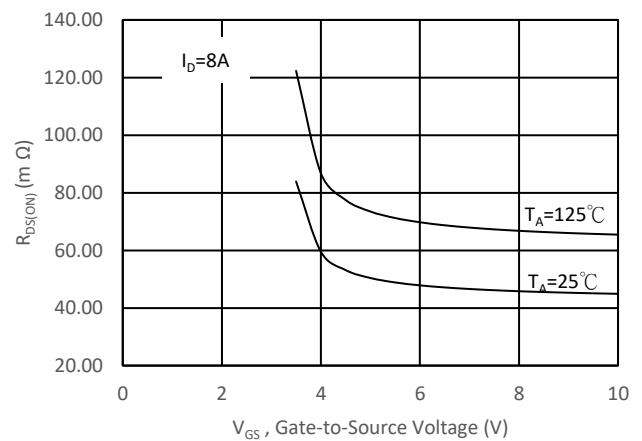


Fig.4 On-Resistance v.s. Gate Voltage

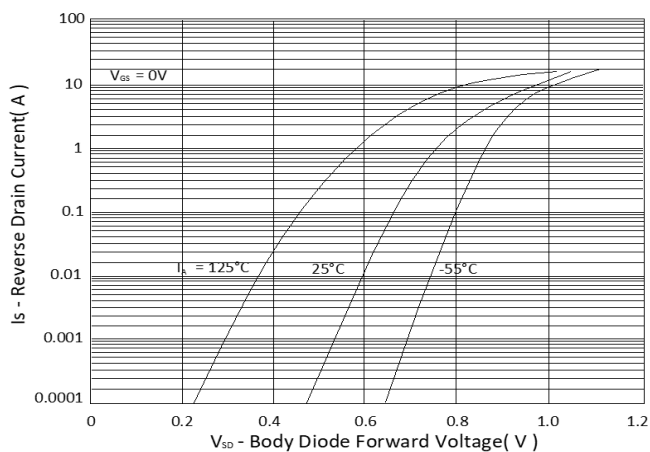


Fig.5 Forward Characteristic of Reverse Diode

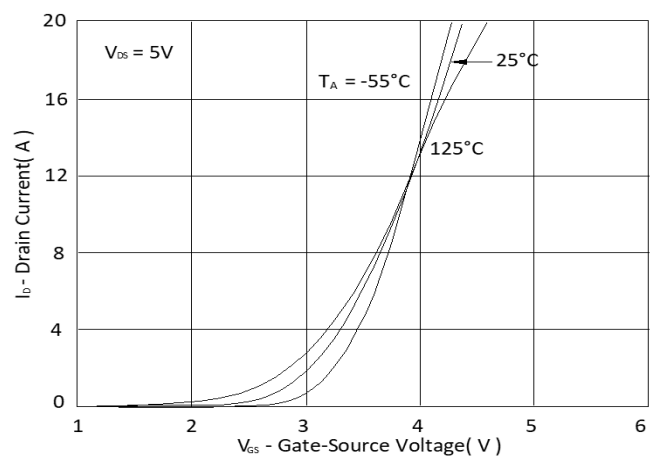


Fig.6 Transfer Characteristics

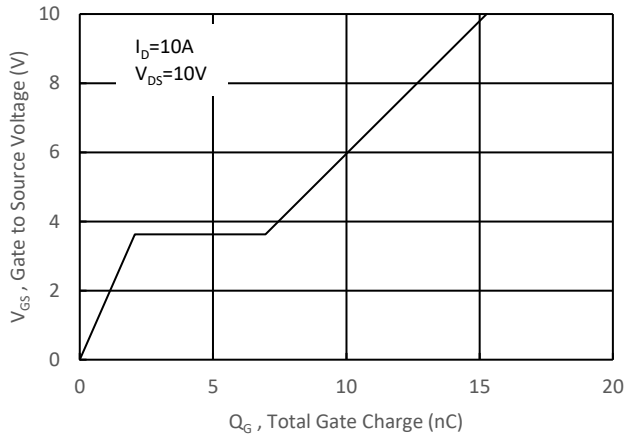


Fig.7 Gate Charge Characteristics

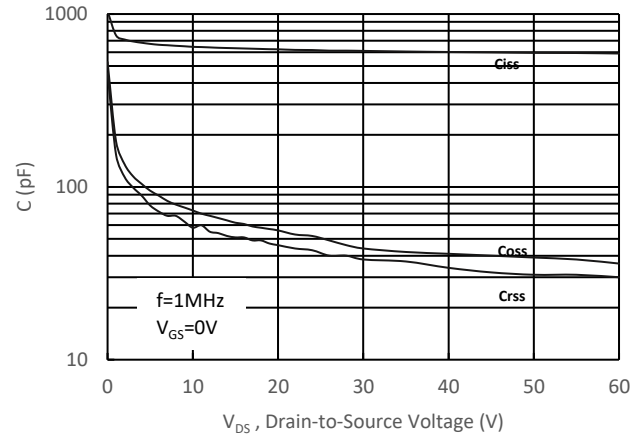


Fig.8 Typical Capacitance Characteristics

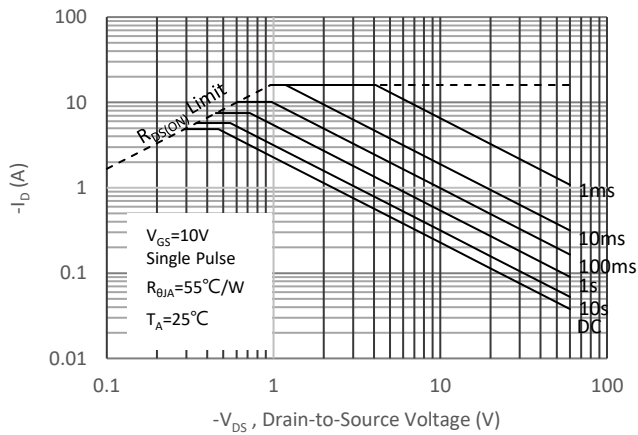


Fig.9. Maximum Safe Operating Area

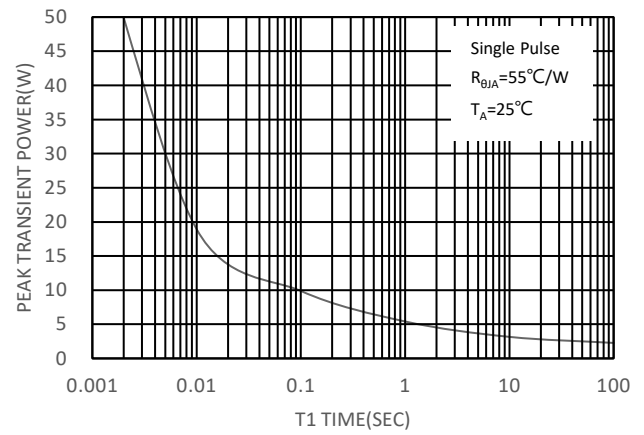


Fig.10. Single Pulse Maximum Power Dissipation

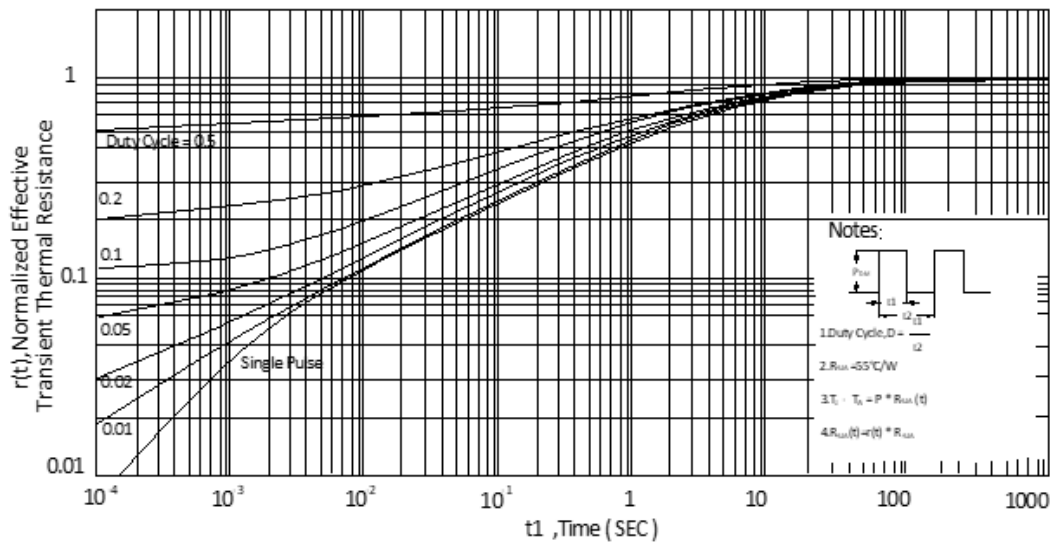


Fig.11. Effective Transient Thermal Impedance

▪ P-CH_ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250uA	-60			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250uA	-1	-1.6	-3	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = -48V, V _{GS} = 0V			1	uA
		V _{DS} =-42V, V _{GS} =0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	-10			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 8A		78	90	mΩ
		V _{GS} = 4.5V, I _D = 6A		100	135	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 8A		9		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = -30V, f = 1MHz		945		pF
Output Capacitance ⁵	C _{oss}			67		
Reverse Transfer Capacitance ⁵	C _{rss}			56		
Gate Resistance ^{4,5}	R _g	f = 1MHz		5.1		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = -30V, V _{GS} = -10V, I _D = -8A		20.2		nC
	Q _g (V _{GS} =4.5V)			10.5		
Gate-Source Charge ^{1,2,5}	Q _{gs}			2.1		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			4.9		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = -30V, V _{GS} = -10V, I _D = -5A , R _g = 6Ω		6.2		nS
Rise Time ^{1,2,5}	t _r			8.2		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			45.4		
Fall Time ^{1,2,5}	t _f			29.0		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				-10	A
Pulsed Current ³	I _{SM}				-40	
Forward Voltage ^{1,4}	V _{SD}	I _F = I _S , V _{GS} = 0V			-1.3	V
Reverse Recovery Time ⁵	t _{rr}	I _F = I _S , dI _F /dt = 100A / uS		19.5		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			2.47		A
Reverse Recovery Charge ⁵	Q _{rr}			19.0		nC

¹ Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

² Independent of operating temperature.

³ Pulse width limited by maximum junction temperature.

⁴ Guarantee by FT test Item

⁵ Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.



▪ P-CH_TYPICAL CHARACTERISTICS

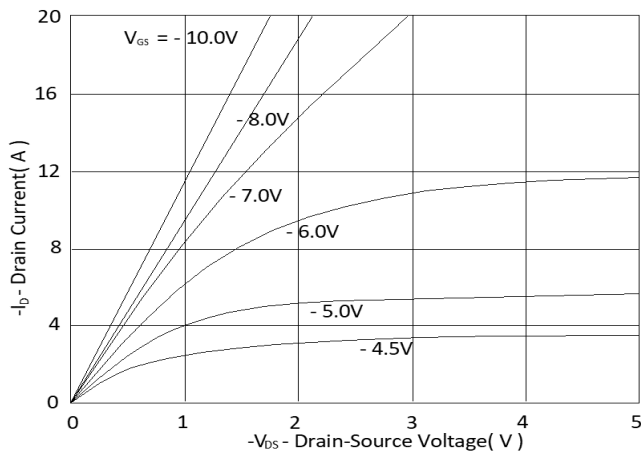


Fig.1 Typical Output Characteristics

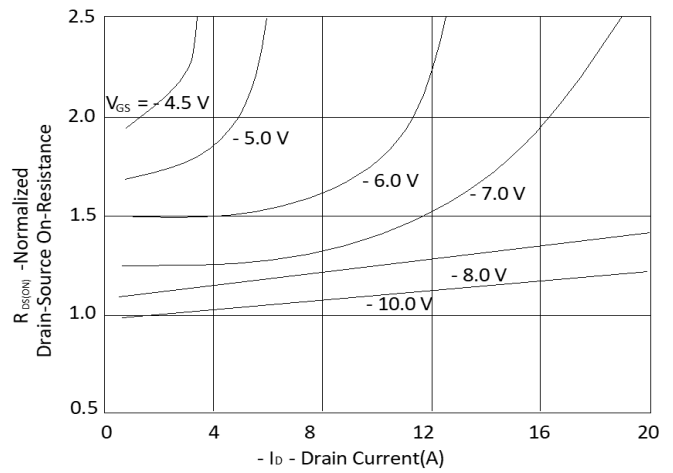


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

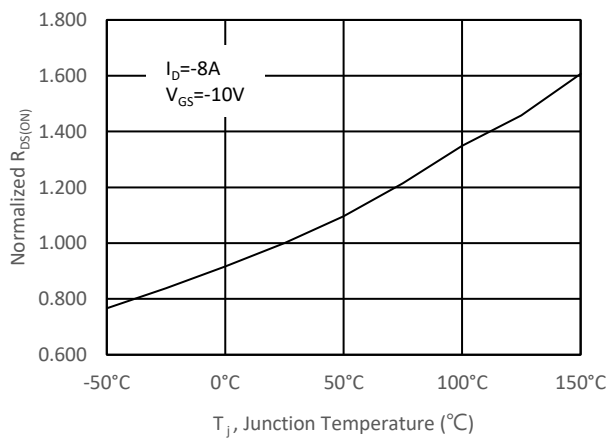


Fig.3 Normalized On-Resistance v.s. Junction Temperature

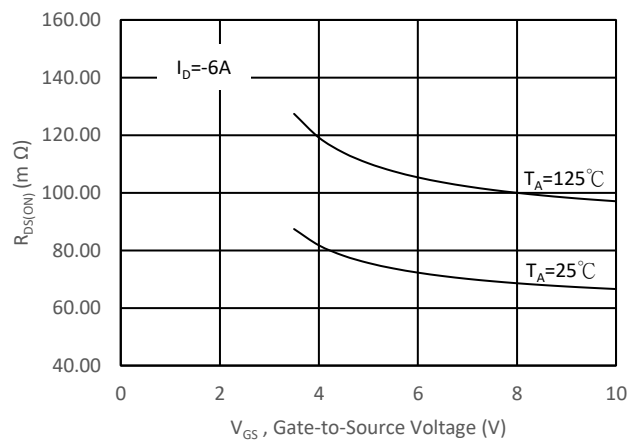


Fig.4 On-Resistance v.s. Gate Voltage

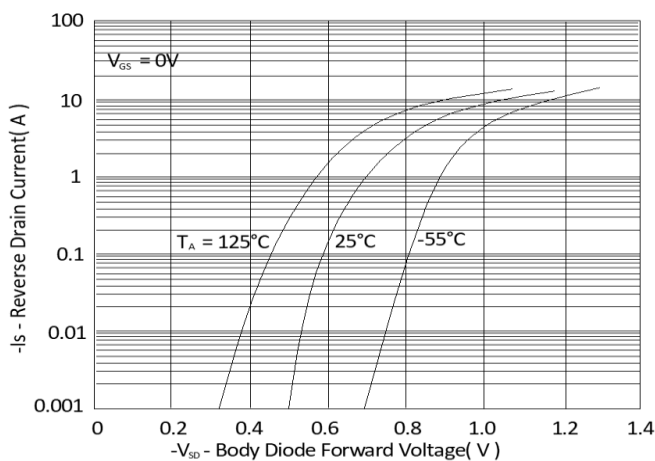


Fig.5 Forward Characteristic of Reverse Diode

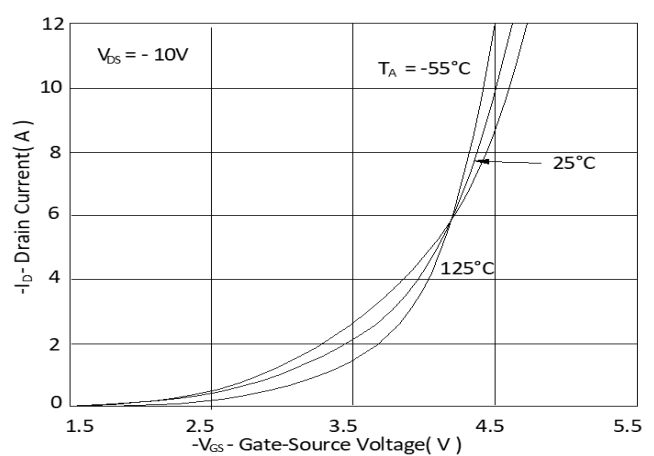


Fig.6 Transfer Characteristics

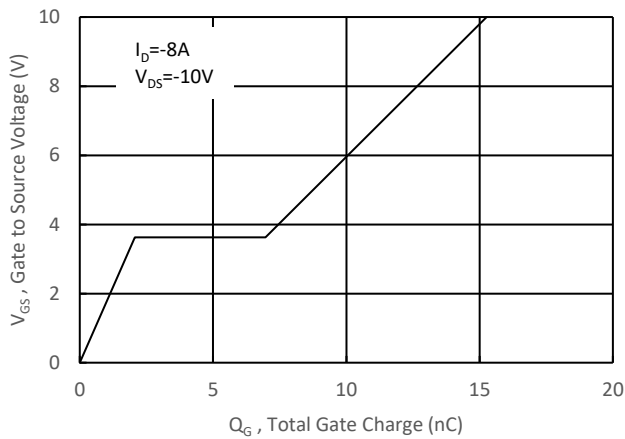


Fig.7 Gate Charge Characteristics

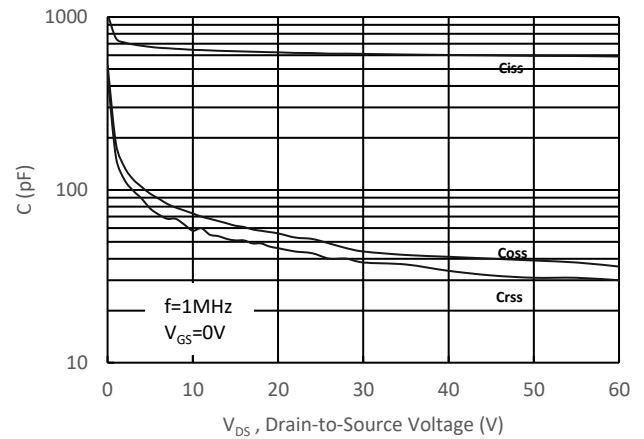


Fig.8 Typical Capacitance Characteristics

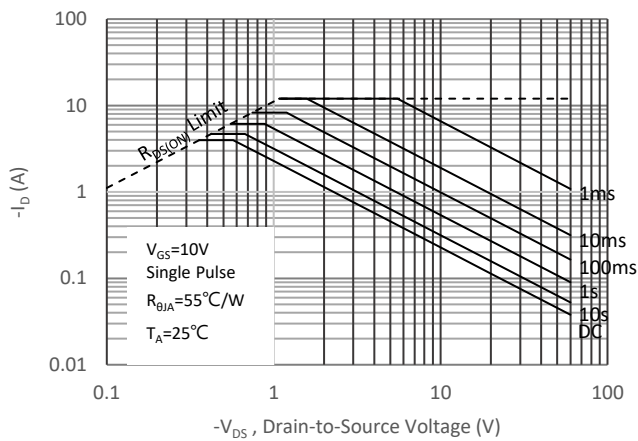


Fig 9. Maximum Safe Operating Area

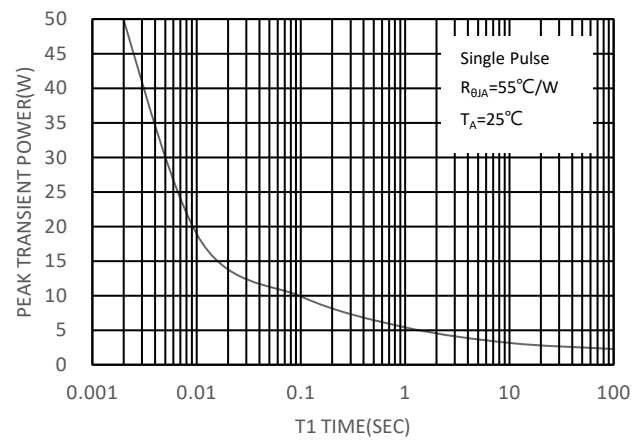


Fig 10. Single Pulse Maximum Power Dissipation

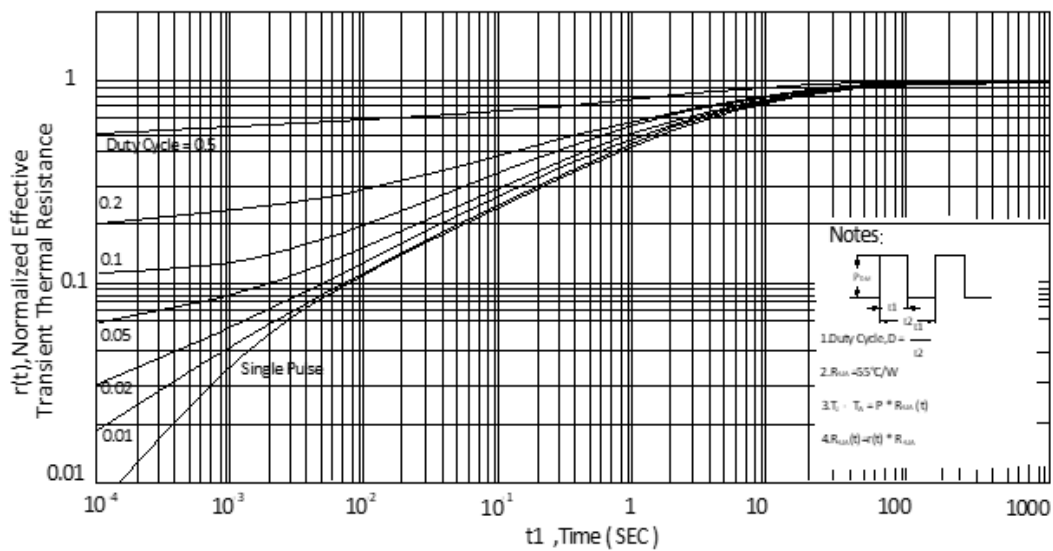


Fig 11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMB60C06V for EDFN 3x3



B60C06: Device Name

ABCDEFGH: Date Code

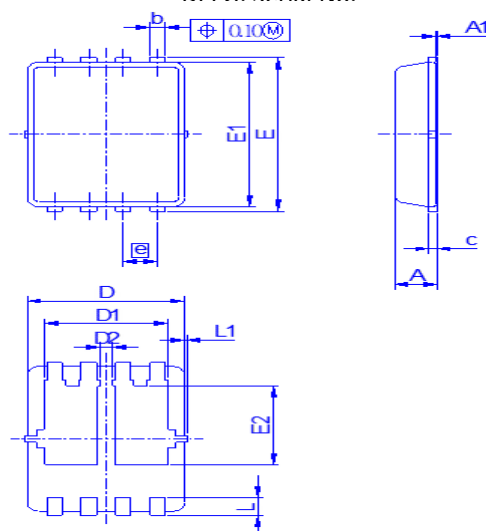
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DFFG: Serial No.

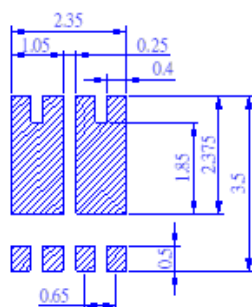
Outline Drawing



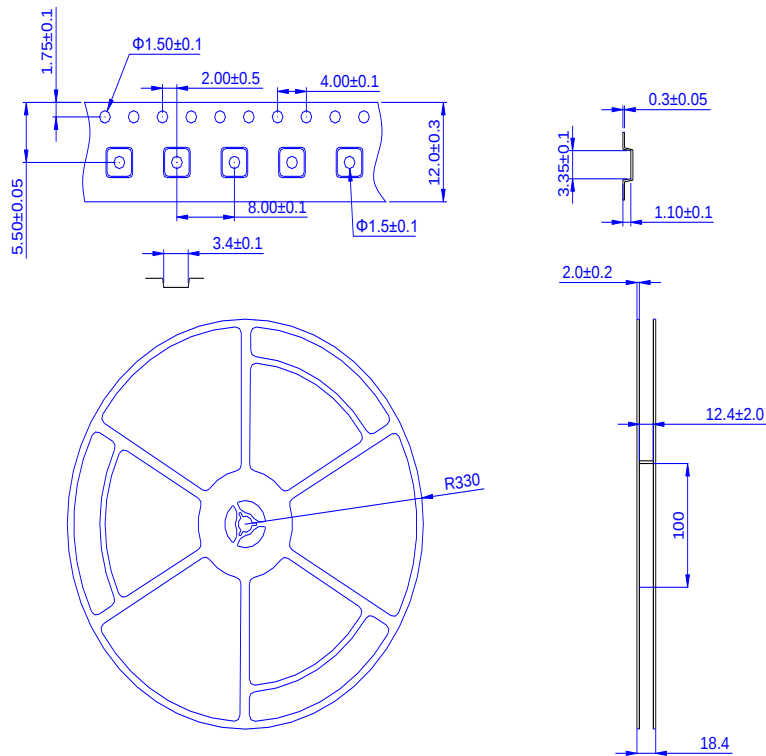
Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	e	L
Min.	0.65	0	0.2	0.1	2.9	2.15	0.28	3.1	2.9	1.53	0.55	0.3
Typ.	0.75	-	0.3	0.15	3	2.47	0.38	3.2	3	1.81	0.65	0.4
Max.	0.9	0.05	0.4	0.25	3.3	2.75	-	3.5	3.3	1.98	0.75	0.5

Dimension	L1	θ1
Min.	-	0°
Typ.	0.075	10°
Max.	0.15	14°

Footprint



◆ Tape&Reel Information:5000pcs/Reel(Dimension in millimeter)



產品別	EDFN 3x3
Reel尺寸	13"
編帶方式	FEED DIRECTION
前空格	50
後空格	50
裝箱數	
滿捲數量	5K
捲/內盒比	01:01
內盒滿箱數	5K
內/外箱比	10:01
外箱滿箱數	50K