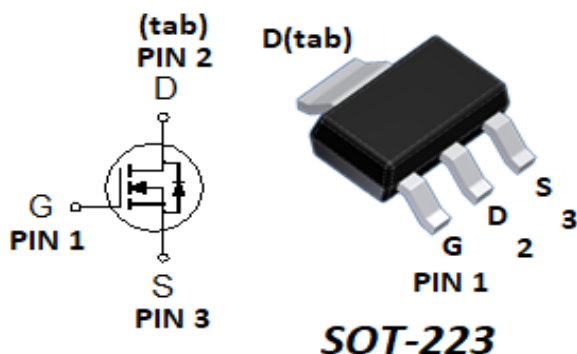


Single N-Channel Logic Level Enhancement Mode Field Effect Transistor

• Product Summary:

	N-CH
BV_{DSS}	100V
$R_{DS(on)} (MAX.) @ V_{GS}=10V$	50mΩ
$R_{DS(on)} (MAX.) @ V_{GS}=4.5V$	70mΩ
$I_D @ T_C=25^{\circ}C$	8.5A
$I_D @ T_A=25^{\circ}C$	5.0A

• Pin Description:



Single N Channel MOSFET

UIS, Rg 100% Tested

RoHS & Halogen Free & TSCA Compliant

• ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}C$ Unless Otherwise Noted)



PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^{\circ}C$	I_D	8.5	A
	$T_C = 100^{\circ}C$		5	
Continuous Drain Current	$T_A = 25^{\circ}C$	I_D	5	
	$T_A = 70^{\circ}C$		4	
Pulsed Drain Current ¹		I_{DM}	20	
Avalanche Current		I_{AS}	12	mJ
Avalanche Energy	$L = 0.1mH$	EAS	7.2	
Repetitive Avalanche Energy ²	$L = 0.05mH$	EAR	3.6	W
Power Dissipation	$T_C = 25^{\circ}C$	P_D	6.3	
	$T_C = 100^{\circ}C$		2.5	W
Power Dissipation	$T_A = 25^{\circ}C$	P_D	2.1	
	$T_A = 70^{\circ}C$		1.4	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	$^{\circ}C$

• 100% UIS testing in condition of $V_D=50V$, $L=0.1mH$, $V_G=10V$, $I_L=7A$, Rated $V_{DS}=100V$ N-CH

• THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Lead	$R_{\theta JC}$		20	$^{\circ}C/W$
Junction-to-Ambient ³	$R_{\theta JA}$		58.45	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $< 1\%$

³58.45 $^{\circ}C/W$ when mounted on a 1 in² pad of 2 oz copper.

⁴Guarantee by Engineering test

▪ ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	100			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1	2	3	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 80V, V _{GS} = 0V			1	μA
		V _{DS} =70V, V _{GS} =0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	8.5			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 7A		38	50	mΩ
		V _{GS} = 4.5V, I _D = 4A		54	70	
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 50V, f = 1MHz		3731		pF
Output Capacitance ⁵	C _{OSS}			86		
Reverse Transfer Capacitance ⁵	C _{rss}			48		
Gate Resistance ^{4,5}	R _g	f = 1MHz		1.1		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 50V, V _{GS} = 10V, I _D = 7A		76		nC
	Q _g (V _{GS} =4.5V)			37		
Gate-Source Charge ^{1,2,5}	Q _{gs}			11		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			20		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 50V, V _{GS} = 10V, I _D = 5A , R _g = 6Ω		15.2		nS
Rise Time ^{1,2,5}	t _r			13.2		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			91.8		
Fall Time ^{1,2,5}	t _f			27		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				8.5	A
Pulsed Current ³	I _{SM}				20	
Forward Voltage ^{1,4}	V _{SD}	I _F = I _S , V _{GS} = 0V			1.3	V
Reverse Recovery Time ⁵	t _{rr}	I _F = I _S , dI _F /dt = 100A / μS		41.3		nS
Reverse Recovery Charge ⁵	Q _{rr}			77.1		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.



▪ TYPICAL CHARACTERISTICS

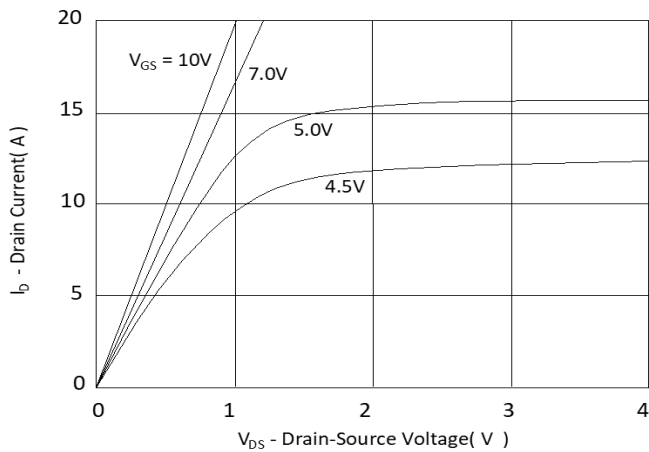


Fig.1 Typical Output Characteristics

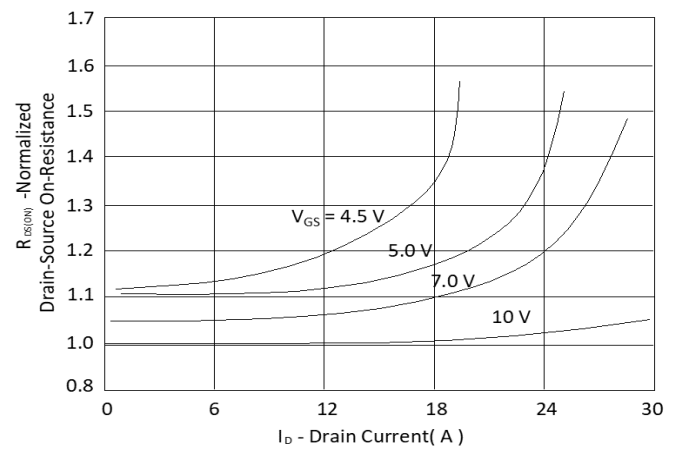


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

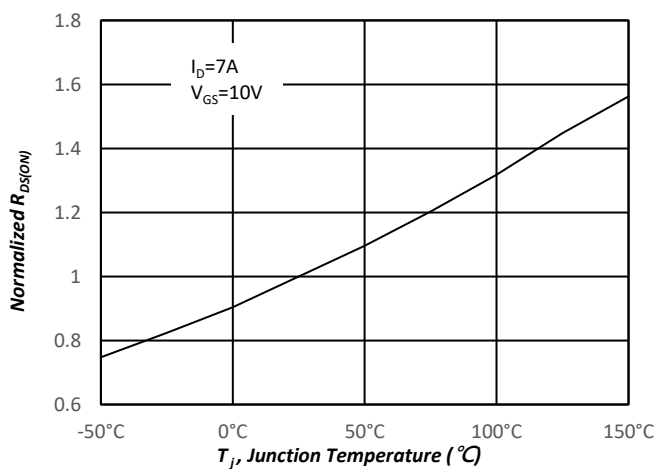


Fig.3 Normalized On-Resistance v.s. Junction Temperature

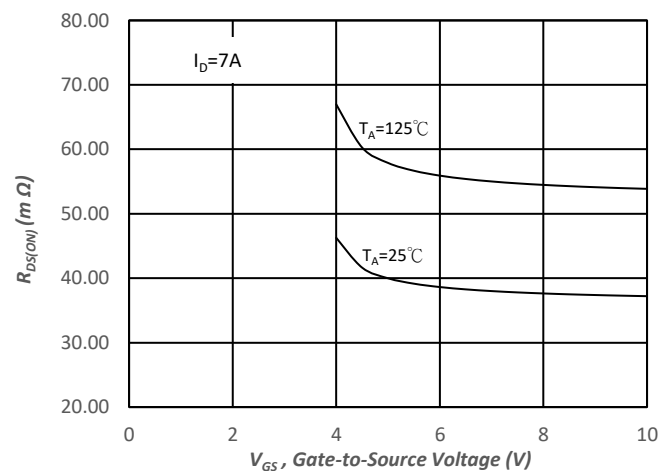


Fig.4 On-Resistance v.s. Gate Voltage

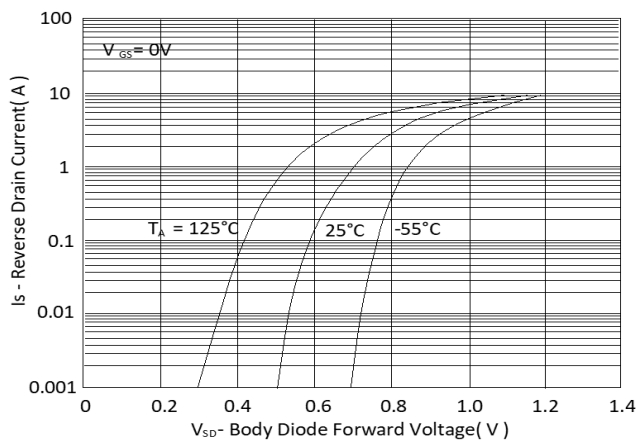


Fig.5 Forward Characteristic of Reverse Diode

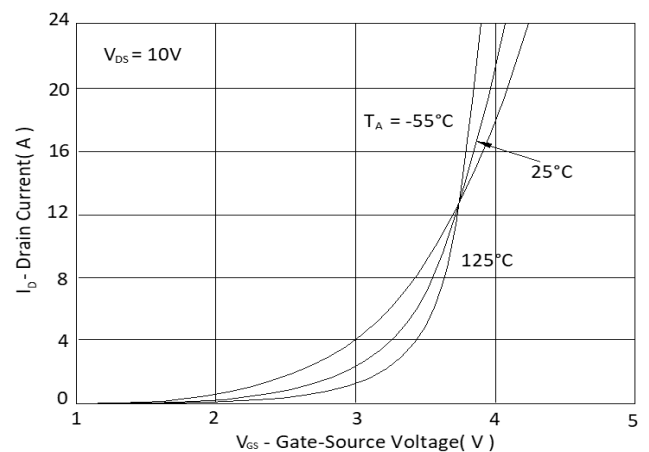


Fig.6 Transfer Characteristics

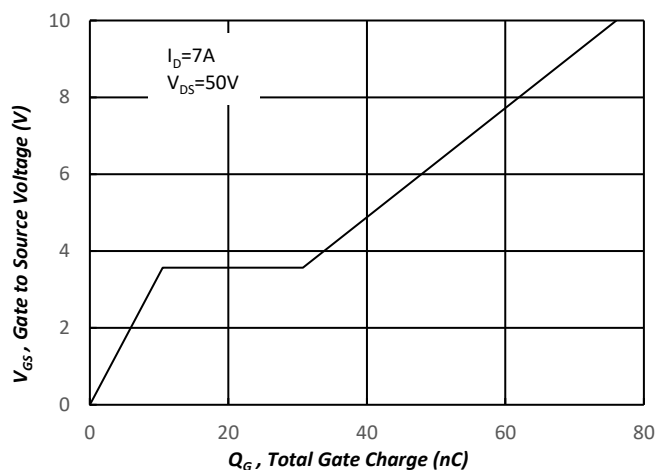


Fig.7 Gate Charge Characteristics

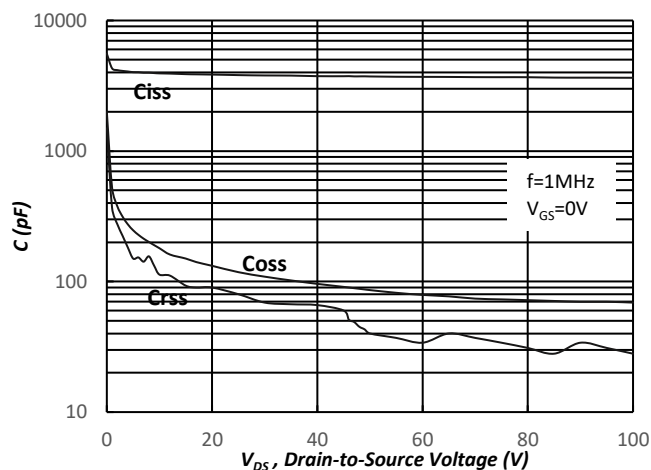


Fig.8 Typical Capacitance Characteristics

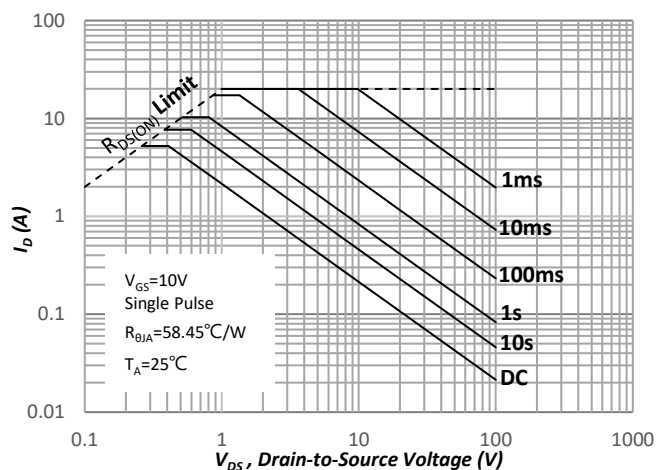


Fig.9. Maximum Safe Operating Area

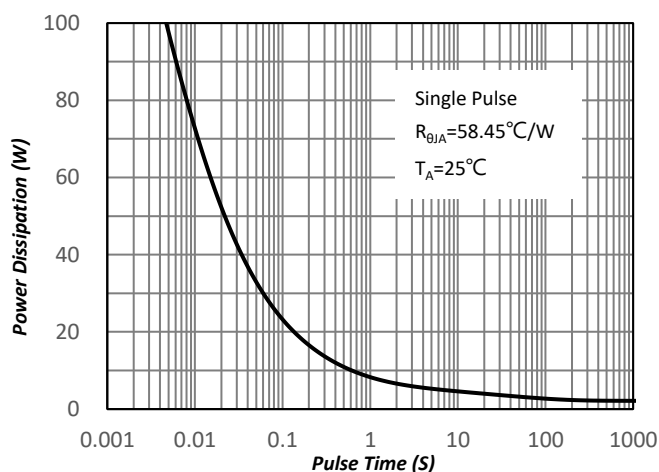


Fig.10. Single Pulse Maximum Power Dissipation

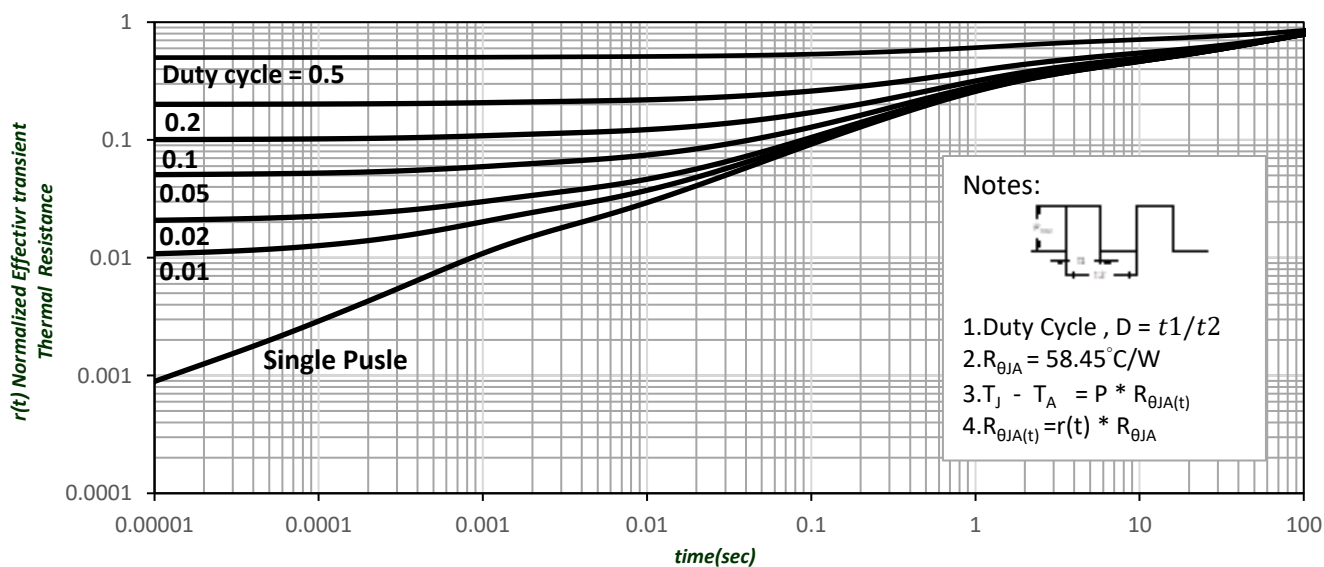
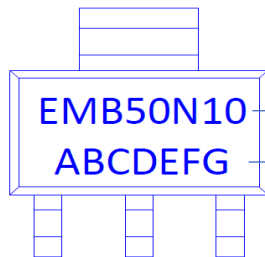


Fig.11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMB50N10Q for SOT-223



EMB50N10: Device Name

ABCDEFG: Date Code

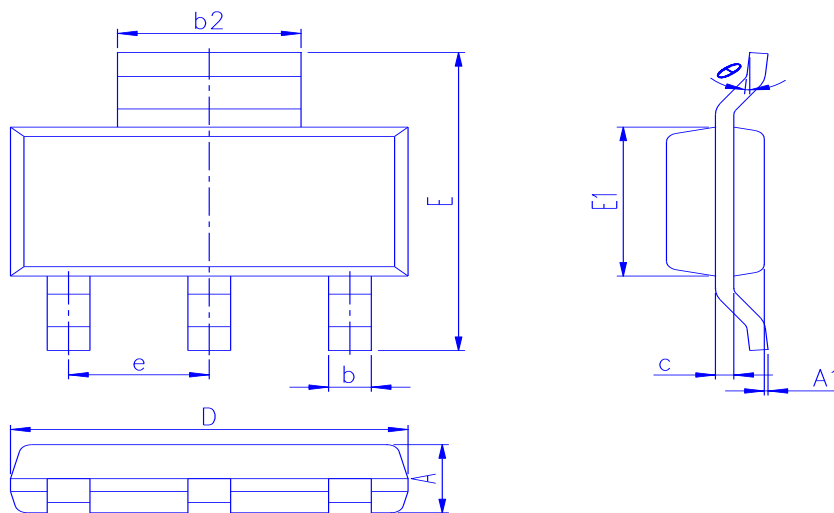
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

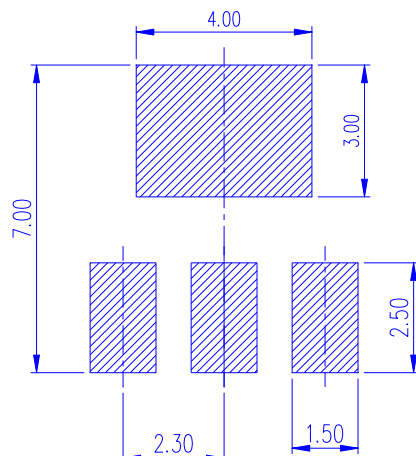
DEFG: Serial No.

Outline Drawing

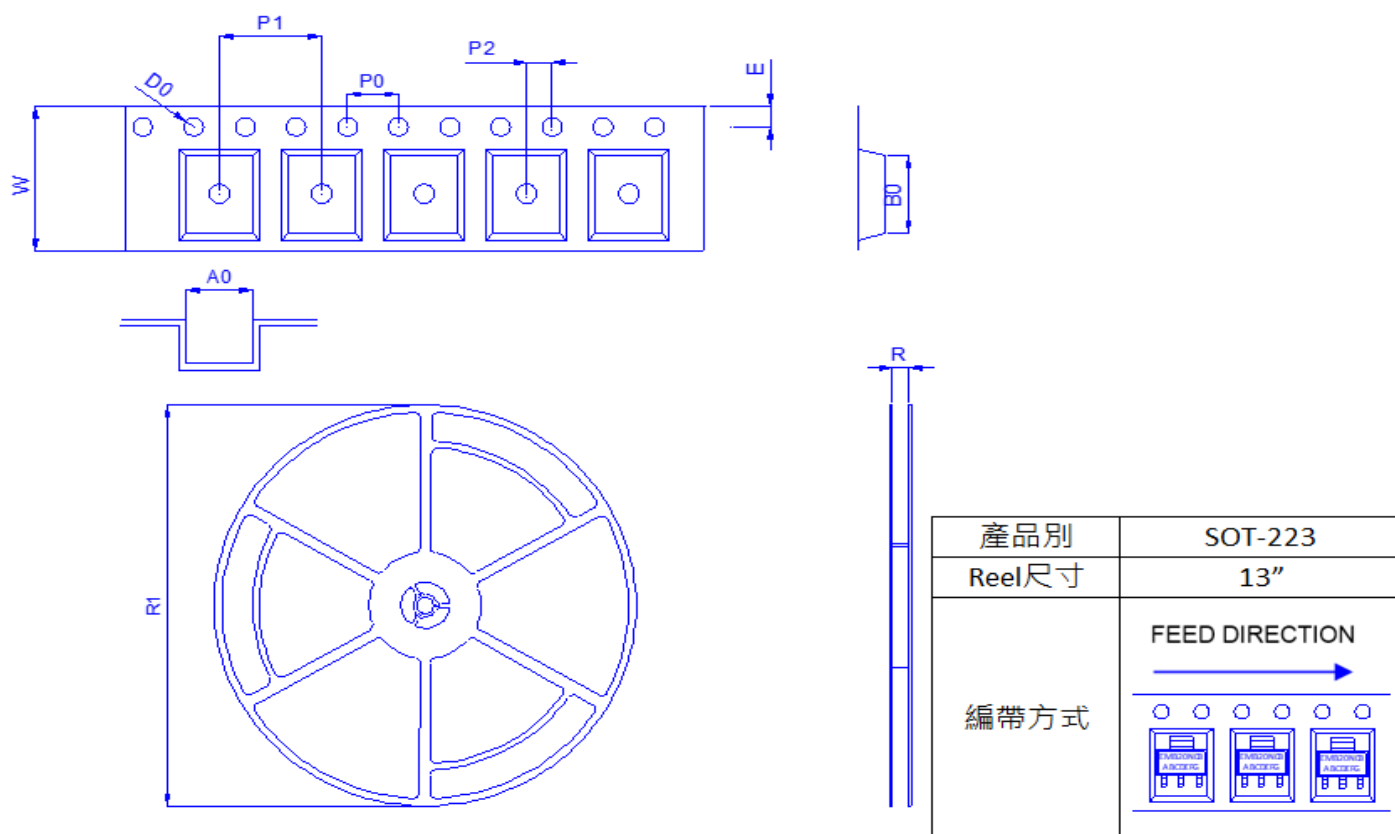


Dimension	E	b2	A1	θ	b	c	e	D	E1	A
Min	6.7	2.9	0.02	0°	0.6	0.23		6.3	3.3	1.4
Typ.	7	3	0.06		0.72	0.29	2.3	6.5	3.5	1.6
Max	7.3	3.1	0.1	10°	0.84	0.35		6.7	3.7	1.8

Footprint



◆ Tape&Reel Information:2500pcs/Reel



Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	6.7	7.3	1.5	1.75	2	4	8	2	12	16.5	330
±	0.4	0.3	0.1	0.1	0.3	0.1	0.1	0.1	0.3	3	2