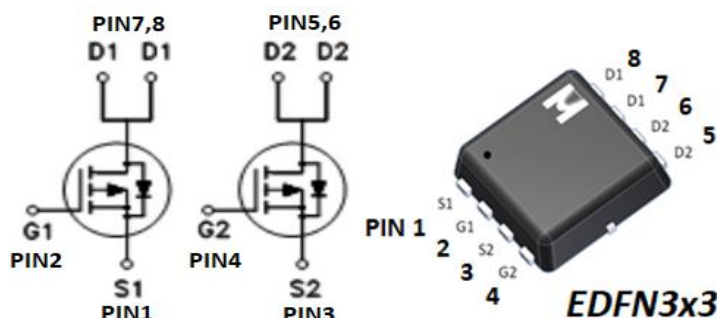


Dual P-Channel Logic Level Enhancement Mode Field Effect Transistor

•Product Summary:

	P-CH
BVDSS	30V
$R_{DS(on)} (MAX.) @ V_{GS}=10V$	35.0mΩ
$R_{DS(on)} (MAX.) @ V_{GS}=5V$	55.0mΩ
$I_D @ T_C=25^{\circ}C$	16.0A
$I_D @ T_A=25^{\circ}C$	5.0A

• Pin Description:



Dual P Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

•ABSOLUTE MAXIMUM RATINGS ($T_C = 25^{\circ}C$ Unless Otherwise Noted)



PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^{\circ}C$	I_D	-16	A
	$T_C = 100^{\circ}C$		-10	
Continuous Drain Current	$T_A = 25^{\circ}C$	I_D	-5	
	$T_A = 70^{\circ}C$		-4	
Pulsed Drain Current ¹		I_{DM}	-27.8	
Avalanche Current		I_{AS}	-26.0	mJ
Avalanche Energy	$L = 0.1mH$	EAS	33.8	
Repetitive Avalanche Energy ²	$L = 0.05mH$	EAR	16.9	
Power Dissipation	$T_C = 25^{\circ}C$	P_D	15.6	W
	$T_C = 100^{\circ}C$		6.3	
Power Dissipation	$T_A = 25^{\circ}C$	P_D	2	W
	$T_A = 70^{\circ}C$		1.3	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	$^{\circ}C$

•THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		8	$^{\circ}C/W$
Junction-to-Ambient ³	$R_{\theta JA}$		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle < 1%

³62.5 $^{\circ}C$ / W when mounted on a 1 in² pad of 2 oz copper.

⁴Guarantee by Engineering test

•ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250uA	-30			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250uA	-1	-1.5	-3	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = -24V, V _{GS} = 0V			-1	uA
		V _{DS} =-20V, V _{GS} =0V, T _J = 125 °C			-10	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = -10V, V _{GS} = -10V	-16			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = -10V, I _D = -6.5A		30	35	mΩ
		V _{GS} = -5V, I _D = -4.5A		43	55	
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = -15V, f = 1MHz		1050		pF
Output Capacitance ⁵	C _{oss}			115		
Reverse Transfer Capacitance ⁵	C _{rss}			100		
Gate Resistance ^{4,5}	R _g	f = 1MHz		4.0		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =-10V)	V _{DS} = -15V, V _{GS} = -10V, I _D = -6.5A		19.7		nC
	Q _g (V _{GS} =-5V)			10.0		
Gate-Source Charge ^{1,2,5}	Q _{gs}			2.4		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			3.9		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = -15V, V _{GS} = -10V, I _D = -1A , R _g = 6Ω		5.8		nS
Rise Time ^{1,2,5}	t _r			2.0		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			42.2		
Fall Time ^{1,2,5}	t _f			20.0		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				-16	A
Pulsed Current ³	I _{SM}				-28	
Forward Voltage ^{1,4}	V _{SD}	I _F = I _S , V _{GS} = 0V			-1.3	V
Reverse Recovery Time ⁵	t _{rr}	I _F = I _S , dI _F /dt = 100A / uS		10.1		nS
Reverse Recovery Charge ⁵	Q _{rr}			4.4		nC

¹ Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

² Independent of operating temperature.

³ Pulse width limited by maximum junction temperature.

⁴ Guarantee by FT test Item

⁵ Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.



▪ TYPICAL CHARACTERISTICS

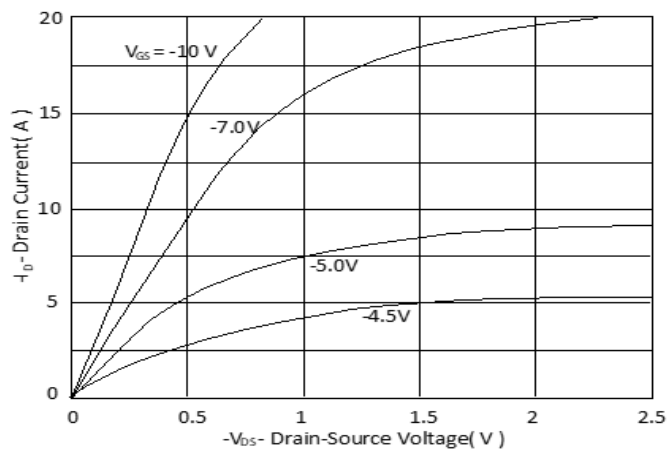


Fig.1 Typical Output Characteristics

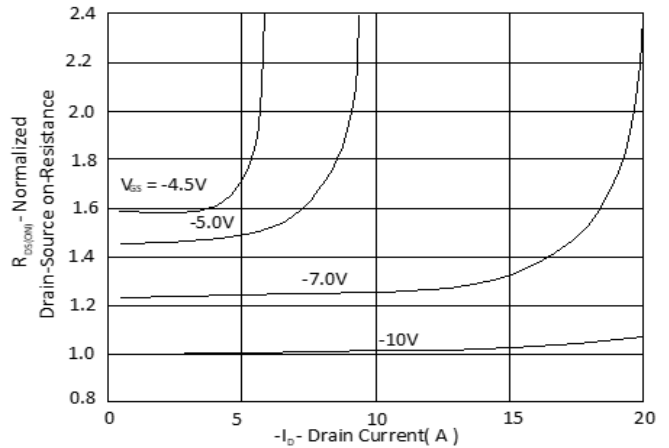


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

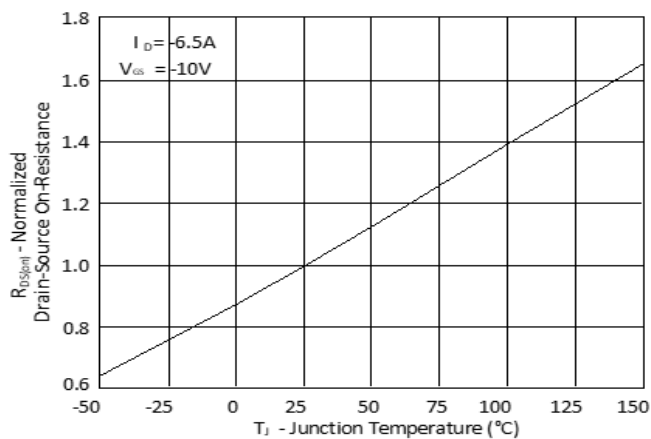


Fig.3 Normalized On-Resistance v.s. Junction Temperature

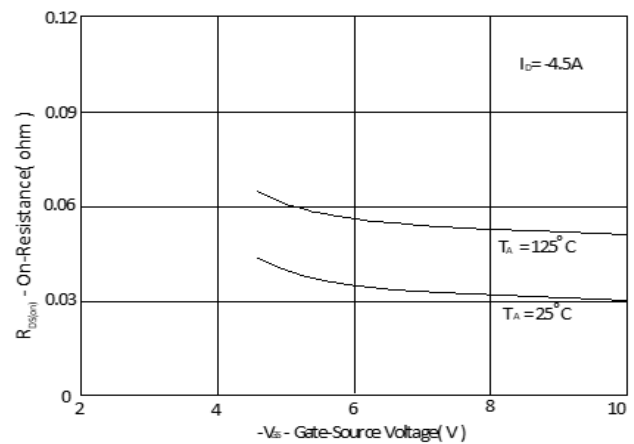


Fig.4 On-Resistance v.s. Gate Voltage

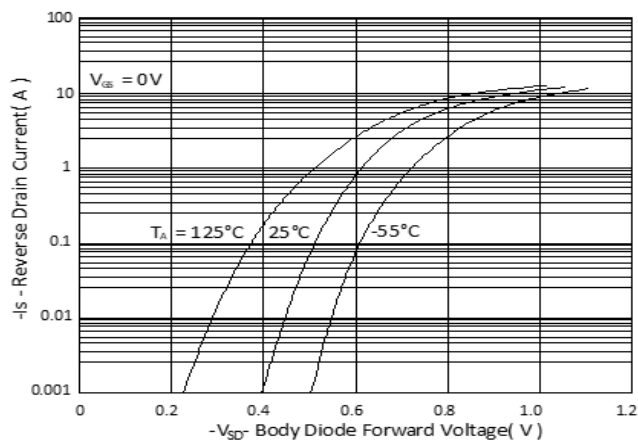


Fig.5 Forward Characteristic of Reverse Diode

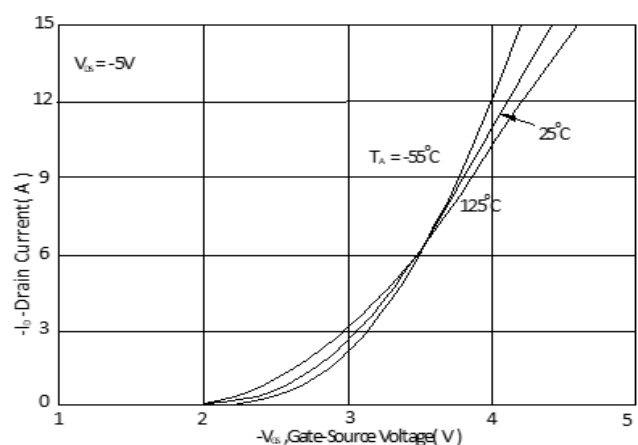


Fig.6 Transfer Characteristics

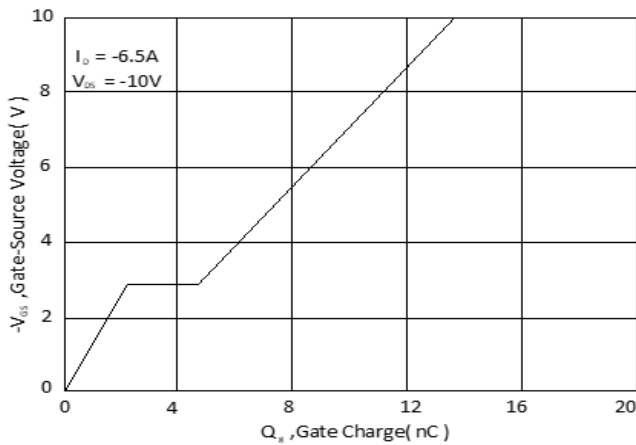


Fig.7 Gate Charge Characteristics

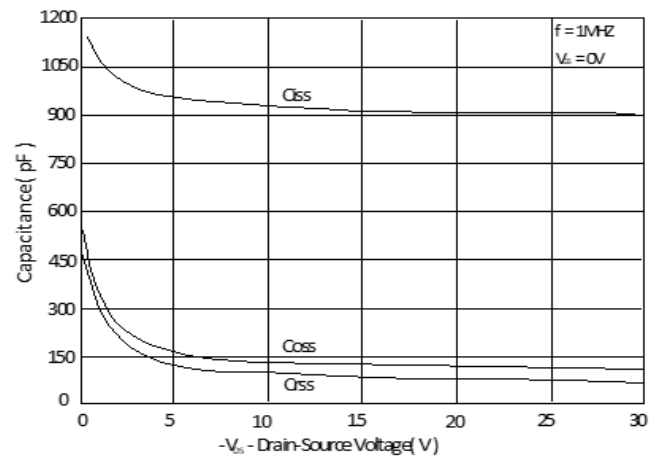


Fig.8 Typical Capacitance Characteristics

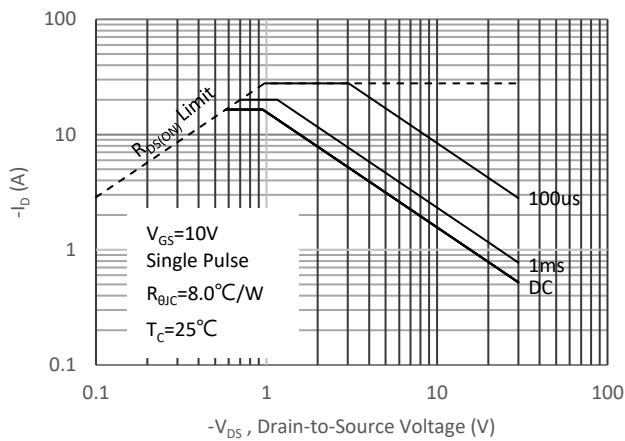


Fig.9. Maximum Safe Operating Area

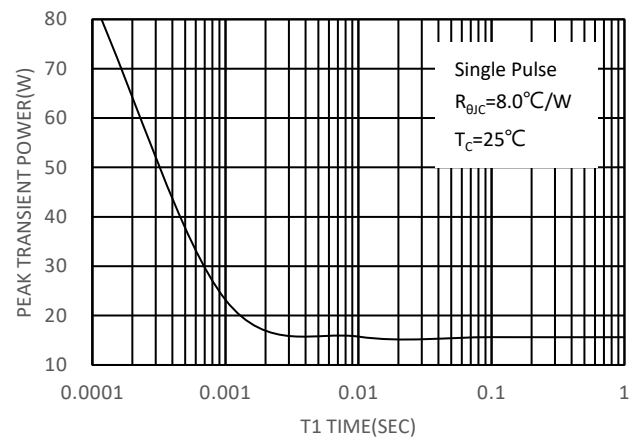


Fig.10. Single Pulse Maximum Power Dissipation

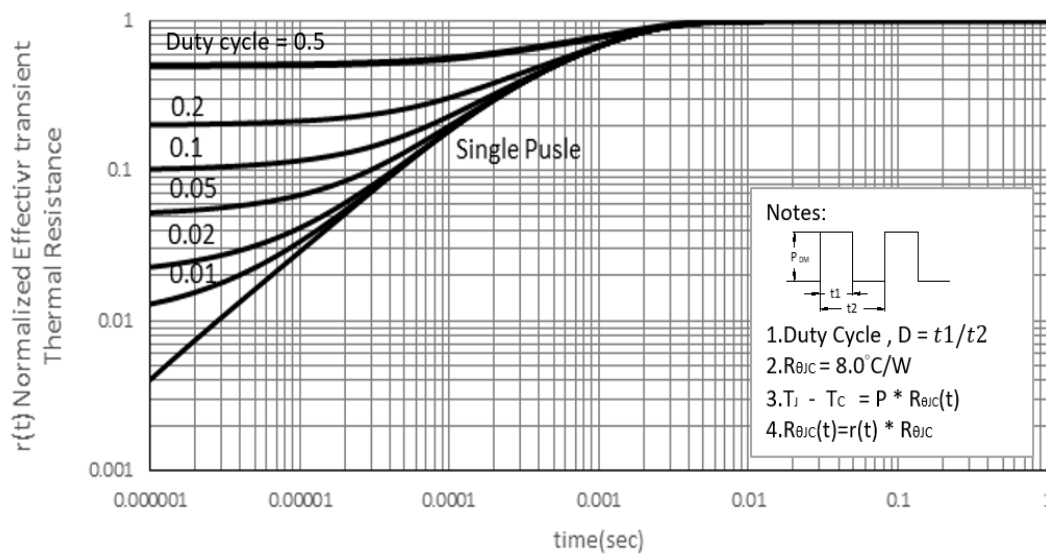
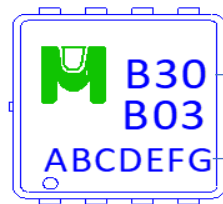


Fig.11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMB30B03V for EDFN 3x3



B30B03: Device Name

ABCDEFGH: Date Code

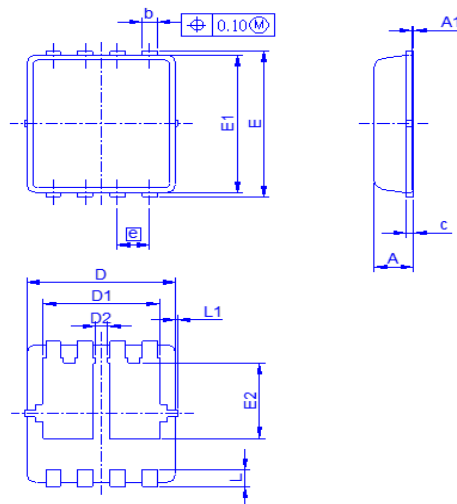
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

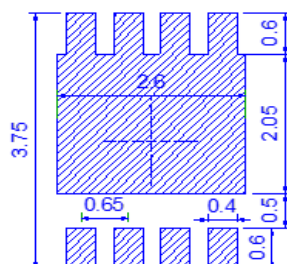
Outline Drawing



Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	e	L
Min.	0.65	0	0.2	0.1	2.9	2.15	0.28	3.1	2.9	1.53	0.55	0.3
Typ.	0.75	-	0.3	0.15	3	2.47	0.38	3.2	3	1.81	0.65	0.4
Max.	0.9	0.05	0.4	0.25	3.3	2.75	-	3.5	3.3	1.98	0.75	0.5

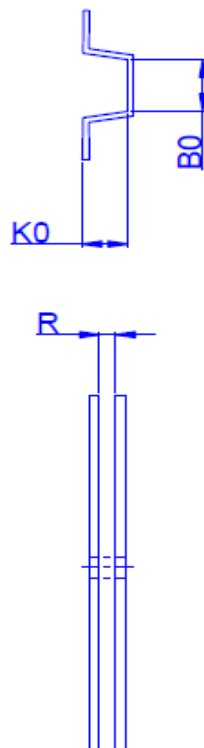
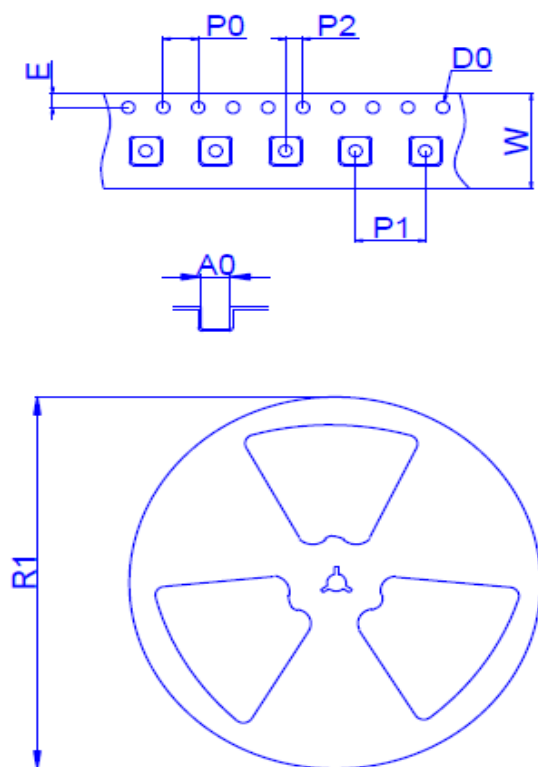
Dimension	L1	θ1
Min.	-	0°
Typ.	0.075	10°
Max.	0.15	14°

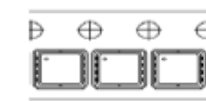
Footprint





◆ Tape&Reel Information:5000pcs/Reel



產品別	EDFN3X3
Reel 尺寸	13"
編帶 方式	FEED DIRECTION 

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	3.6	3.5	1.55	1.7	1.2	4	8	2	12	14	330
±	0.3	0.3	0.2	0.2	0.2	0.1	0.1	0.1	1	2	2