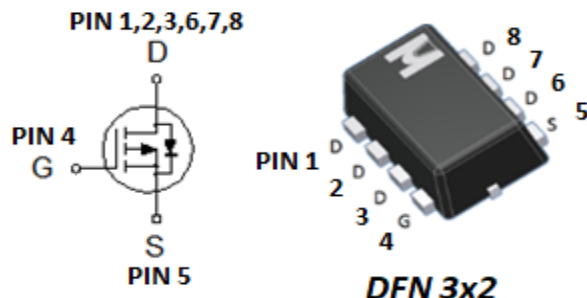


Single P-Channel Logic Level Enhancement Mode Field Effect Transistor

▪ Product Summary:

	P-CH
BVDSS	-30V
$R_{DS(on)} (MAX.) @ V_{GS} = -10V$	26.0mΩ
$R_{DS(on)} (MAX.) @ V_{GS} = -4.5V$	36.0mΩ
$I_D @ T_A = 25^{\circ}C$	-5.0A

▪ Pin Description:



Single P Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



▪ ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 25	V
Continuous Drain Current	$T_C = 25^{\circ}C$	I_D	-10	A
	$T_C = 100^{\circ}C$		-6	
Continuous Drain Current	$T_A = 25^{\circ}C$	I_D	-5	
	$T_A = 70^{\circ}C$		-4	
Pulsed Drain Current ¹		I_{DM}	-40	mJ
Avalanche Current		I_{AS}	-14	
Avalanche Energy	$L = 0.1mH$	EAS	9.8	mJ
Repetitive Avalanche Energy ²	$L = 0.05mH$	EAR	4.9	
Power Dissipation	$T_C = 25^{\circ}C$	P_D	4.2	W
	$T_C = 100^{\circ}C$		1.7	
Power Dissipation	$T_A = 25^{\circ}C$	P_D	2.5	W
	$T_A = 70^{\circ}C$		1.6	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	$^{\circ}C$

▪ THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case		$R_{\theta JC}$		30	$^{\circ}C/W$
Junction-to-Ambient ³	$t \leq 10s$	$R_{\theta JA}$		50	
	Steady-State	$R_{\theta JA}$		90	

¹ Pulse width limited by maximum junction temperature.

² Duty cycle $< 1\%$

³ The power dissipation P_D is based on $T_{J(MAX)} = 150^{\circ}C$, using $\leq 10s$ junction-to-ambient thermal resistance.

⁴ The value of $R_{\theta JA}$ is measured with mounted on a 1 in² pad of 2 oz copper.

▪ ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250uA	-30			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250uA	-0.8	-1.3	-1.9	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±30	uA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = -24V, V _{GS} = 0V			1	uA
		V _{DS} = -20V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = -5V, V _{GS} = -10V	-10			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = -10V, I _D = -5A		22	26	mΩ
		V _{GS} = -4.5V, I _D = -4A		31	36	
Forward Transconductance ¹	g _{fs}	V _{DS} = -5V, I _D = -5A		12		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = -15V, f = 1MHz		779		pF
Output Capacitance ⁵	C _{oss}			124		
Reverse Transfer Capacitance ⁵	C _{rss}			97		
Gate Resistance ^{4,5}	R _g	f = 1MHz		5.5		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = -15V, V _{GS} = -10V, I _D = -8A		14.9		nC
	Q _g (V _{GS} =4.5V)			8		
Gate-Source Charge ^{1,2,5}	Q _{gs}			1.7		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			3.3		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = -15V, V _{GS} = -10V, I _D = -5A , R _g = 6Ω		5.6		nS
Rise Time ^{1,2,5}	t _r			11.8		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			33.5		
Fall Time ^{1,2,5}	t _f			30.5		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				-10	A
Pulsed Current ³	I _{SM}				-40	
Forward Voltage ^{1,4}	V _{SD}	I _F = I _S , V _{GS} = 0V			-1.2	V
Reverse Recovery Time ⁵	t _{rr}	I _F = I _S , dI _F /dt = 400A / uS		11.6		nS
Reverse Recovery Charge ⁵	Q _{rr}			9.4		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.



▪ TYPICAL CHARACTERISTICS

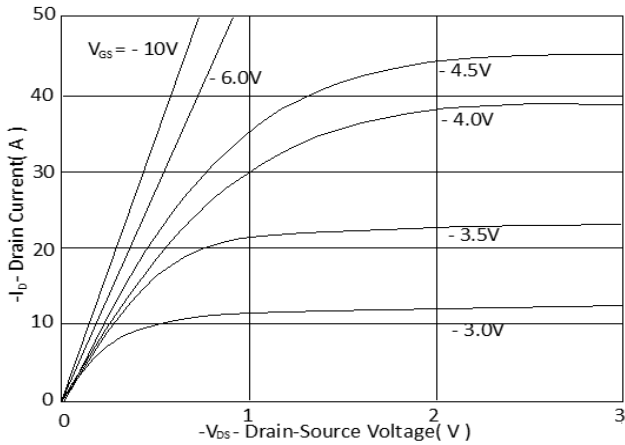


Fig.1 Typical Output Characteristics

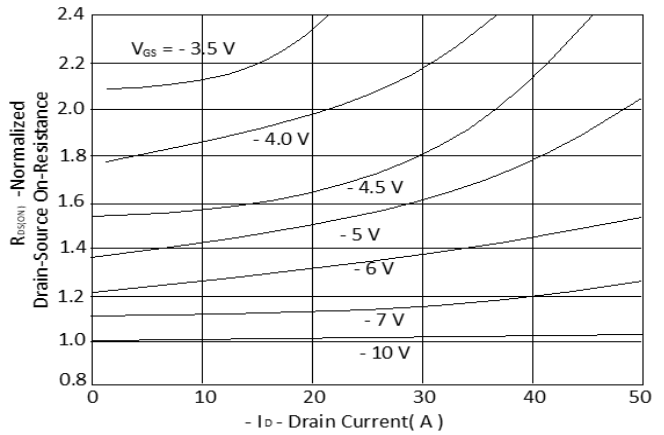


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

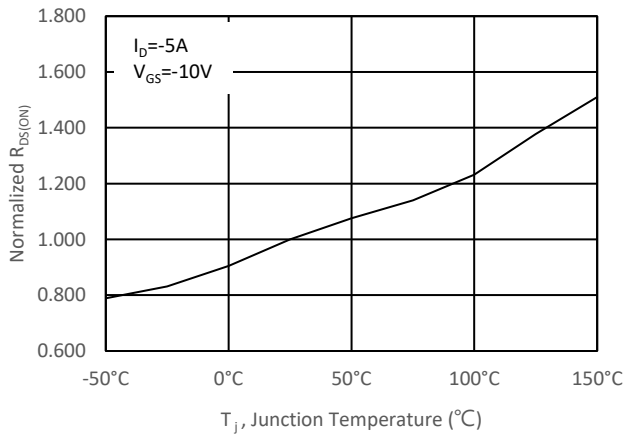


Fig.3 Normalized On-Resistance v.s. Junction Temperature

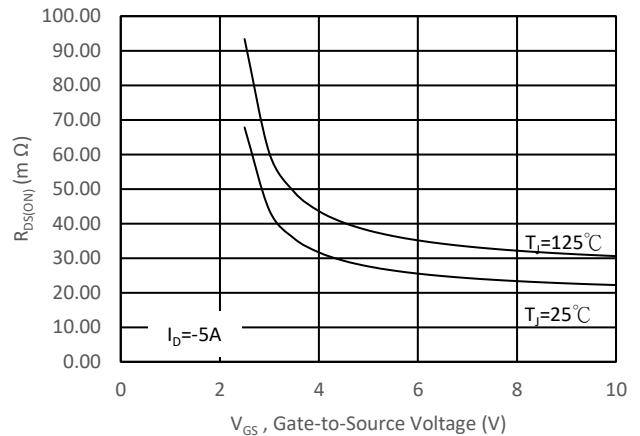


Fig.4 On-Resistance v.s. Gate Voltage

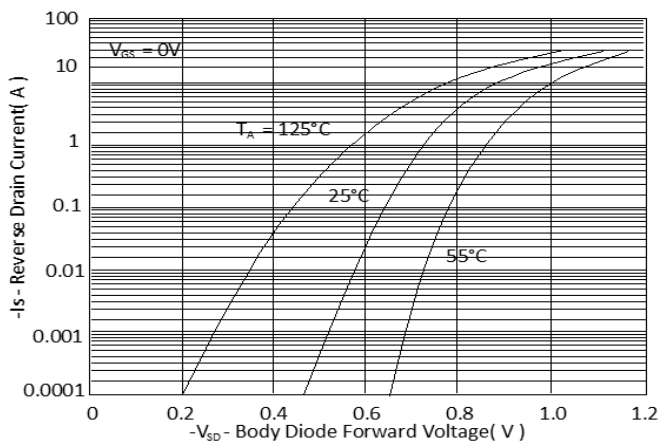


Fig.5 Forward Characteristic of Reverse Diode

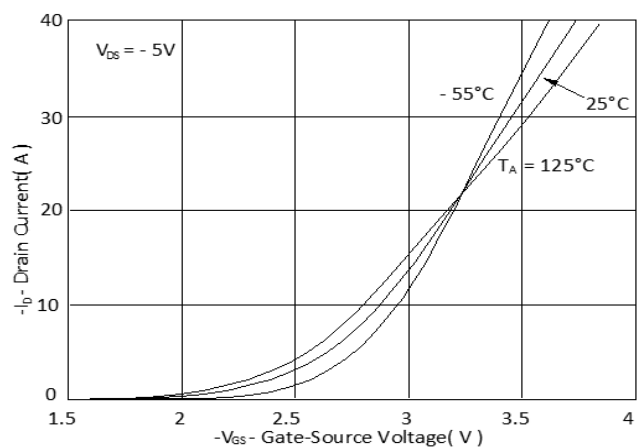


Fig.6 Transfer Characteristics

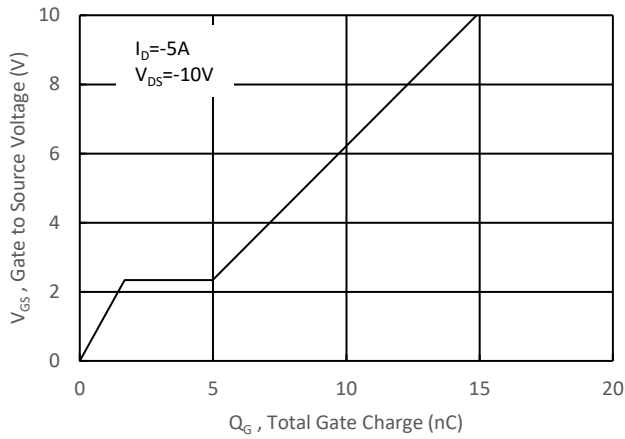


Fig.7 Gate Charge Characteristics

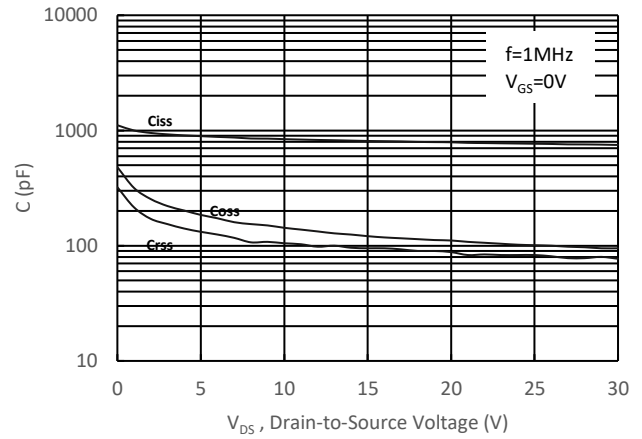


Fig.8 Typical Capacitance Characteristics

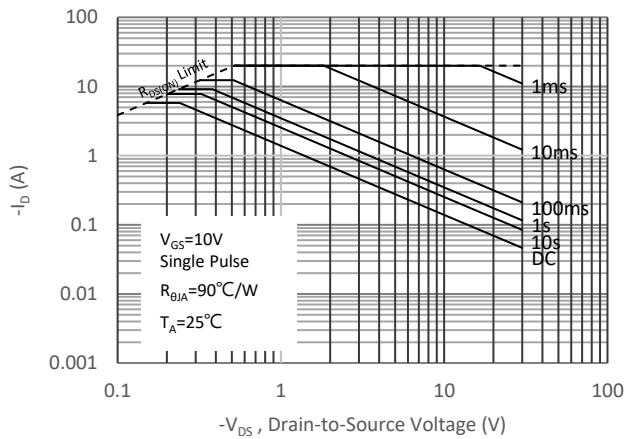


Fig.9. Maximum Safe Operating Area

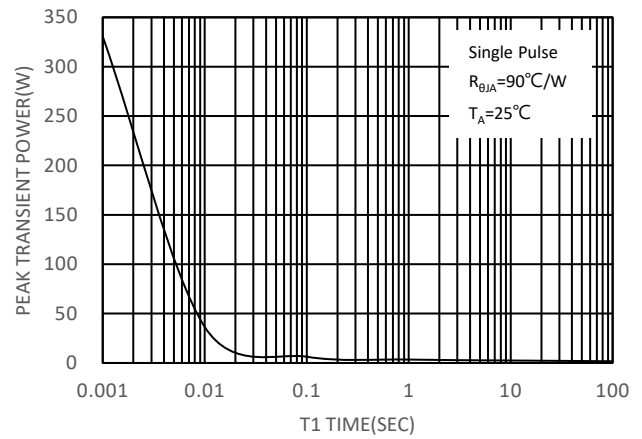


Fig.10. Single Pulse Maximum Power Dissipation

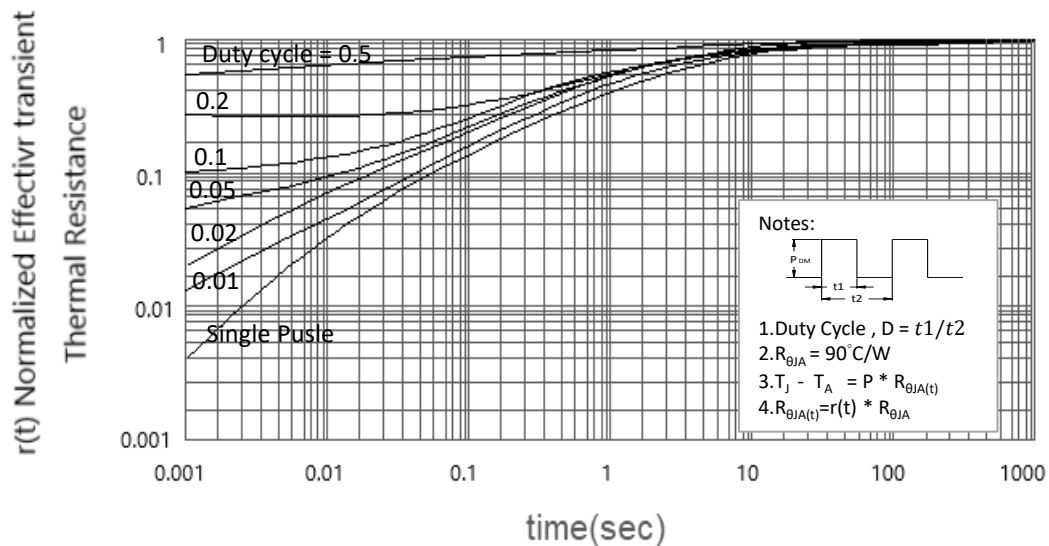
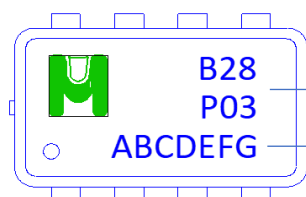


Fig.11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMB28P03L for DFN 3x2



B28P03: Device Name

ABCDEFGH: Date Code

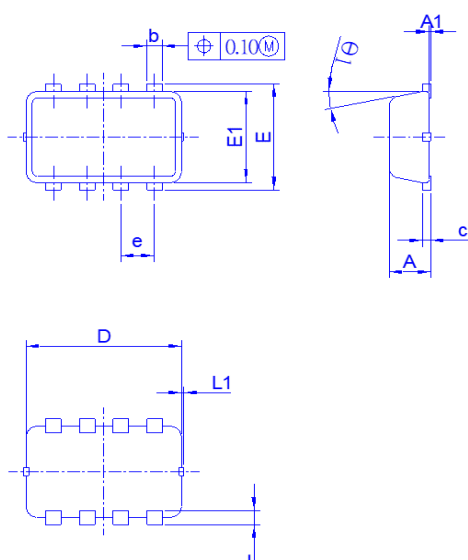
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

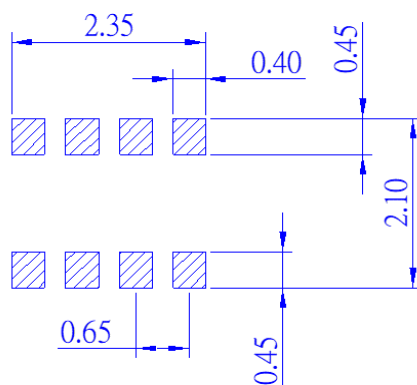
DEFG: Serial No.

Outline Drawing

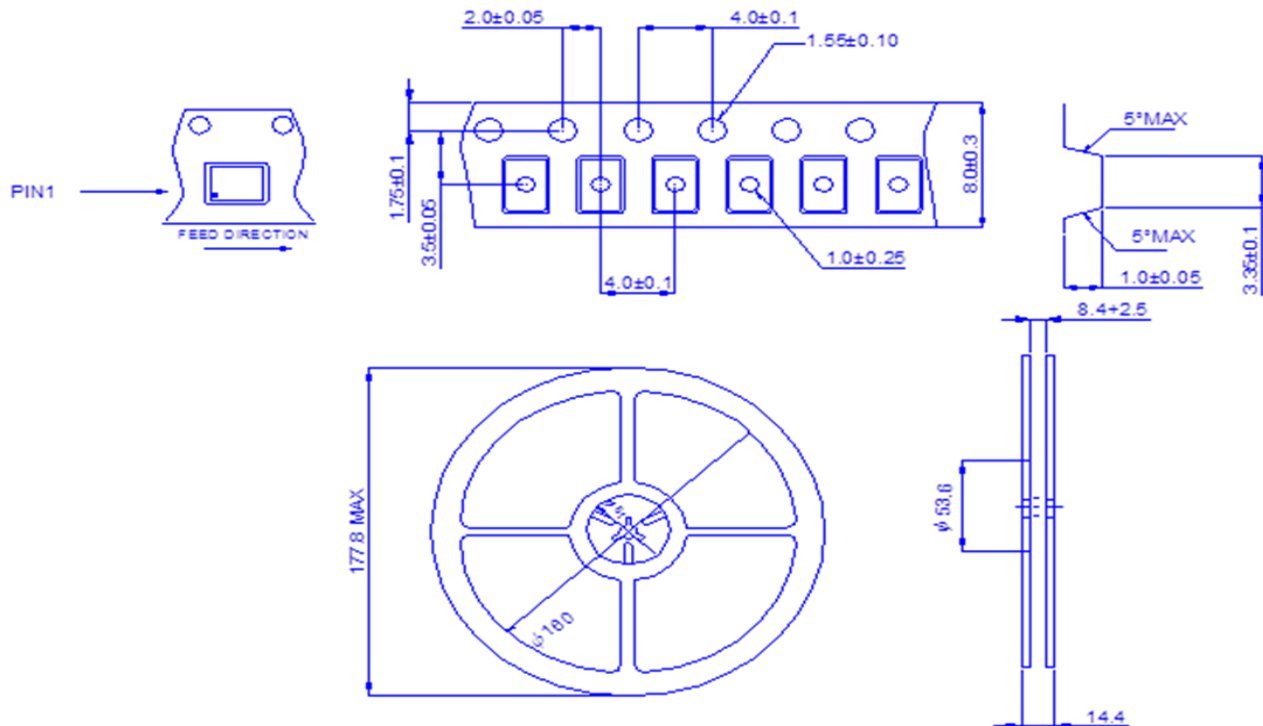


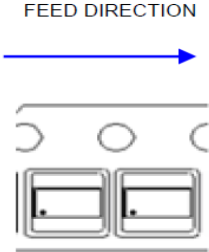
Dimension	A	A1	b	c	D	E	E1	e	L	L1	θ1
Min.	0.7	0	0.24	0.08					0.2	0	0°
Typ.					3	2	1.7	0.65			
Max.	0.9	0.05	0.35	0.25					0.4	0.1	12°

Footprint



◆ Tape&Reel Information:3000pcs/Reel
(Dimension in millimeter)



產品別	DFN3.0X2.0-08
Reel 尺寸	7"
編帶方式	
前空格	50
後空格	50
裝箱數	
滿捲數量	3K
捲/內盒比	5 : 1
內盒滿箱數	15K
內/外箱比	12 : 1
外箱滿箱數	180K



★Datasheet Latest version specification :

	Revision History	Prepared	Approved	Date
A.0	Initial Datasheet	Johnson	Sam	2020/7/8
A.1	Update Tape&Reel information	Johnson	Sam	2020/7/28
A.1	Update electrical characteristics	Johnson	Sam	2020/8/25