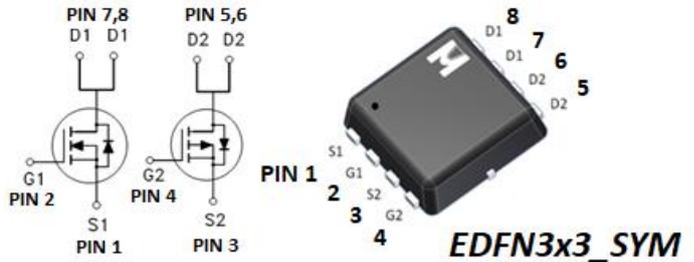


N-Channel + P-Channel Logic Level Enhancement Mode Field Effect Transistor

• Product Summary:

	N-CH	P-CH
BVDSS	30V	-30V
$R_{DS(ON)(MAX.)}@V_{GS}=10V$	20m $\Omega$	20m $\Omega$
$R_{DS(ON)(MAX.)}@V_{GS}=4.5V$	38m $\Omega$	35m $\Omega$
$I_D @T_C=25^\circ C$	22A	-25A
$I_D @T_A=25^\circ C$	10A	-10A

• Pin Description:



N + P Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



• ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$  Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS		UNIT	
		N-CH	P-CH		
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V	
Continuous Drain Current	$I_D$	$T_C = 25^\circ C$	22	-25	A
		$T_C = 100^\circ C$	13	-16	
Continuous Drain Current	$I_D$	$T_A = 25^\circ C$	10	-10	
		$T_A = 70^\circ C$	7	-7	
Pulsed Drain Current <sup>1</sup>	$I_{DM}$	42.5	-51		
Avalanche Current	$I_{AS}$	19	-40		
Avalanche Energy	EAS	L = 0.1mH	18	80	mJ
Repetitive Avalanche Energy <sup>2</sup>			9	40	
Power Dissipation	$P_D$	$T_C = 25^\circ C$	15.6	20.8	W
		$T_C = 100^\circ C$	6.3	8.3	
Power Dissipation	$P_D$	$T_A = 25^\circ C$	3.1	3.1	W
		$T_A = 70^\circ C$	2	2	
Operating Junction & Storage Temperature Range	$T_j, T_{stg}$	-55 to 150		$^\circ C$	

• 100% UIS testing in condition of  $V_D=25V, L=0.1mH, V_G=10V, I_L=12A$ , Rated  $V_{DS}=30V$  N-CH

• 100% UIS testing in condition of  $V_D=25V, L=0.1mH, V_G=10V, I_L=24A$ , Rated  $V_{DS}=30V$  P-CH

• THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM		UNIT
			N-CH	P-CH	
Junction-to-Case	$R_{\theta JC}$		8	6	$^\circ C/W$
Junction-to-Ambient <sup>3</sup>	$R_{\theta JA}$		40	40	

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle < 1%

<sup>3</sup>40 $^\circ C / W$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.

<sup>4</sup>Guarantee by Engineering test

▪ N-CH\_ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage <sup>4</sup>	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250uA	30			V
Gate Threshold Voltage <sup>4</sup>	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250uA	1.2	1.7	2.5	
Gate-Body Leakage <sup>4</sup>	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V			±100	nA
Zero Gate Voltage Drain Current <sup>4</sup>	I <sub>DSS</sub>	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V			1	uA
		V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125 °C			25	
On-State Drain Current <sup>1</sup>	I <sub>D(ON)</sub>	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 10V	22			A
Drain-Source On-State Resistance <sup>1,4</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 8A		17.8	20	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 6A		26.7	38	
Forward Transconductance <sup>1</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 5V, I <sub>D</sub> = 8A		13		S
<b>DYNAMIC</b>						
Input Capacitance <sup>5</sup>	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 15V, f = 1MHz		520		pF
Output Capacitance <sup>5</sup>	C <sub>oss</sub>			96		
Reverse Transfer Capacitance <sup>5</sup>	C <sub>rss</sub>			73		
Gate Resistance <sup>4,5</sup>	R <sub>g</sub>	f = 1MHz		1.4		Ω
Total Gate Charge <sup>1,2,5</sup>	Q <sub>g</sub> (V <sub>GS</sub> =10V)	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A		12		nC
	Q <sub>g</sub> (V <sub>GS</sub> =4.5V)			5		
Gate-Source Charge <sup>1,2,5</sup>	Q <sub>gs</sub>			2.3		
Gate-Drain Charge <sup>1,2,5</sup>	Q <sub>gd</sub>			5.1		
Turn-On Delay Time <sup>1,2,5</sup>	t <sub>d(on)</sub>	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 5A, R <sub>g</sub> = 3Ω		5.3		nS
Rise Time <sup>1,2,5</sup>	t <sub>r</sub>			9.1		
Turn-Off Delay Time <sup>1,2,5</sup>	t <sub>d(off)</sub>			13.2		
Fall Time <sup>1,2,5</sup>	t <sub>f</sub>			1.8		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Continuous Current	I <sub>S</sub>				22	A
Pulsed Current <sup>3</sup>	I <sub>SM</sub>				42.5	
Forward Voltage <sup>1,4</sup>	V <sub>SD</sub>	I <sub>F</sub> = I <sub>S</sub> , V <sub>GS</sub> = 0V			1.3	V
Reverse Recovery Time <sup>5</sup>	t <sub>rr</sub>	I <sub>F</sub> = I <sub>S</sub> , dI <sub>F</sub> /dt = 100A / uS		17.1		nS
Peak Reverse Recovery Current <sup>5</sup>	I <sub>RM(REC)</sub>			0.46		A
Reverse Recovery Charge <sup>5</sup>	Q <sub>rr</sub>			11.9		nC

<sup>1</sup> Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

<sup>2</sup> Independent of operating temperature.

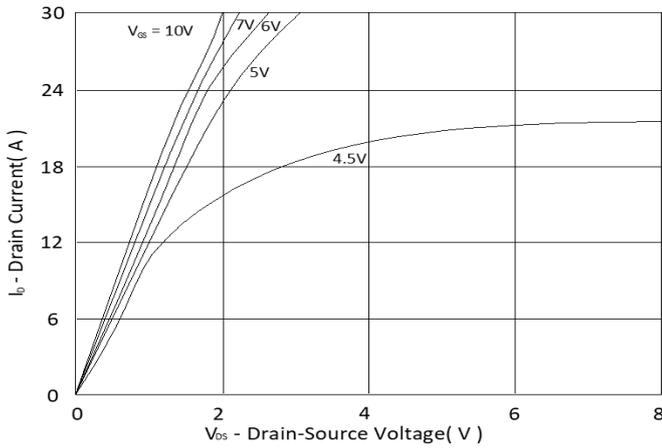
<sup>3</sup> Pulse width limited by maximum junction temperature.

<sup>4</sup> Guarantee by FT test Item

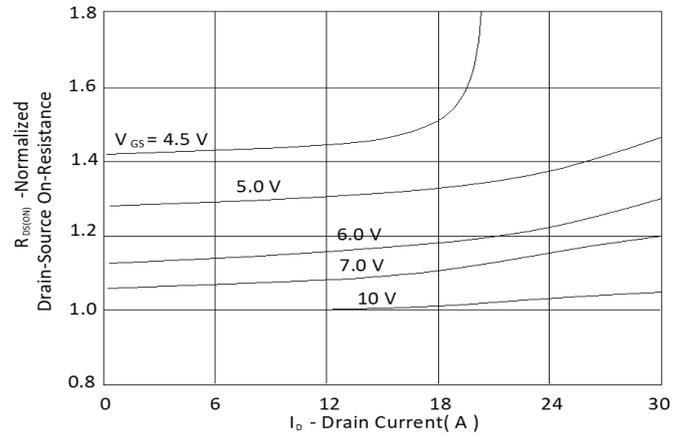
<sup>5</sup> Guarantee by Engineering test

**EMC will review datasheet by quarter, and update new version.**

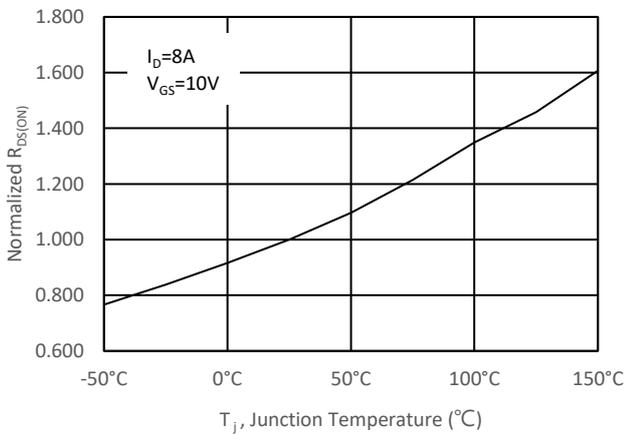
▪ N-CH\_TYPICAL CHARACTERISTICS



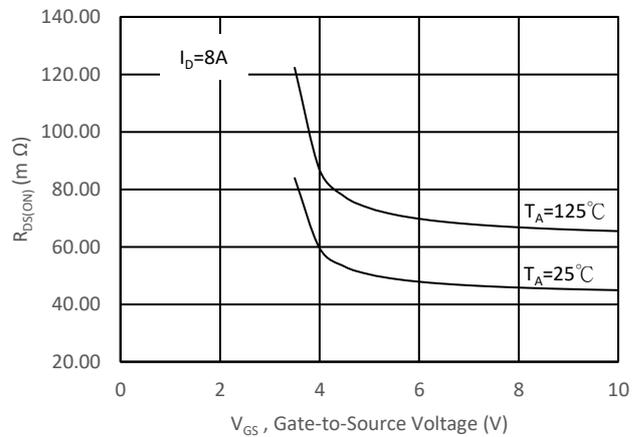
**Fig.1 Typical Output Characteristics**



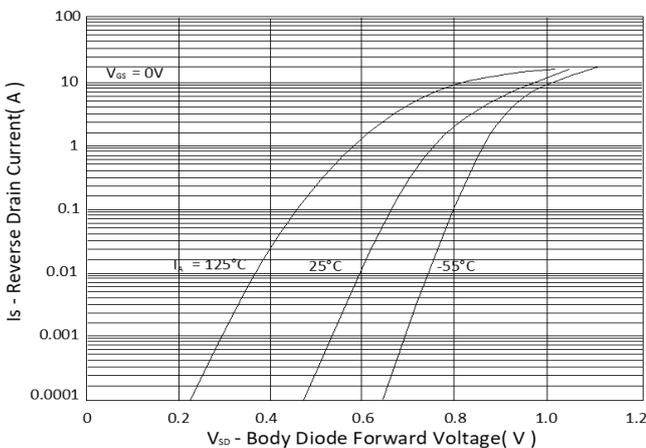
**Fig.2 On-Resistance Variation with Drain Current and Gate Voltage**



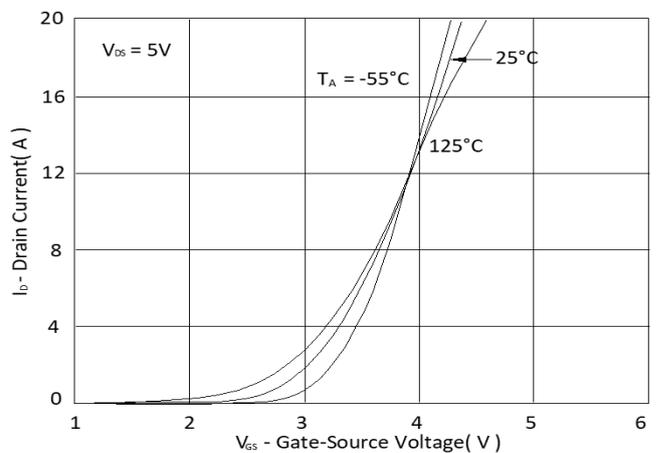
**Fig.3 Normalized On-Resistance v.s. Junction Temperature**



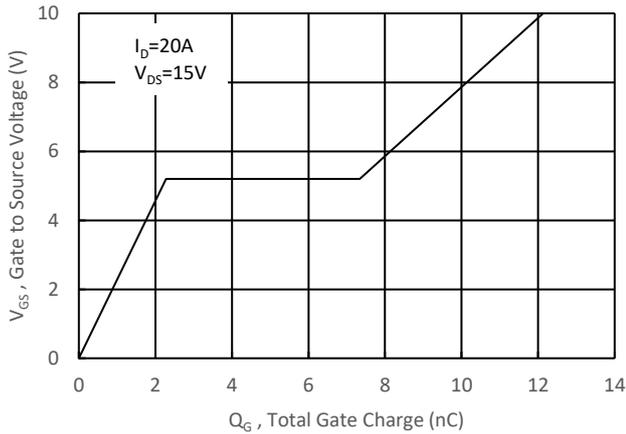
**Fig.4 On-Resistance v.s. Gate Voltage**



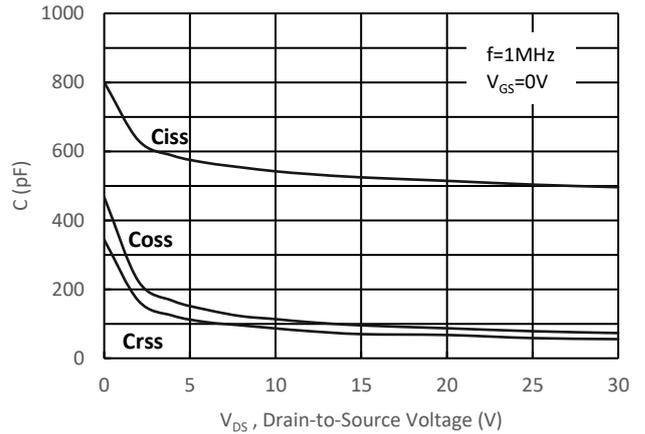
**Fig.5 Forward Characteristic of Reverse Diode**



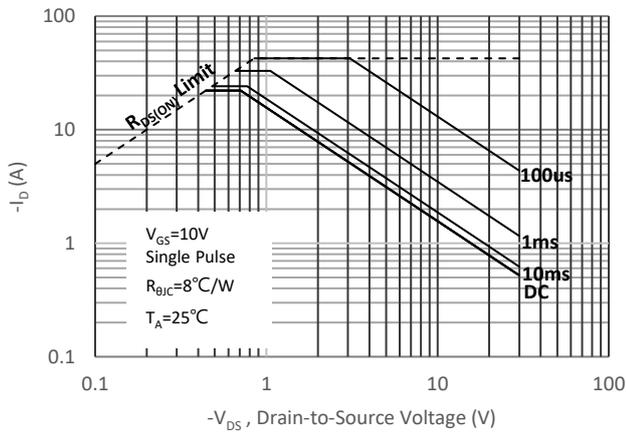
**Fig.6 Transfer Characteristics**



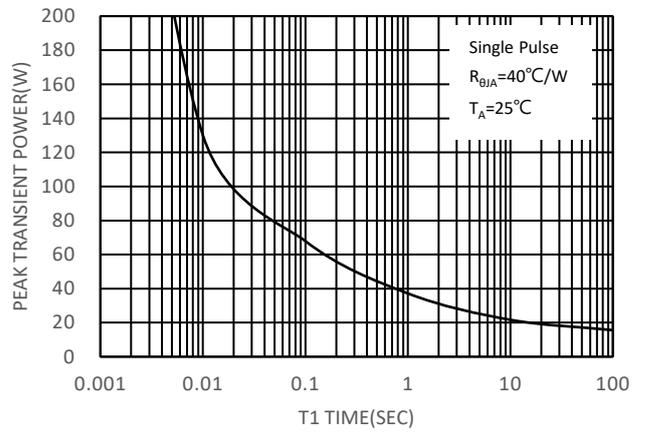
**Fig.7 Gate Charge Characteristics**



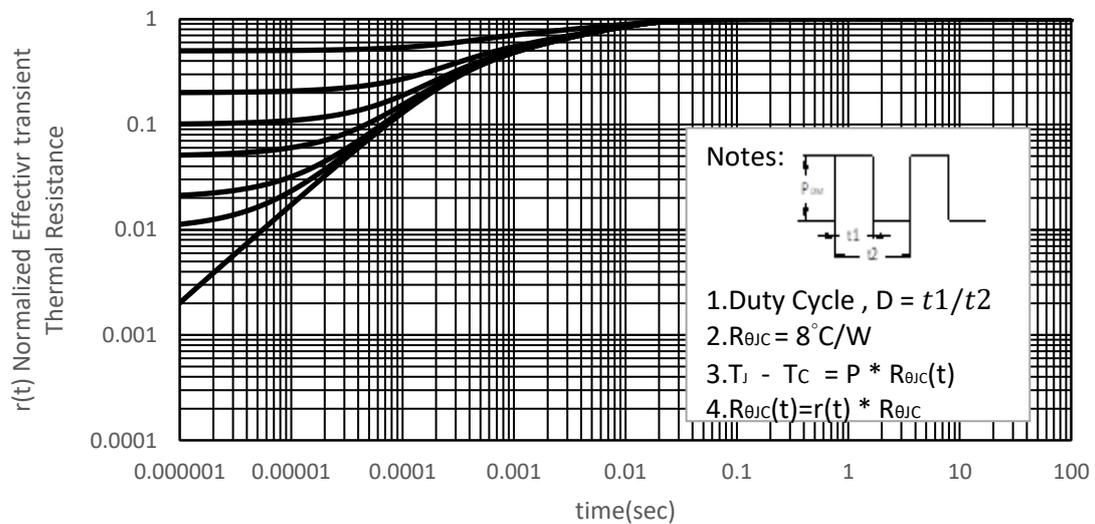
**Fig.8 Typical Capacitance Characteristics**



**Fig 9. Maximum Safe Operating Area**



**Fig 10. Single Pulse Maximum Power Dissipation**



**Fig 11. Effective Transient Thermal Impedance**



▪ P-CH\_ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage <sup>4</sup>	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250uA	-30			V
Gate Threshold Voltage <sup>4</sup>	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250uA	-1	-1.7	-3	
Gate-Body Leakage <sup>4</sup>	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V			±100	nA
Zero Gate Voltage Drain Current <sup>4</sup>	I <sub>DSS</sub>	V <sub>DS</sub> = -24V, V <sub>GS</sub> = 0V			-1	uA
		V <sub>DS</sub> = -20V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125 °C			-25	
On-State Drain Current <sup>1</sup>	I <sub>D(ON)</sub>	V <sub>DS</sub> = -10V, V <sub>GS</sub> = -10V	-25			A
Drain-Source On-State Resistance <sup>1,4</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> = -10V, I <sub>D</sub> = -10A		14.7	20	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -7A		20.6	35	
Forward Transconductance <sup>1</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -5V, I <sub>D</sub> = -8A		9		S
<b>DYNAMIC</b>						
Input Capacitance <sup>5</sup>	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = -15V, f = 1MHz		1280		pF
Output Capacitance <sup>5</sup>	C <sub>oss</sub>			211		
Reverse Transfer Capacitance <sup>5</sup>	C <sub>rss</sub>			164		
Gate Resistance <sup>4,5</sup>	R <sub>g</sub>	f = 1MHz	6.15			Ω
Total Gate Charge <sup>1,2,5</sup>	Q <sub>g</sub> (V <sub>GS</sub> =10V)	V <sub>DS</sub> = -15V, V <sub>GS</sub> = -10V, I <sub>D</sub> = -20A		25		nC
	Q <sub>g</sub> (V <sub>GS</sub> =4.5V)			12		
Gate-Source Charge <sup>1,2,5</sup>	Q <sub>gs</sub>			5.2		
Gate-Drain Charge <sup>1,2,5</sup>	Q <sub>gd</sub>			5.3		
Turn-On Delay Time <sup>1,2,5</sup>	t <sub>d(on)</sub>			6		
Rise Time <sup>1,2,5</sup>	t <sub>r</sub>	V <sub>DS</sub> = -15V, V <sub>GS</sub> = -10V, I <sub>D</sub> = -5A, R <sub>g</sub> = 3Ω		11.4		
Turn-Off Delay Time <sup>1,2,5</sup>	t <sub>d(off)</sub>			41.7		
Fall Time <sup>1,2,5</sup>	t <sub>f</sub>			35		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Continuous Current	I <sub>S</sub>				-25	A
Pulsed Current <sup>3</sup>	I <sub>SM</sub>				-51	
Forward Voltage <sup>1,4</sup>	V <sub>SD</sub>	I <sub>F</sub> = I <sub>S</sub> , V <sub>GS</sub> = 0V			-1.3	V
Reverse Recovery Time <sup>5</sup>	t <sub>rr</sub>	I <sub>F</sub> = I <sub>S</sub> , dI <sub>F</sub> /dt = 100A / uS		18.8		nS
Peak Reverse Recovery Current <sup>5</sup>	I <sub>RM(REC)</sub>			0.49		A
Reverse Recovery Charge <sup>5</sup>	Q <sub>rr</sub>			12.4		nC

<sup>1</sup>Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

<sup>2</sup>Independent of operating temperature.

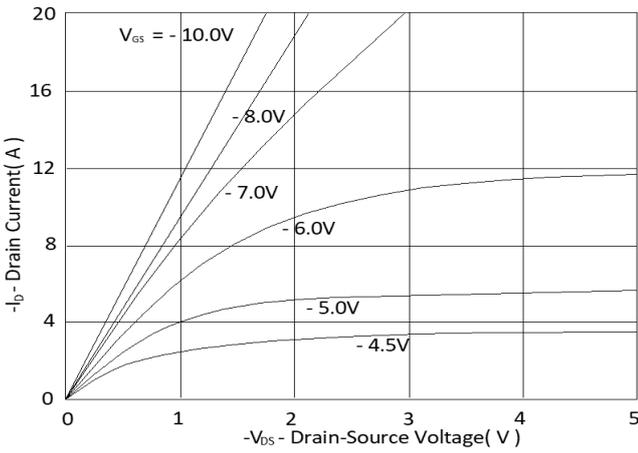
<sup>3</sup>Pulse width limited by maximum junction temperature.

<sup>4</sup>Guarantee by FT test Item

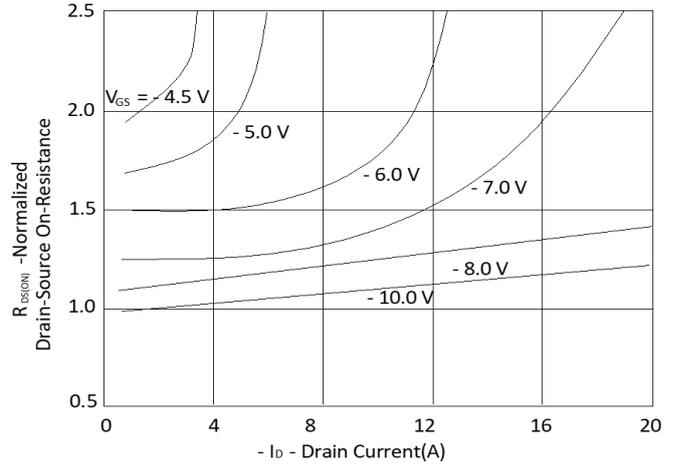
<sup>5</sup>Guarantee by Engineering test

**EMC will review datasheet by quarter, and update new version.**

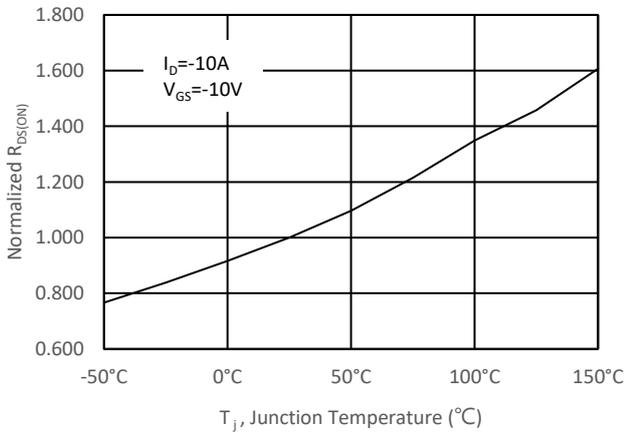
▪ P-CH\_TYPICAL CHARACTERISTICS



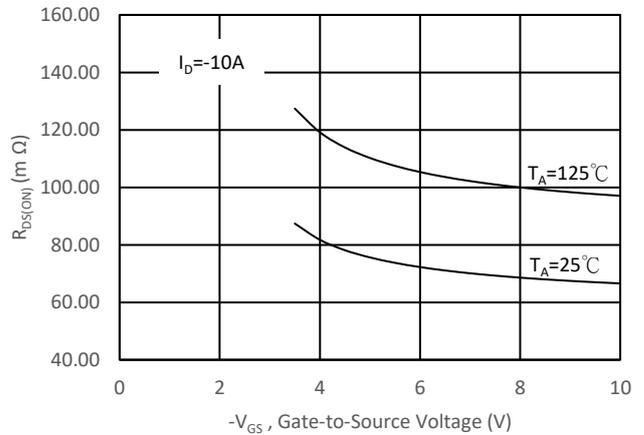
**Fig.1 Typical Output Characteristics**



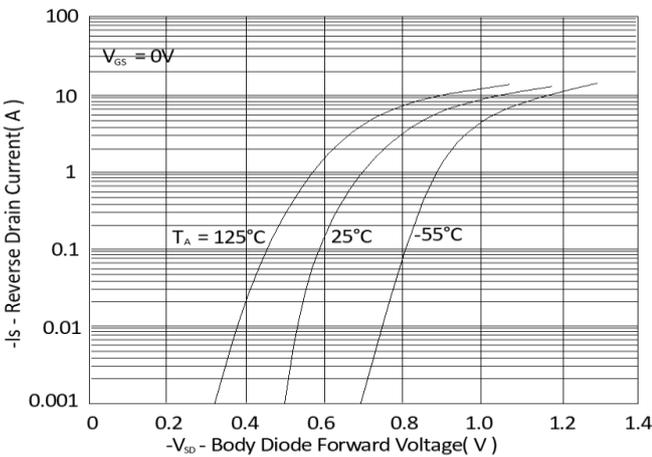
**Fig.2 On-Resistance Variation with Drain Current and Gate Voltage**



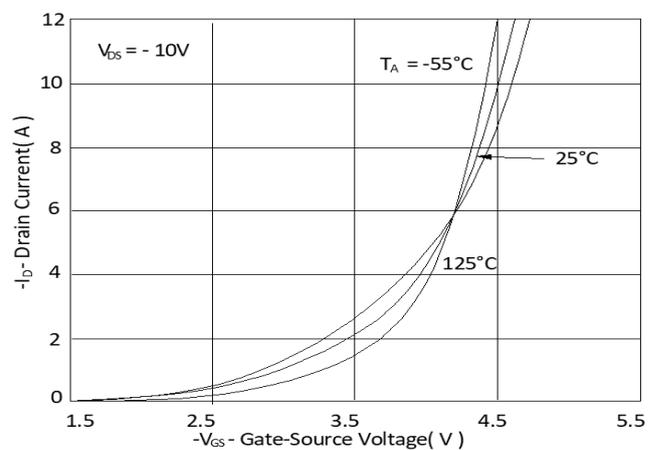
**Fig.3 Normalized On-Resistance v.s. Junction Temperature**



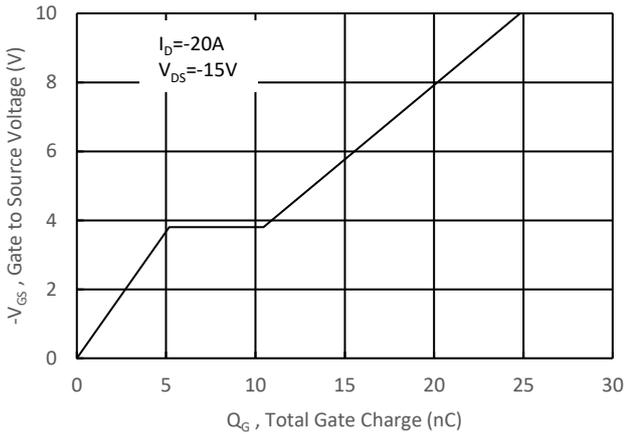
**Fig.4 On-Resistance v.s. Gate Voltage**



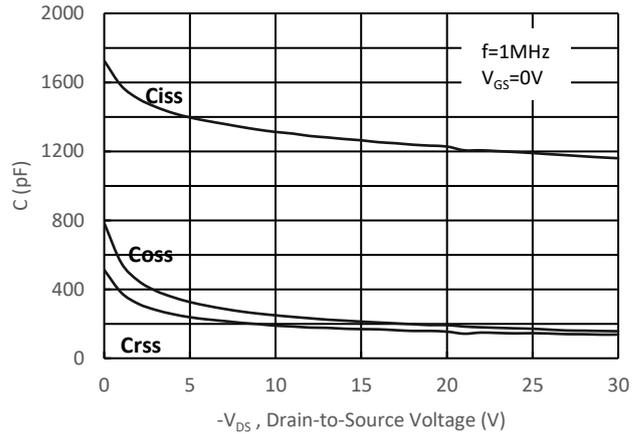
**Fig.5 Forward Characteristic of Reverse Diode**



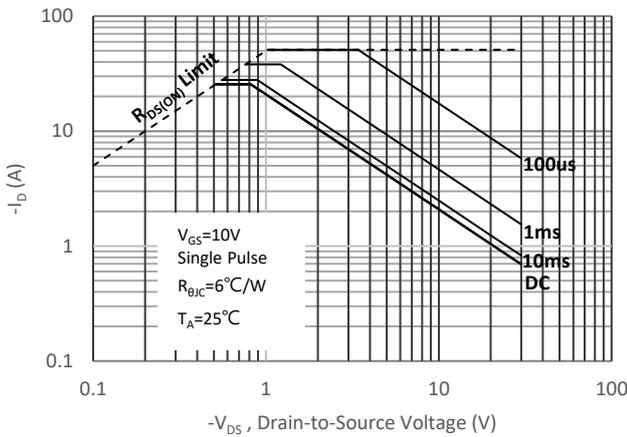
**Fig.6 Transfer Characteristics**



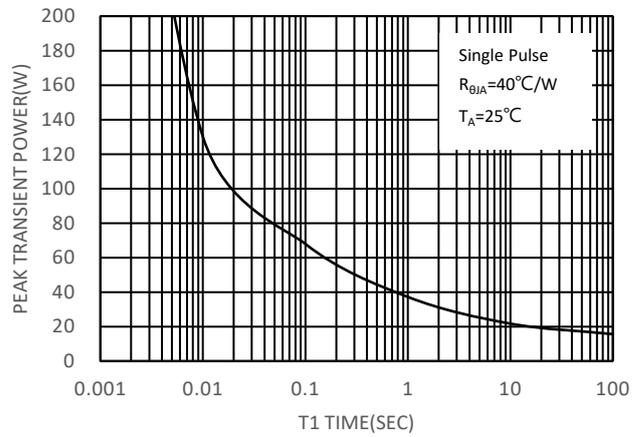
**Fig.7 Gate Charge Characteristics**



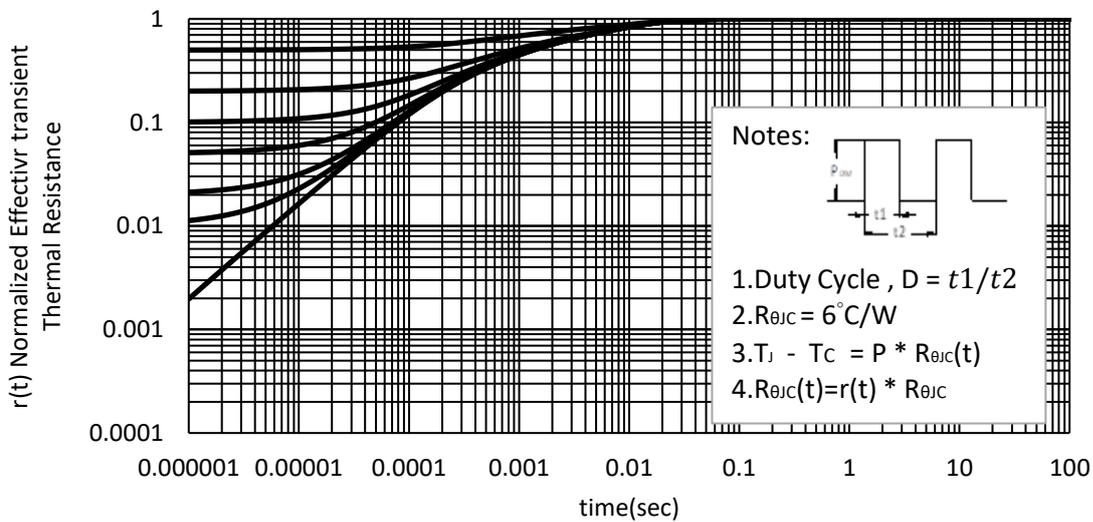
**Fig.8 Typical Capacitance Characteristics**



**Fig 9. Maximum Safe Operating Area**



**Fig 10. Single Pulse Maximum Power Dissipation**



**Fig 11. Effective Transient Thermal Impedance**

**Ordering & Marking Information:**

Device Name: EMB20C03V for EDFN 3x3



→ B20C03: Device Name

→ ABCDEFG: Date Code

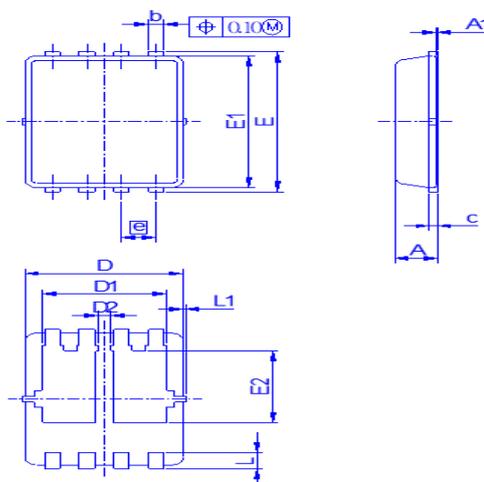
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

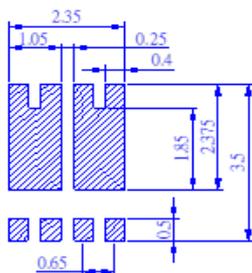
**Outline Drawing**



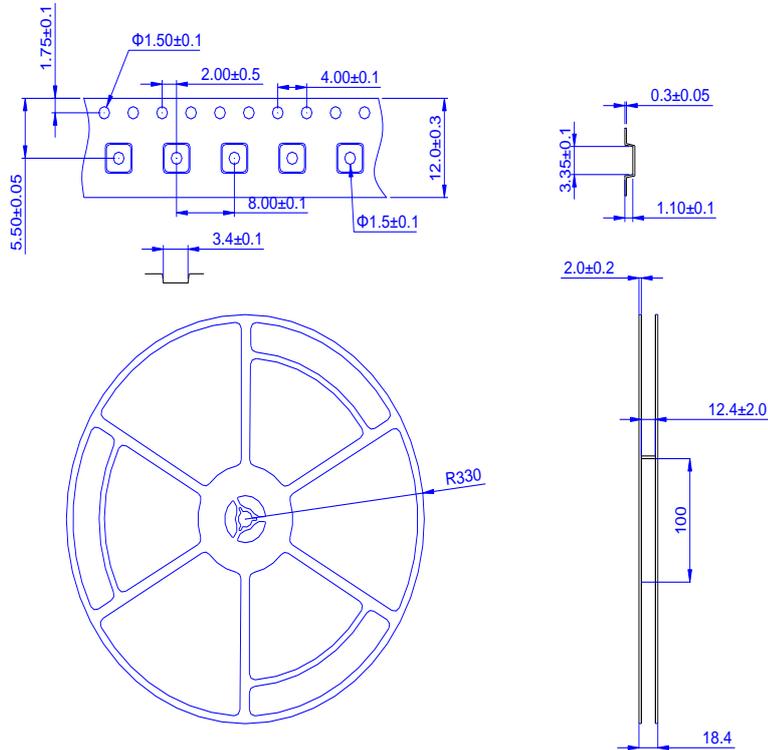
Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	e	L
Min.	0.65	0	0.2	0.1	2.9	2.15	0.28	3.1	2.9	1.53	0.55	0.3
Typ.	0.75	-	0.3	0.15	3	2.47	0.38	3.2	3	1.81	0.65	0.4
Max.	0.9	0.05	0.4	0.25	3.3	2.75	-	3.5	3.3	1.98	0.75	0.5

Dimension	L1	θ1
Min.	-	0°
Typ.	0.075	10°
Max.	0.15	14°

**Footprint**



◆ Tape&Reel Information:5000pcs/Reel(Dimension in millimeter)



產品別	EDFN 3x3
Reel尺寸	13"
編帶方式	<p>FEED DIRECTION</p>
前空格	50
後空格	50
裝箱數	
滿捲數量	5K
捲/內盒比	1:1
內盒滿箱數	5K
內/外箱比	10:1
外箱滿箱數	50K