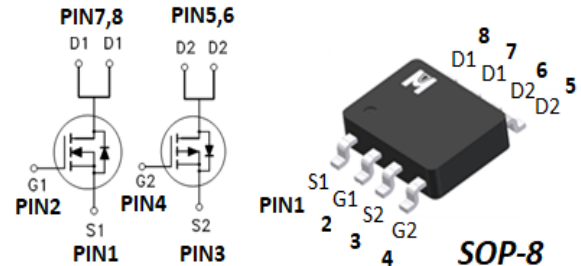


N-Channel + P Channel Logic Level Enhancement Mode Field Effect Transistor

▪ **Product Summary:**

	N-CH	P-CH
BVDSS	30 V	-30 V
$R_{DS(on)} (MAX.) @ V_{GS}=10V$	18 mΩ	22 mΩ
$R_{DS(on)} (MAX.) @ V_{GS}=4.5V$	26 mΩ	37 mΩ
$I_D @ T_C=25^{\circ}C$	12 A	-12 A
$I_D @ T_A=25^{\circ}C$	8 A	-7 A

▪ **Pin Description:**



N Channel + P Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



▪ **ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}C$ Unless Otherwise Noted)**

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
			N-CH	P-CH	
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	$T_C = 25^{\circ}C$	I_D	12	-12	A
	$T_C = 100^{\circ}C$		8	-7	
Continuous Drain Current	$T_A = 25^{\circ}C$	I_D	8	-7	
	$T_A = 70^{\circ}C$		6	-6	
Pulsed Drain Current ¹		I_{DM}	32	-28	A
Avalanche Current		I_{AS}	22	-30	
Avalanche Energy	$L = 0.1mH$	EAS	24.2	45	mJ
Repetitive Avalanche Energy ²	$L = 0.05mH$	EAR	12.1	22.50	
Power Dissipation	$T_C = 25^{\circ}C$	P_D	5	5	W
	$T_C = 100^{\circ}C$		2	2	
Power Dissipation	$T_A = 25^{\circ}C$	P_D	2	2	W
	$T_A = 70^{\circ}C$		1.3	1.3	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		$^{\circ}C$

▪ **THERMAL RESISTANCE RATINGS**

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM		UNIT
			N-CH	P-CH	
Junction-to-Case	$R_{\theta JC}$		25	25	$^{\circ}C/W$
Junction-to-Ambient ³	$R_{\theta JA}$		62.5	62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle < 1%

³62.5 $^{\circ}C/W$ when mounted on a 1 in² pad of 2 oz copper.

⁴Guarantee by Engineering test

▪ N-CH_ELECTRICAL CHARACTERISTICS (T_j = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250uA	30			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	1.5	1.8	3	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 24V, V _{GS} = 0V			1	uA
		V _{DS} =20V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	12			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 10A		15	18	mΩ
		V _{GS} = 4.5V, I _D = 6A		21	26	
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		727		pF
Output Capacitance ⁵	C _{OSS}			123		
Reverse Transfer Capacitance ⁵	C _{rss}			107		
Gate Resistance ^{4,5}	R _g	f = 1MHz		1.4		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 15V, V _{GS} = 10V, I _D = 10A		16.0		nC
	Q _g (V _{GS} =4.5V)			8.8		
Gate-Source Charge ^{1,2,5}	Q _{gs}			2.0		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			4.8		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 15V, V _{GS} = 10V, I _D = 5A , R _g = 6Ω		6.7		nS
Rise Time ^{1,2,5}	t _r			12.2		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			21.4		
Fall Time ^{1,2,5}	t _f			16.2		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				12	A
Pulsed Current ³	I _{SM}				32	
Forward Voltage ^{1,4}	V _{SD}	I _F = 15A, V _{GS} = 0V			1.2	V
Reverse Recovery Time ⁵	t _{rr}	I _F = 15A, dI _F /dt = 100A / uS		10.3		nS
Reverse Recovery Charge ⁵	Q _{rr}			4.3		nC

¹ Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

² Independent of operating temperature.

³ Pulse width limited by maximum junction temperature.

⁴ Guarantee by FT test Item

⁵ Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪ TYPICAL CHARACTERISTICS

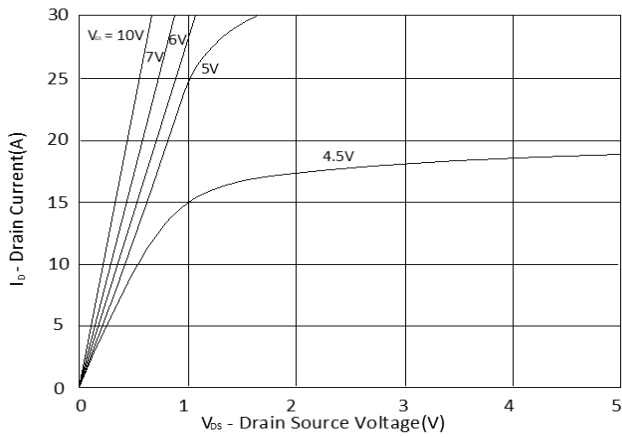


Fig.1 Typical Output Characteristics

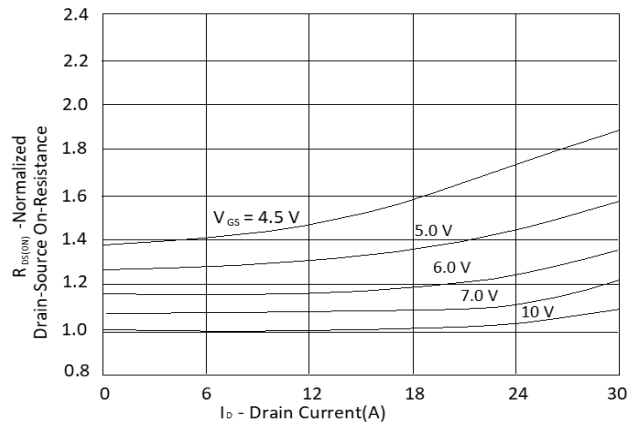


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

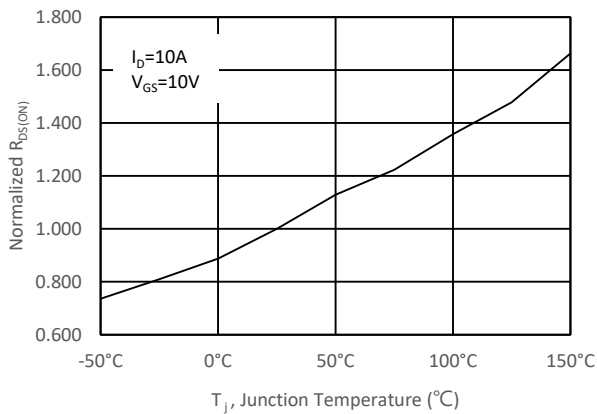


Fig.3 Normalized On-Resistance v.s. Junction Temperature

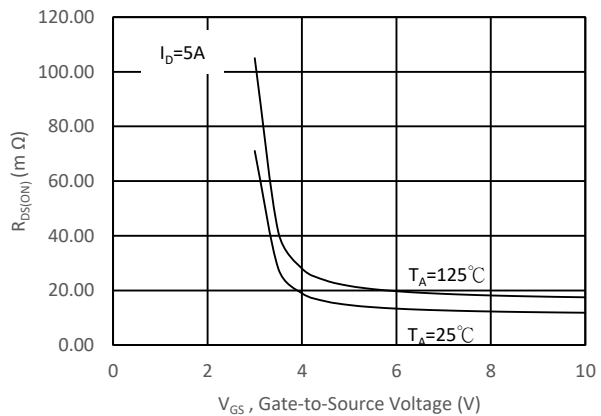


Fig.4 On-Resistance v.s. Gate Voltage

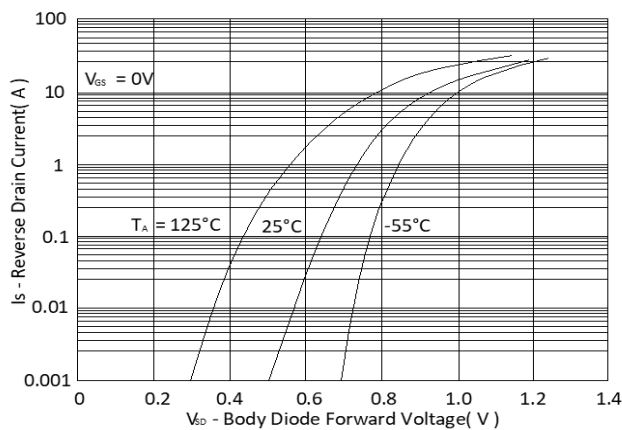


Fig.5 Forward Characteristic of Reverse Diode

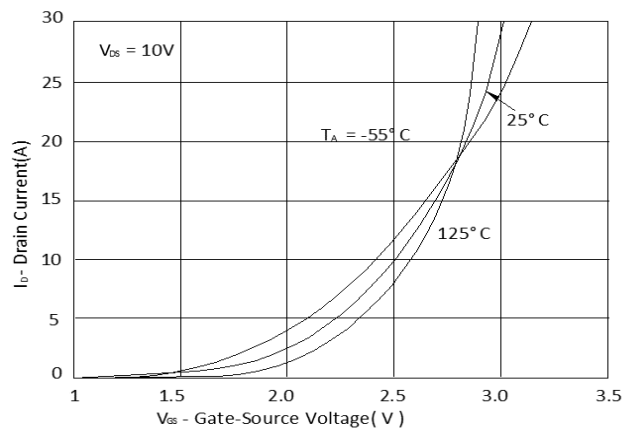


Fig.6 Transfer Characteristics

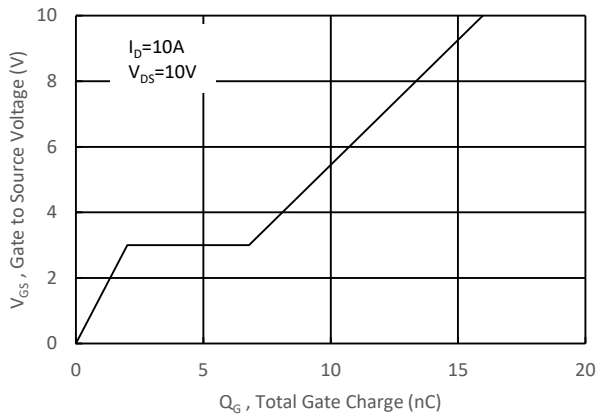


Fig.7 Gate Charge Characteristics

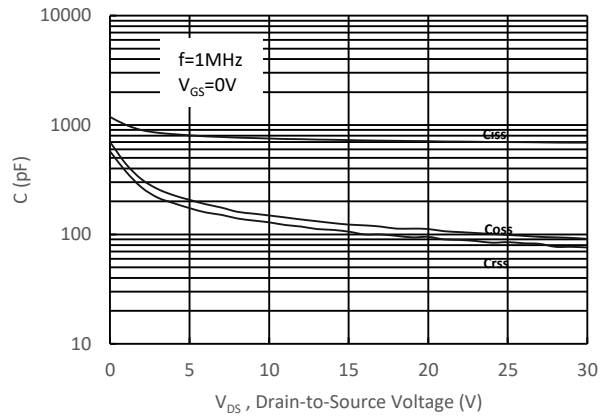


Fig.8 Typical Capacitance Characteristics

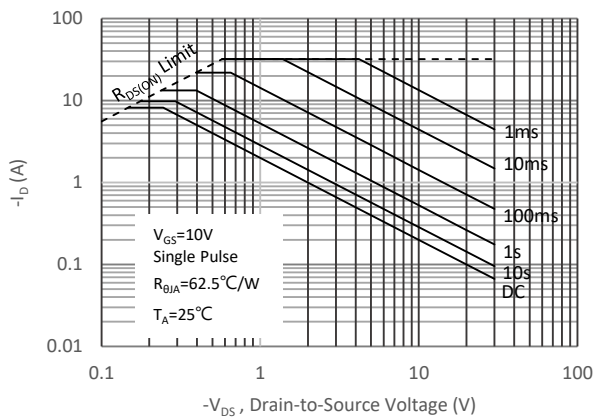


Fig 9. Maximum Safe Operating Area

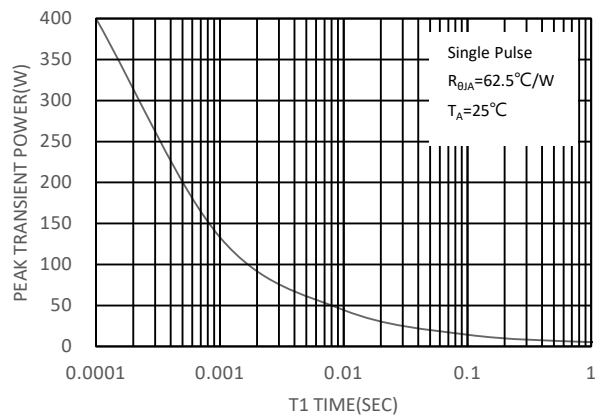


Fig 10. Single Pulse Maximum Power Dissipation

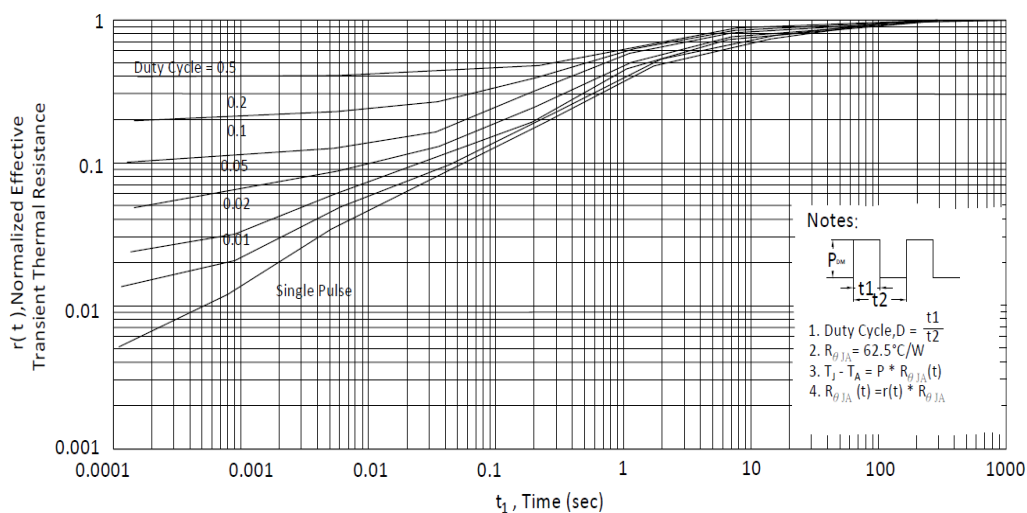


Fig 11. Effective Transient Thermal Impedance

▪ P-CH_ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250uA	-30			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250uA	-1.5	-2.0	-3.0	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = -24V, V _{GS} = 0V			-1	uA
		V _{DS} = -20V, V _{GS} = 0V, T _J = 125 °C			-25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = -5V, V _{GS} = -10V	-12			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = -10V, I _D = -8A		18	22	mΩ
		V _{GS} = -4.5V, I _D = -6A		28	37	
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = -15V, f = 1MHz		775		pF
Output Capacitance ⁵	C _{oss}			126		
Reverse Transfer Capacitance ⁵	C _{rss}			100		
Gate Resistance ^{4,5}	R _g	f = 1MHz		5.2		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = -15V, V _{GS} = -10V, I _D = -8A		14.6		nC
	Q _g (V _{GS} =4.5V)			7.8		
Gate-Source Charge ^{1,2,5}	Q _{gs}			2.3		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			3.8		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = -15V, V _{GS} = -10V, I _D = -5A , R _g = 6Ω		6.5		nS
Rise Time ^{1,2,5}	t _r			14.0		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			27.9		
Fall Time ^{1,2,5}	t _f			24.5		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				-12	A
Pulsed Current ³	I _{SM}				-28	
Forward Voltage ^{1,4}	V _{SD}	I _F = -15A, V _{GS} = 0V			-1.2	V
Reverse Recovery Time ⁵	t _{rr}	I _F = -15A, dI _F /dt = 100A / uS		6.7		nS
Reverse Recovery Charge ⁵	Q _{rr}			2.4		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪ TYPICAL CHARACTERISTICS

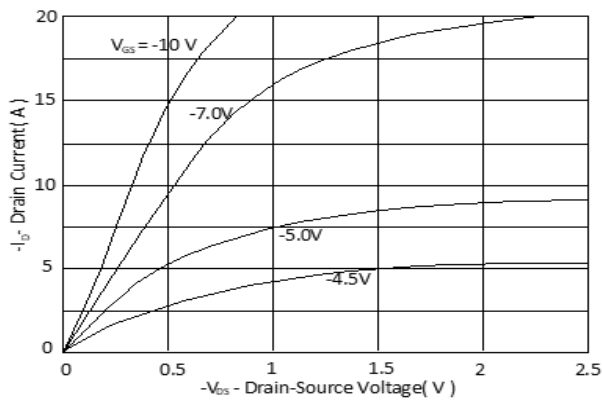


Fig.1 Typical Output Characteristics

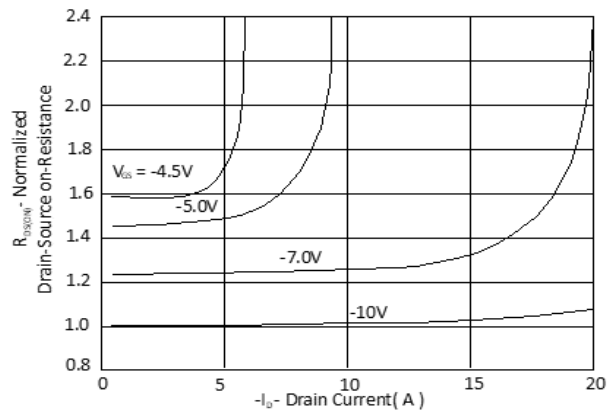


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

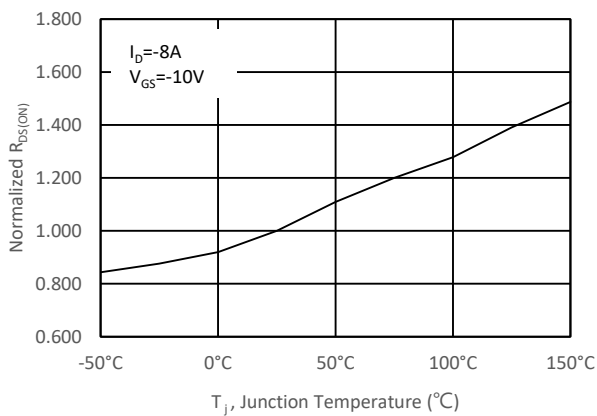


Fig.3 Normalized On-Resistance v.s. Junction Temperature

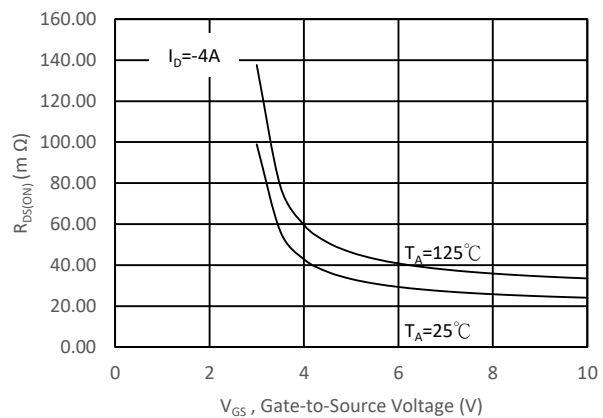


Fig.4 On-Resistance v.s. Gate Voltage

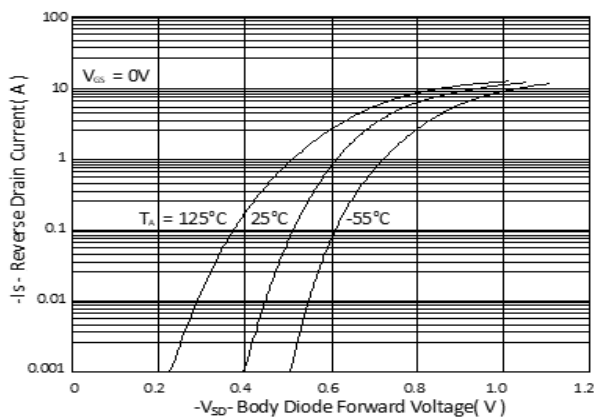


Fig.5 Forward Characteristic of Reverse Diode

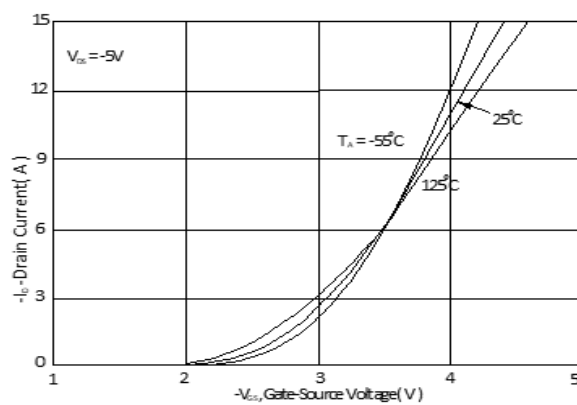


Fig.6 Transfer Characteristics

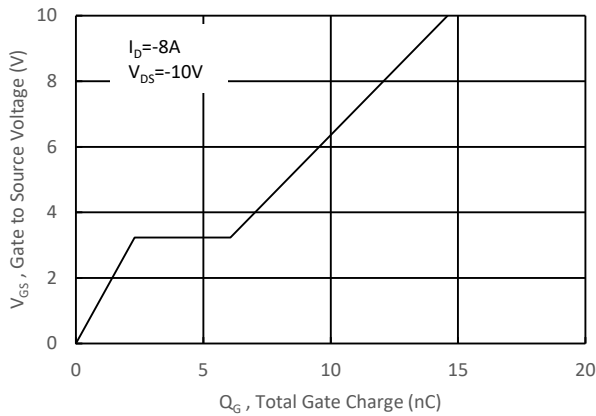


Fig.7 Gate Charge Characteristics

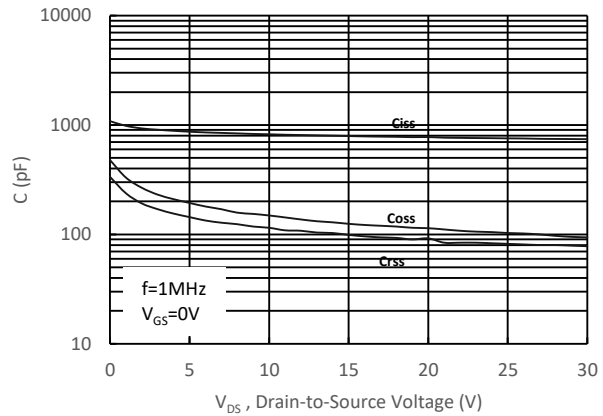


Fig.8 Typical Capacitance Characteristics

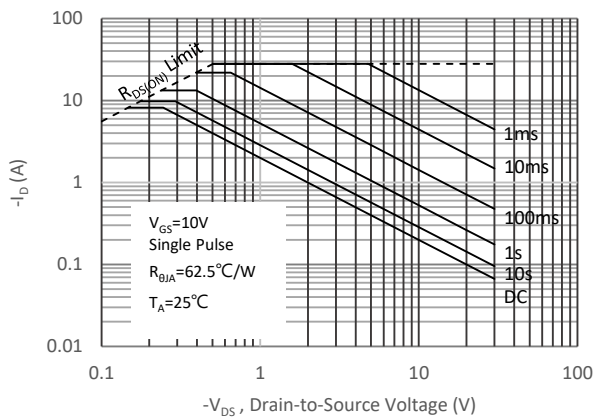


Fig 9. Maximum Safe Operating Area

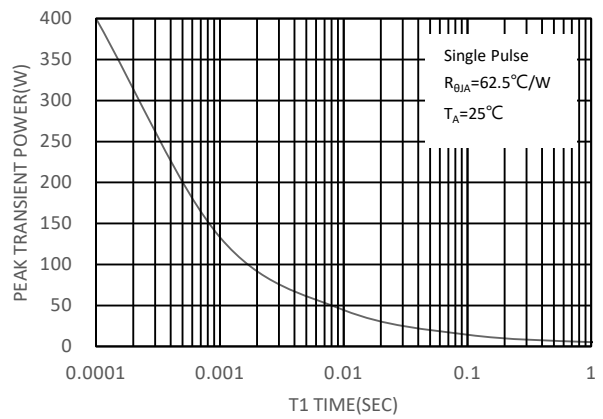


Fig 10. Single Pulse Maximum Power Dissipation

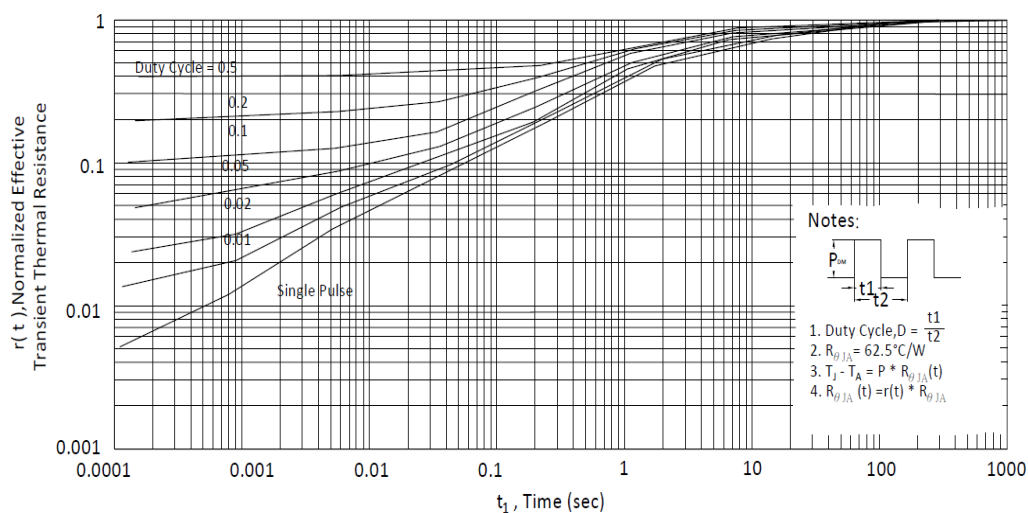
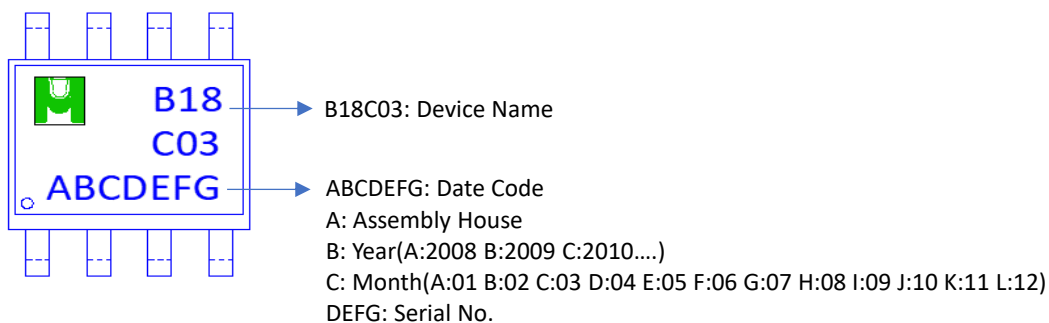


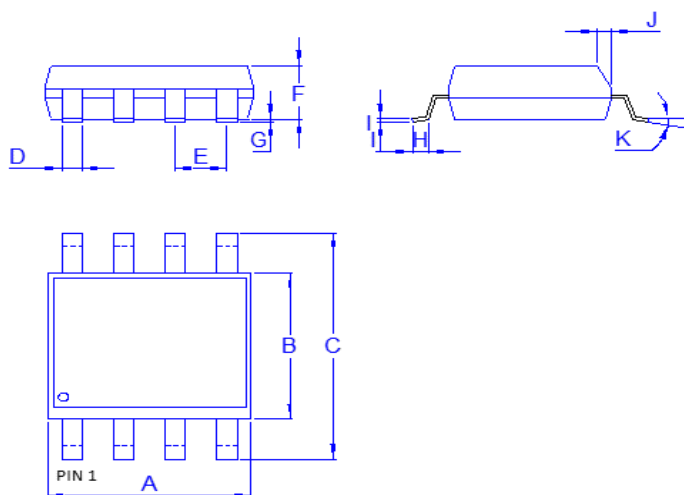
Fig 11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMB18C03G for SOP-8

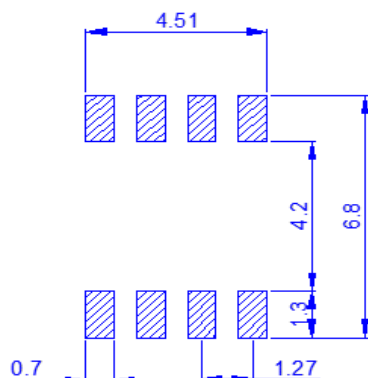


Outline Drawing

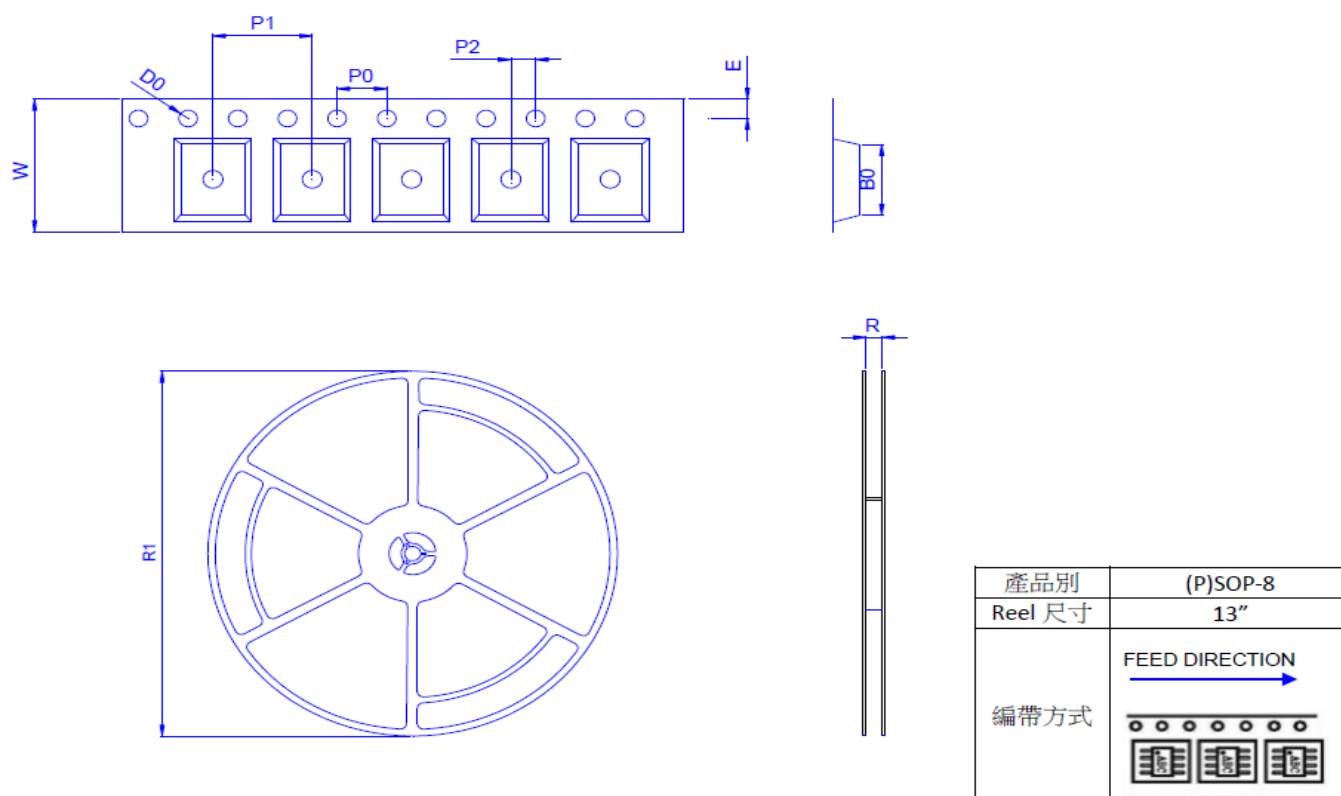


Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.7	3.8	5.8	0.31		1.35	0.01	0.4	0.1	0.25	0°
Typ.	4.9	3.9	6	0.41	1.27	1.55	0.18	0.6	0.2	0.3	
Max.	5.1	4	6.2	0.51		1.75	0.25	1.27	0.25	0.5	8°

Footprint



◆ Tape&Reel Information:2500pcs/Reel



Dimension in mm

Dimension	Carrier tape							Reel	
	B0	D0	E	P0	P1	P2	W	R	R1
Typ.	6.50	1.50	1.75	4.00	8.00	2.00	12.00	12.40	330.00
±	0.40	0.20	0.20	0.20	0.20	0.20	0.50	REF	REF