杰力科技股份有限公司
Excelliance MOS Corporation

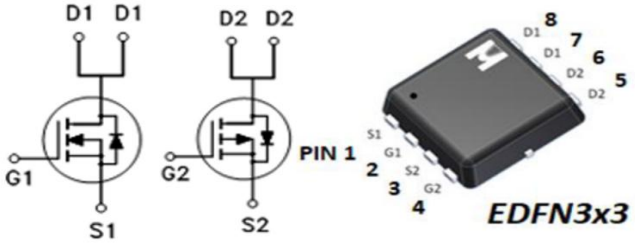
EMB18A04V

Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

▪Product Summary:

	Q1	Q2
BV_{DSS}	40V	40V
$R_{DSON(MAX)}V_{GS}$=10V	23mΩ	23mΩ
$R_{DSON(MAX)}V_{GS}$=4.5V	27mΩ	27mΩ
I_D @T_C=25°C	26A	26A

▪ Pin Description:



Dual N Channel MOSFET
UIS, Rg 100% Tested
RoHS & Halogen Free & TSCA Compliant

▪ ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS Q1	LIMITS Q2	UNIT
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	26	26	A
	T_C = 100 °C		16	16	
Continuous Drain Current	T_A = 25 °C	I_D	8	8	
	T_A = 70 °C		6	6	
Pulsed Drain Current[1]		I_{DM}	104	104	
Avalanche Current		I_{AS}	22	22	
Avalanche Energy	L = 0.1mH	EAS	24	24	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	EAR	12	12	
Power Dissipation	T_C = 25 °C	P_D	25	25	W
	T_C = 100 °C		10	10	
Power Dissipation	T_A = 25 °C	P_D	2.4	2.4	W
	T_A = 70 °C		1.5	1.5	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

▪ 100% UIS testing in condition of VD=35V, L=0.1mH, VG=10V, IL=14A,RG=25Ω,Rated VDS=40V N-CH_Q1

▪ 100% UIS testing in condition of VD=35V, L=0.1mH, VG=10V, IL=14A,RG=25Ω,Rated VDS=40V N-CH_Q2

▪THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM Q1	MAXIMUM Q2	UNIT
Junction-to-Case		$R_{\theta JC}$		5	5	°C/W
Junction-to-Ambient[3,4]	t≦10s	$R_{\theta JA}$		52	52	
	Steady-State	$R_{\theta JA}$		100	100	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle < 1%

[3]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C.

[4]Guarantee by Engineering test

▪ Q1_ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage[4]	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	40			V
Gate Threshold Voltage[4]	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.2	1.8	2.5	
Gate-Body Leakage[4]	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current[4]	I_{DSS}	V_{DS} = 40V, V_{GS} = 0V			1	μA
		V_{DS} =40V, V_{GS} =0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	26			A
Drain-Source On-State Resistance[1,4]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 20A		19	23	mΩ
		V_{GS} = 4.5V, I_D = 20A		22	27	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 20A		48		S
DYNAMIC						
Input Capacitance[5]	C_{iss}	V_{GS} = 0V, V_{DS} = 20V, f = 1MHz		621		pF
Output Capacitance[5]	C_{oss}			73		
Reverse Transfer Capacitance[5]	C_{rss}			44		
Gate Resistance[4,5]	R_g	f = 1MHz		1.5		Ω
Total Gate Charge[1,2,5]	Q_g(V_{GS}=10V)	V_{DS} = 20V, V_{GS} = 10V, I_D = 20A		12		nC
Total Gate Charge[1,2,5]	Q_g(V_{GS}=4.5V)			5		
Gate-Source Charge[1,2,5]	Q_{gs}			3		
Gate-Drain Charge[1,2,5]	Q_{gd}			1.4		
Turn-On Delay Time[1,2,5]	$t_{d(on)}$	V_{DS} = 20V, V_{GS} = 10V, I_D = 5A , Rg = 3Ω		6		nS
Rise Time[1,2,5]	t_r			7		
Turn-Off Delay Time[1,2,5]	$t_{d(off)}$			13		
Fall Time[1,2,5]	t_f			2.3		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				21	A
Pulsed Current[3]	I_{SM}				120	
Forward Voltage[1,4]	V_{SD}	I_F = 20A, V_{GS} = 0V			1.2	V
Reverse Recovery Time[5]	t_{rr}	I_F = 20A, dI_F/dt = 100A / μS		7.3		nS
Peak Reverse Recovery Current[5]	$I_{RM(REC)}$			0.6		A
Reverse Recovery Charge[5]	Q_{rr}			2.3		nC

[1]Pulse test : Pulse Width ≦ 300 usec, Duty Cycle ≦ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

[4]Guarantee by FT test Item

[5]Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪Q1_TYPICAL CHARACTERISTICS

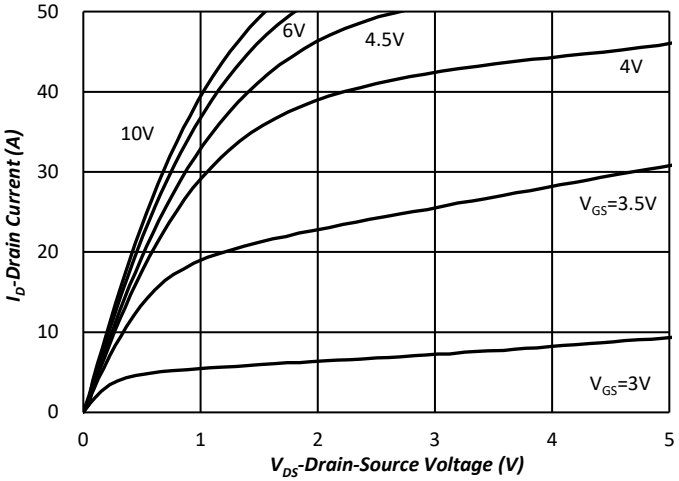


Fig.1 Typical Output Characteristics

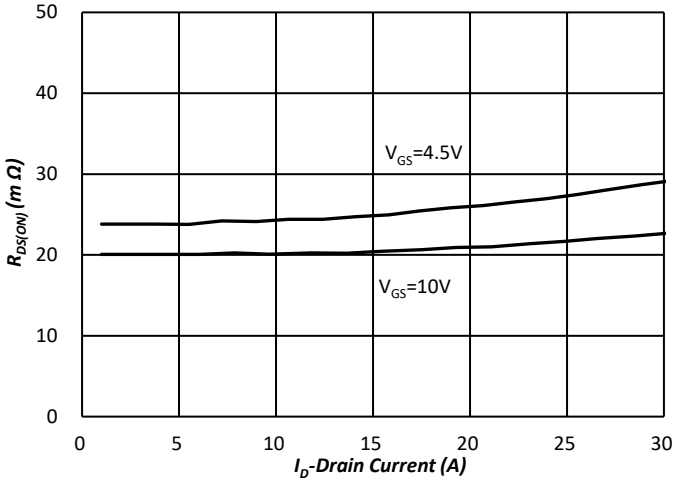


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

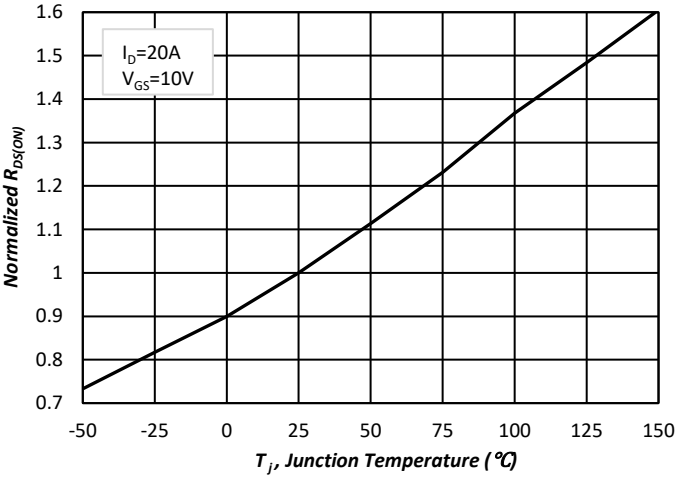


Fig.3 Normalized On-Resistance v.s. Junction Temperature

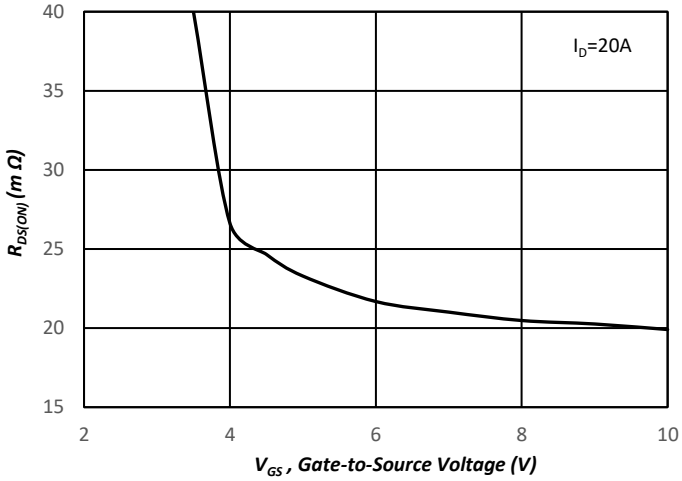


Fig.4 On-Resistance v.s. Gate Voltage

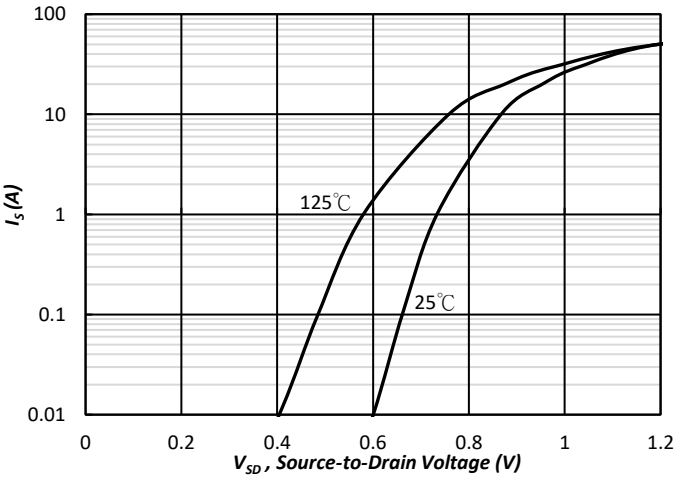


Fig.5 Forward Characteristic of Reverse Diode

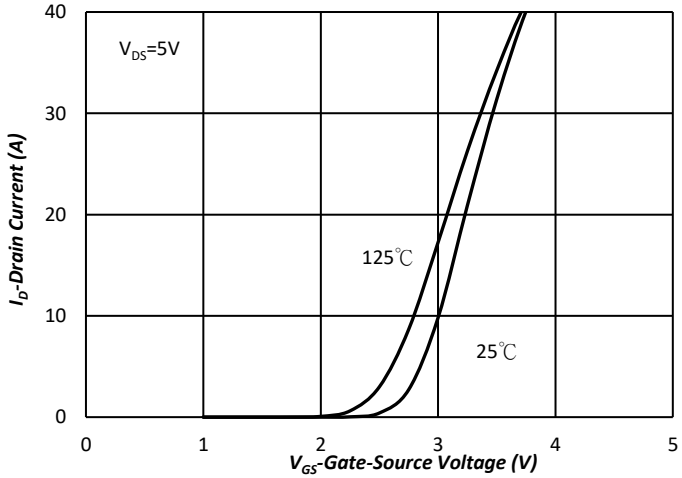


Fig.6 Transfer Characteristics

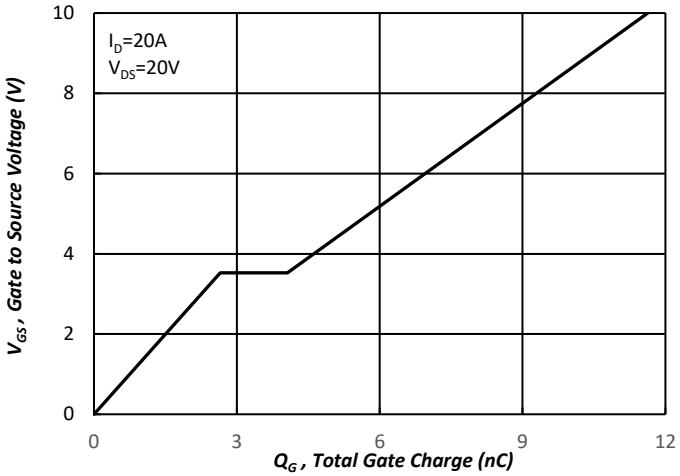


Fig.7 Gate Charge Characteristics

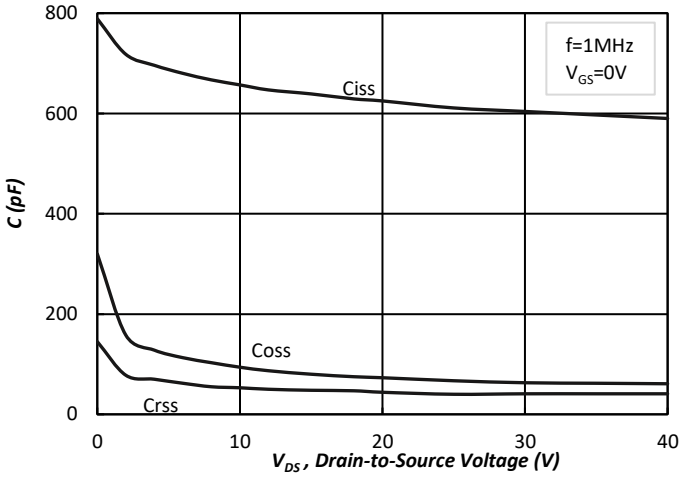


Fig.8 Typical Capacitance Characteristics

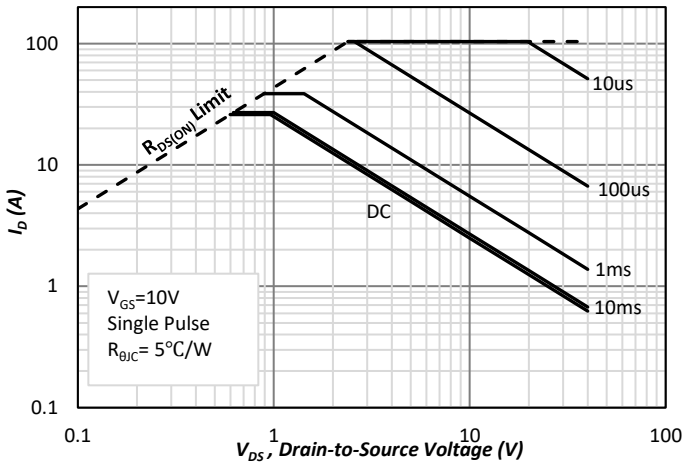


Fig 9. Maximum Safe Operating Area

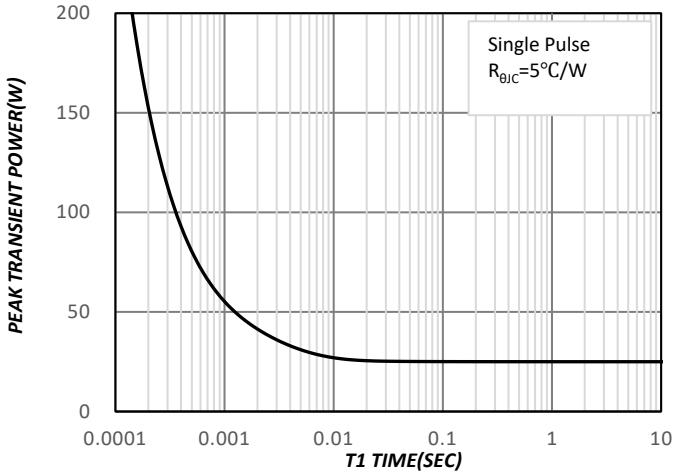


Fig 10. Single Pulse Maximum Power Dissipation

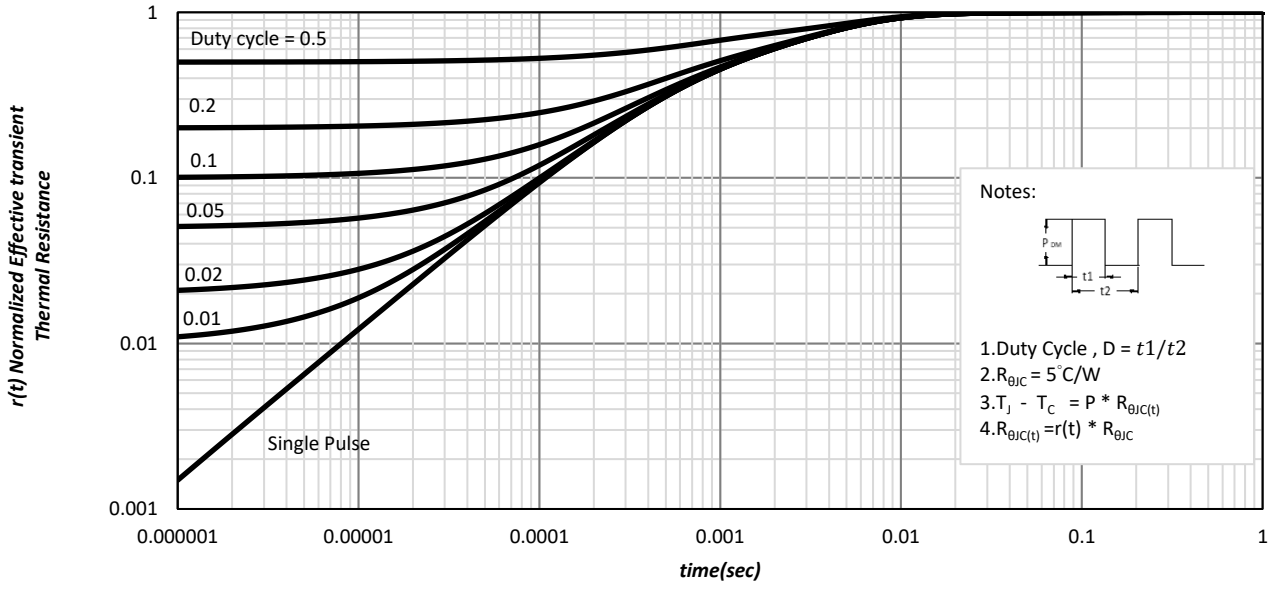


Fig 11. Effective Transient Thermal Impedance

▪ Q2_ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage[4]	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	40			V
Gate Threshold Voltage[4]	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.2	1.8	2.5	
Gate-Body Leakage[4]	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current[4]	I_{DSS}	V_{DS} = 40V, V_{GS} = 0V			1	μA
		V_{DS} =40V, V_{GS} =0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	26			A
Drain-Source On-State Resistance[1,4]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 20A		19	23	mΩ
		V_{GS} = 4.5V, I_D = 15A		22	27	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 18A		48		S
DYNAMIC						
Input Capacitance[5]	C_{iss}	V_{GS} = 0V, V_{DS} = 20V, f = 1MHz		621		pF
Output Capacitance[5]	C_{oss}			73		
Reverse Transfer Capacitance[5]	C_{rss}			44		
Gate Resistance[4,5]	R_g	f = 1MHz		1.5		Ω
Total Gate Charge[1,2,5]	Q_g(V_{GS}=10V)	V_{DS} = 20V, V_{GS} = 10V, I_D = 20A		12		nC
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Turn-On Delay Time[1,2,5]	$t_{d(on)}$	V_{DS} = 20V, V_{GS} = 10V, I_D = 5A , Rg = 3Ω		6		nS
Rise Time[1,2,5]	t_r			7		
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Reverse Recovery Time[5]	t_{rr}	I_F =20A, dI_F/dt = 100A / μS		7.3		nS
Peak Reverse Recovery Current[5]	$I_{RM(REC)}$			0.6		A
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[1]Pulse test : Pulse Width ≦ 300 usec, Duty Cycle ≦ 2%.

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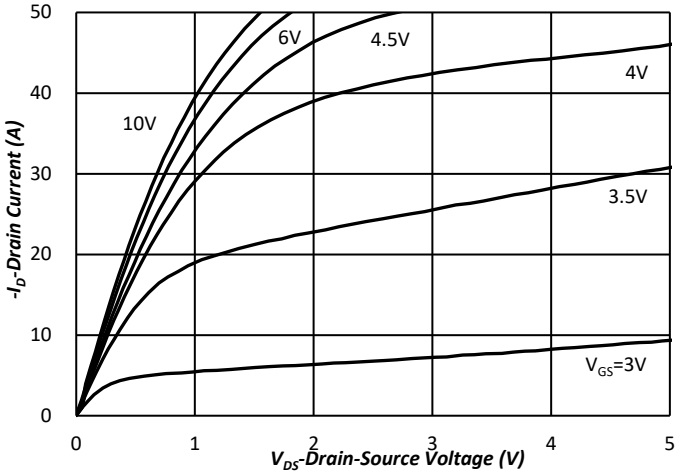


Fig.1 Typical Output Characteristics

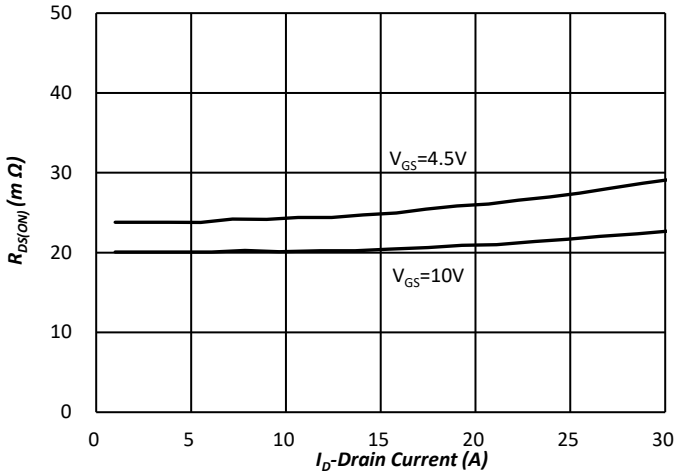


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

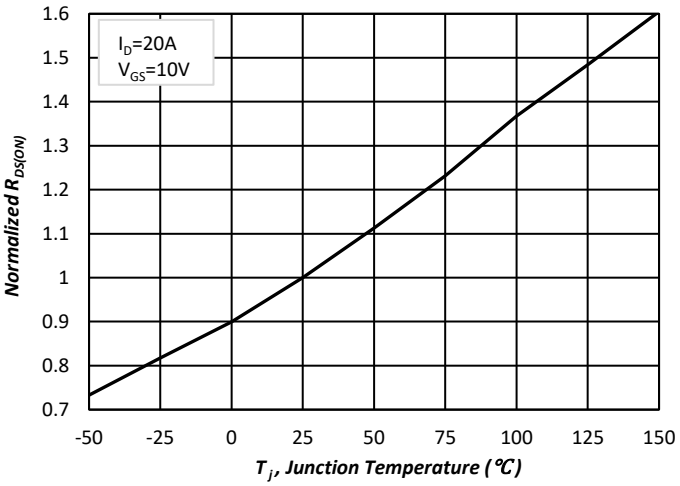


Fig.3 Normalized On-Resistance v.s. Junction Temperature

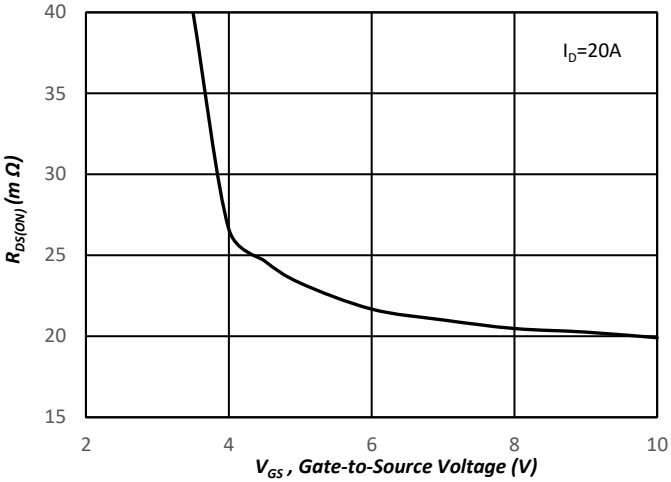


Fig.4 On-Resistance v.s. Gate Voltage

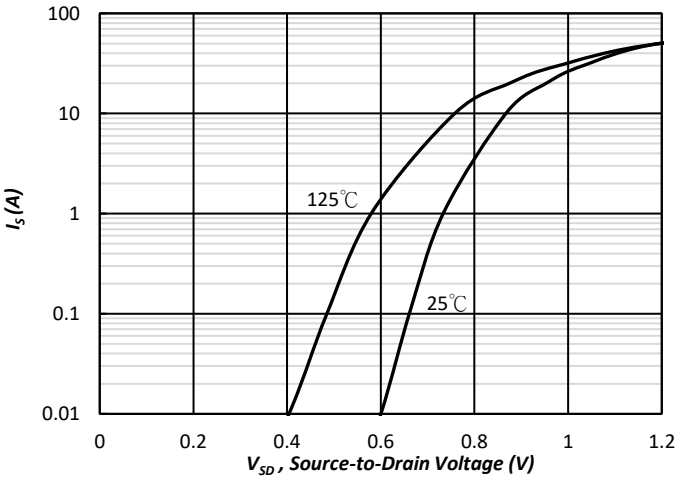


Fig.5 Forward Characteristic of Reverse Diode

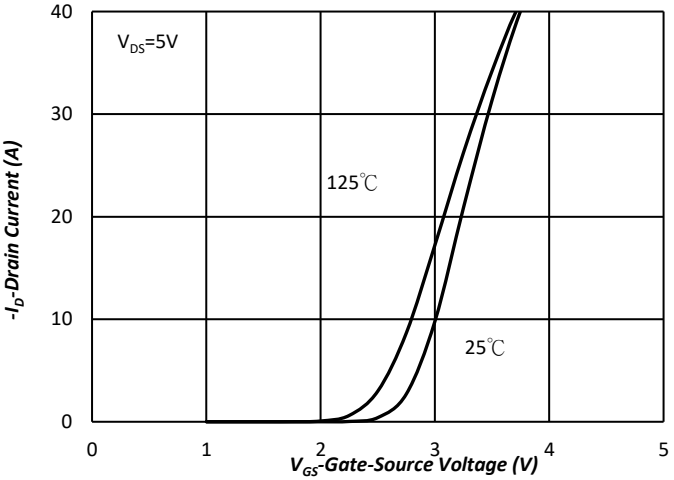


Fig.6 Transfer Characteristics

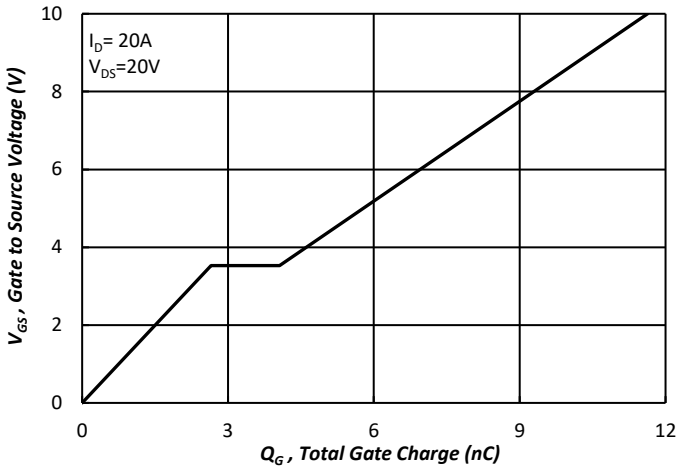


Fig.7 Gate Charge Characteristics

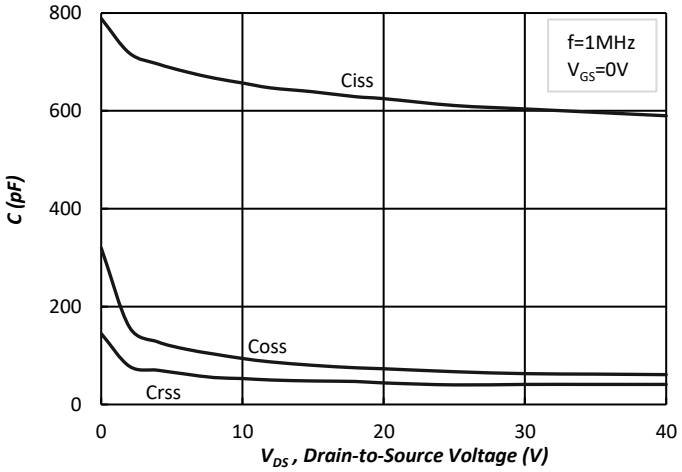
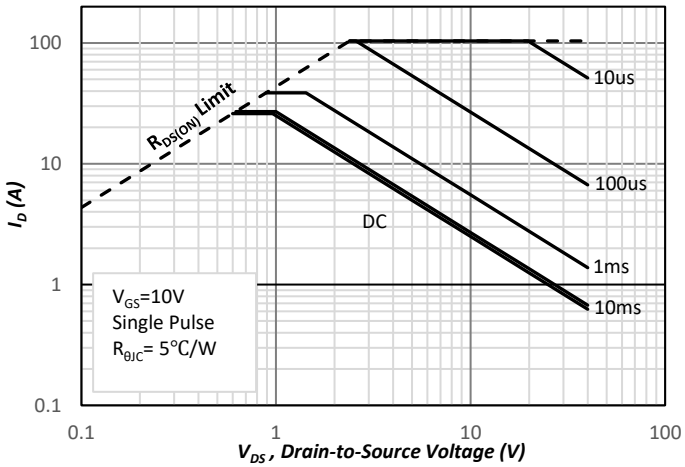


Fig.8 Typical Capacitance Characteristics



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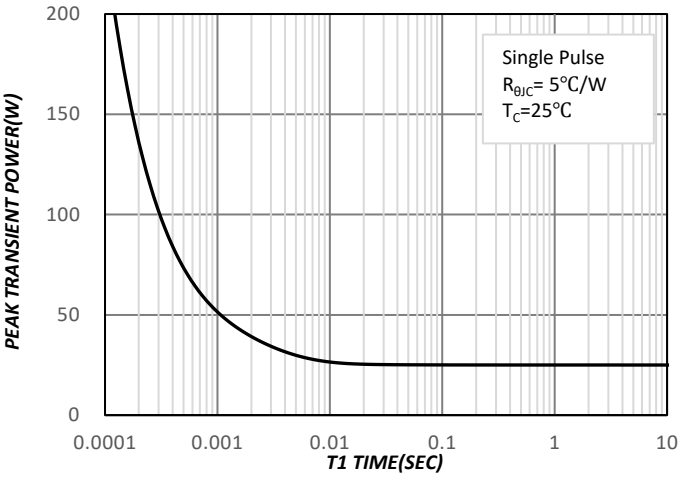

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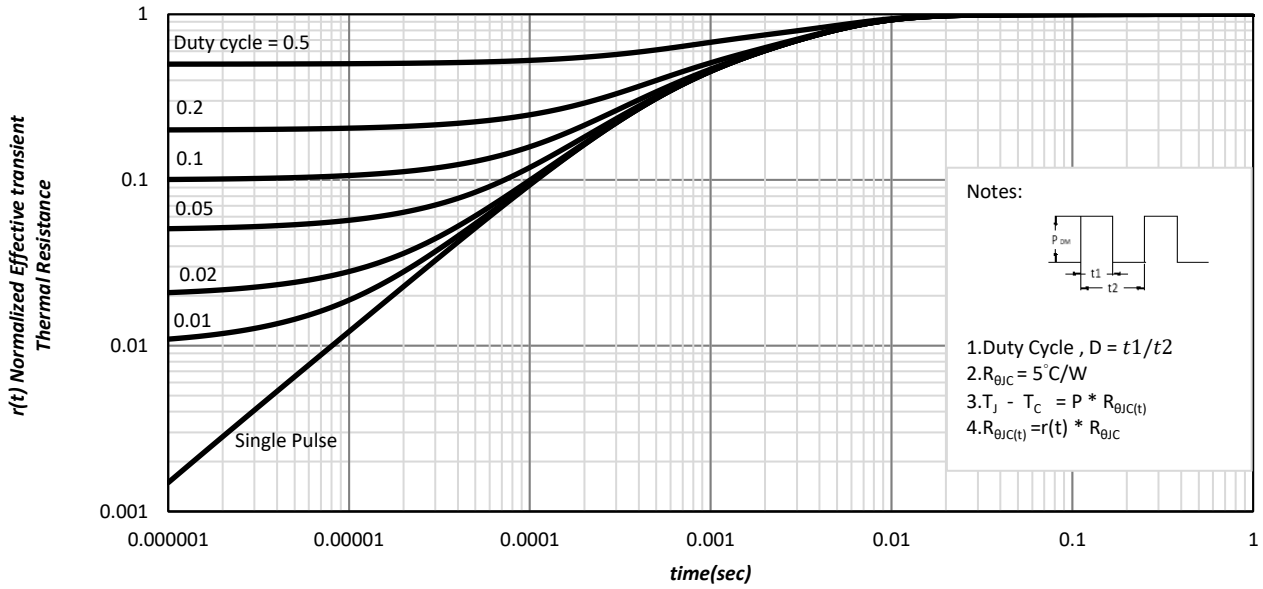
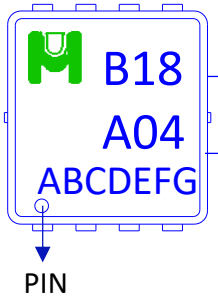


Fig 11. Effective Transient Thermal Impedance

Ordering & Marking Information:

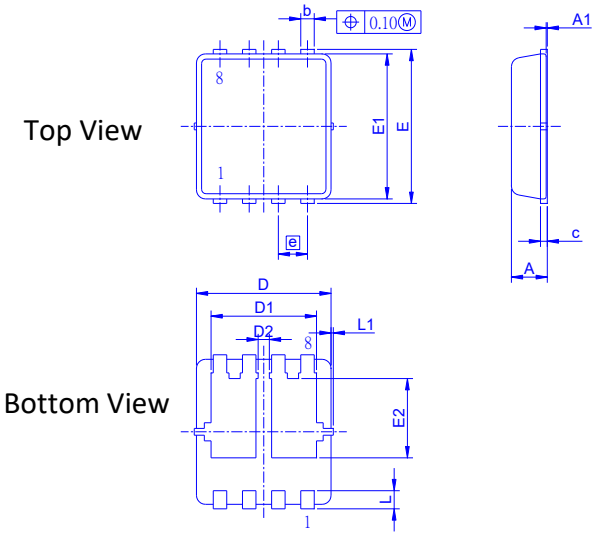
Device Name: EMB18A04V for EDFN3X3



B18A04: Device Name

ABCDEFG: Date Code
A: Assembly House
B: Year(A:2008 B:2009 C:2010….)
C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)
DEFG: Serial No.

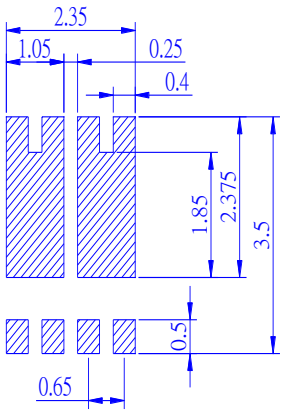
Outline Drawing



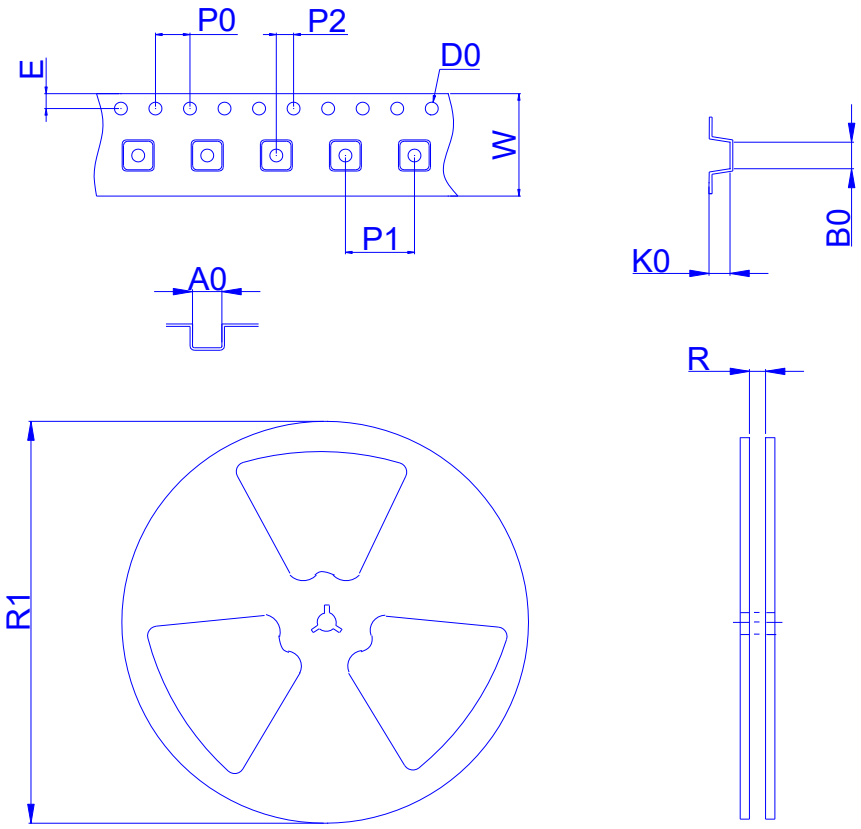
Dimension in mm

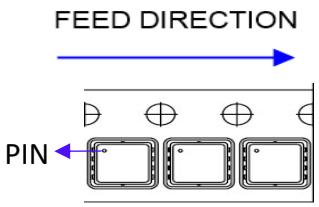
Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	e	L	L1	Θ1
Min.	0.65	0	0.20	0.10	2.90	2.15	0.28	3.10	2.90	1.53	0.55	0.30	-	0°
Typ.	0.75	-	0.30	0.15	3.00	2.47	0.38	3.20	3.00	1.81	0.65	0.40	0.075	10°
Max.	0.90	0.05	0.40	0.25	3.30	2.75	-	3.50	3.30	1.98	0.75	0.50	0.15	14°

Footprint



◆ Tape&Reel Information:5000pcs/Reel



Package	EDFN3X3
Reel	13”
Device orientation	

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	3.6	3.6	1.55	1.7	1.2	4	8	2	12	12.4	330
±	3.6	0.3	0.2	0.2	0.2	0.1	0.1	0.1	1	2	2