

Single P-Channel Logic Level Enhancement Mode Field Effect Transistor

▪ Product Summary:

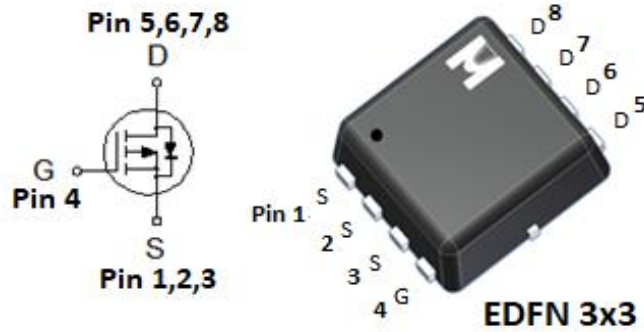
	P-CH
BV_{DSS}	-30V
$R_{DS(on)} (MAX.) @ V_{GS} = -10V$	12m Ω
$R_{DS(on)} (MAX.) @ V_{GS} = -4.5V$	20m Ω
$I_D @ T_C = 25^\circ C$	-56A
$I_D @ T_A = 25^\circ C$	-11A

Single P Channel MOSFET

UIS, Rg 100% Tested

RoHS & Halogen Free & TSCA Compliant

▪ Pin Description:



▪ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 25	V
Continuous Drain Current ¹	$T_C = 25^\circ C$	I_D	-56	A
	$T_C = 100^\circ C$		-35	
Continuous Drain Current ¹	$T_A = 25^\circ C$		-11	
	$T_A = 70^\circ C$		-8.7	
Pulsed Drain Current ¹		I_{DM}	-99	
Avalanche Current ^{1,4}		I_{AS}	-41	
Avalanche Energy ^{1,4}	$L = 0.1mH$	E_{AS}	84	mJ
Repetitive Avalanche Energy ^{2,4}	$L = 0.05mH$	E_{AR}	42	
Power Dissipation ¹	$T_C = 25^\circ C$	P_D	57	W
	$T_C = 100^\circ C$		23	
Power Dissipation ¹	$T_A = 25^\circ C$	P_D	2.2	W
	$T_A = 70^\circ C$		1.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ C$

▪ 100% UIS testing in condition of $V_D = 25V$, $L = 0.1mH$, $V_G = 10V$, $I_L = -25A$, $R_G = 25\Omega$, Rated $V_{DS} = -30V$ P-CH

▪ THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case		$R_{\theta JC}$		2.2	$^\circ C / W$
Junction-to-Ambient ³	$t \leq 10s$	$R_{\theta JA}$		25	
	Steady-State	$R_{\theta JA}$		58	

¹ Pulse width limited by maximum junction temperature.

² Duty cycle $< 1\%$

³ The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ C$.

⁴ Guarantee by Engineering test

▪ ELECTRICAL CHARACTERISTICS (T_j = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-30			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1.2	-1.7	-2.5	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±25V			±500	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = -30V, V _{GS} = 0V			-1	μA
		V _{DS} = -30V, V _{GS} = 0V, T _J = 125 °C			-25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = -10V, V _{GS} = -10V	-56			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = -10V, I _D = -13A		9.5	12	mΩ
		V _{GS} = -4.5V, I _D = -9A		14	20	
Forward Transconductance ¹	g _{fs}	V _{DS} = -5V, I _D = -10A		32		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = -15V, f = 1MHz		1750		pF
Output Capacitance ⁵	C _{oss}			270		
Reverse Transfer Capacitance ⁵	C _{rss}			185		
Gate Resistance ^{4,5}	R _g	f = 1MHz		4.8		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =-10V)	V _{DS} = -15V, V _{GS} = -10V, I _D = -13A		35		nC
	Q _g (V _{GS} =-4.5V)			17		
Gate-Source Charge ^{1,2,5}	Q _{gs}			6.1		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			6.8		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = -15V, V _{GS} = -10V, I _D = -5A , R _g = 3Ω		6.0		nS
Rise Time ^{1,2,5}	t _r			7.0		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			42		
Fall Time ^{1,2,5}	t _f			27		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				-47	A
Pulsed Current ³	I _{SM}				-99	
Forward Voltage ^{1,4}	V _{SD}	I _F = -13A, V _{GS} = 0V			-1.2	V
Reverse Recovery Time ⁵	t _{rr}	I _F = -13A, dI _F /dt = 100A / μS		9.5		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			0.4		A
Reverse Recovery Charge ⁵	Q _{rr}			3.9		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.



•TYPICAL CHARACTERISTICS

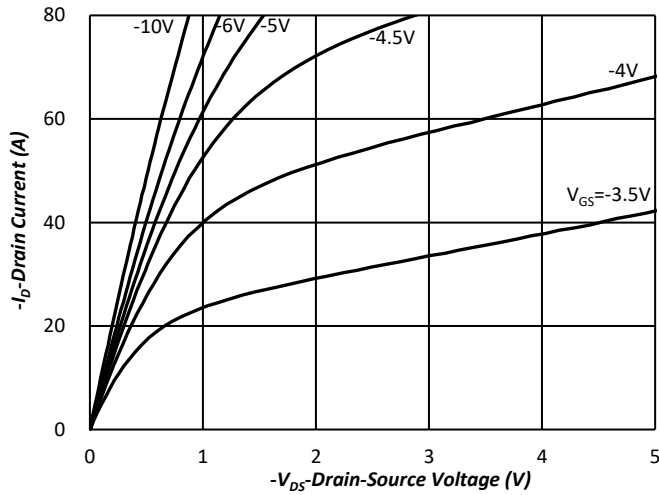


Fig.1 Typical Output Characteristics

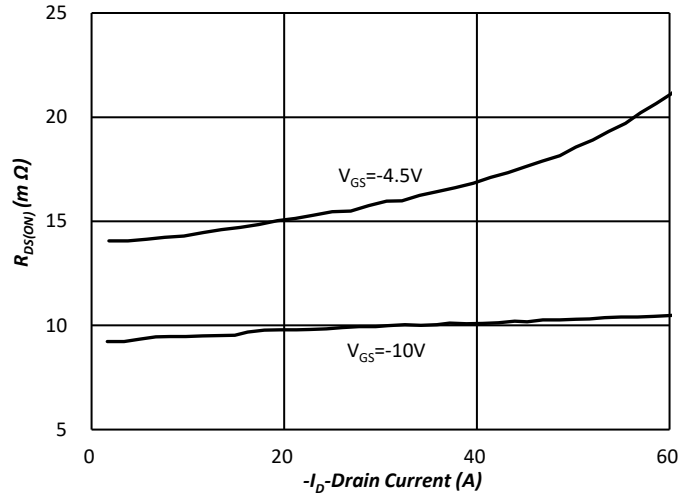


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

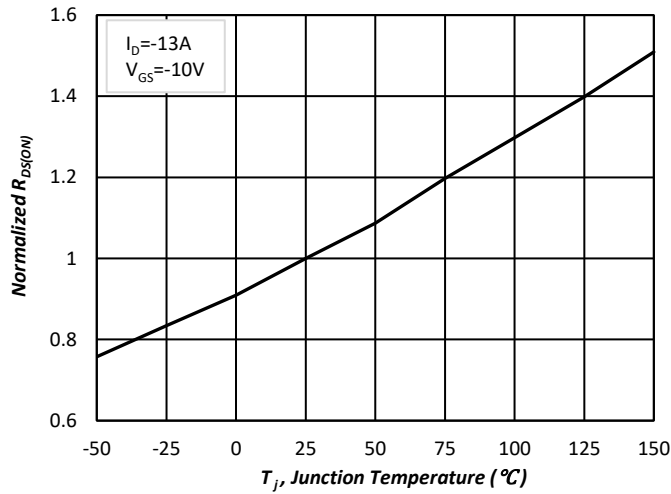


Fig.3 Normalized On-Resistance v.s. Junction Temperature

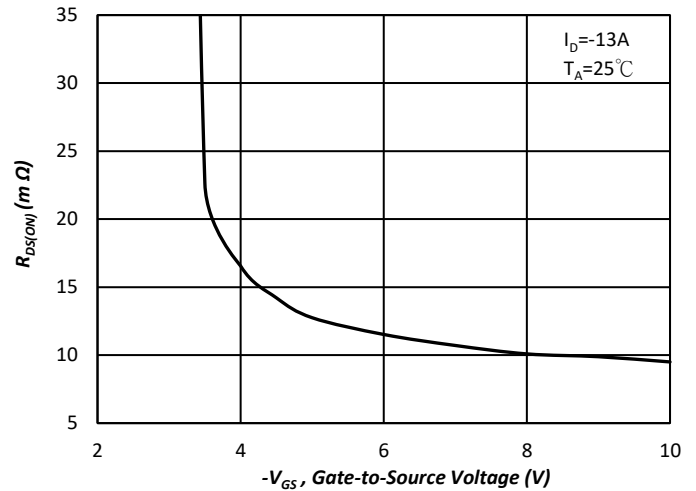


Fig.4 On-Resistance v.s. Gate Voltage

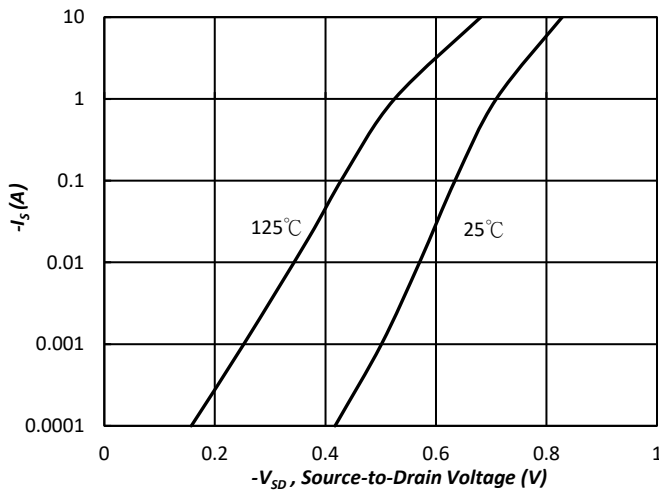


Fig.5 Forward Characteristic of Reverse Diode

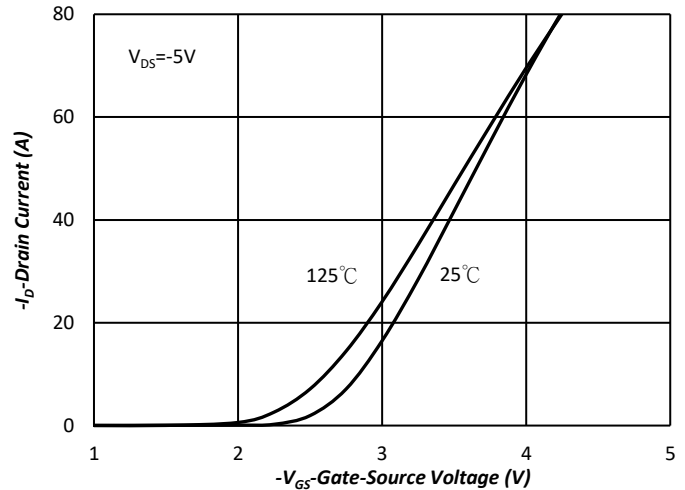


Fig.6 Transfer Characteristics

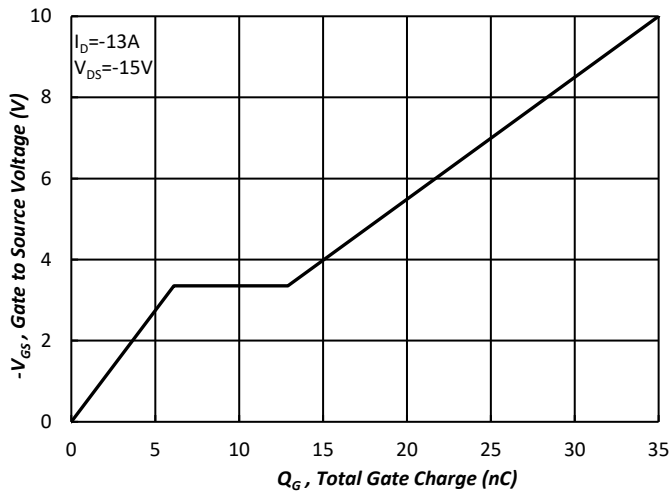


Fig.7 Gate Charge Characteristics

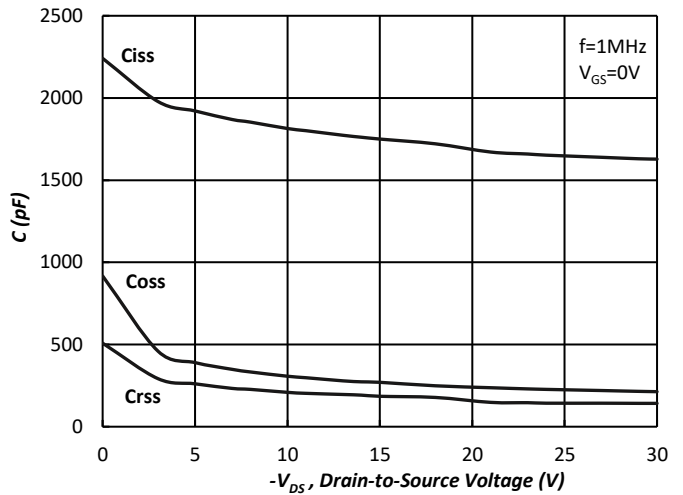


Fig.8 Typical Capacitance Characteristics

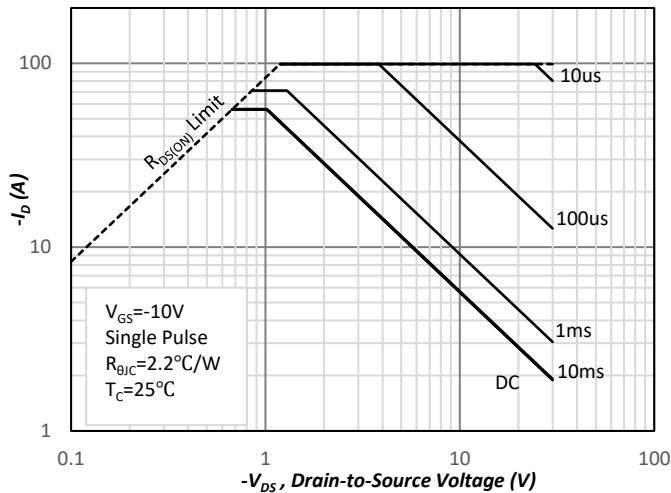


Fig.9. Maximum Safe Operating Area

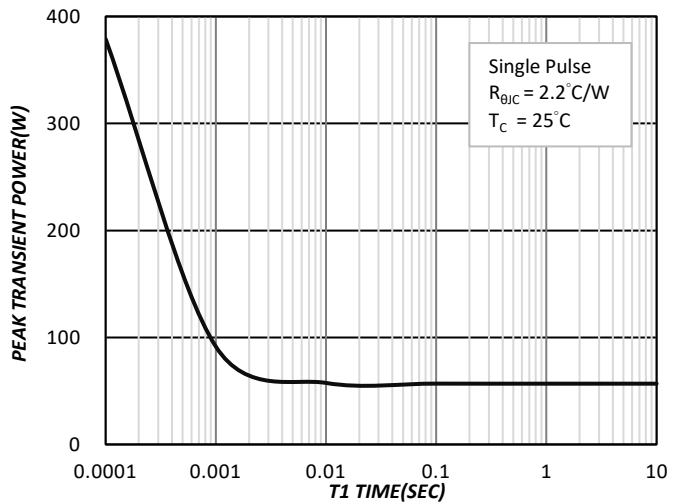


Fig.10. Single Pulse Maximum Power Dissipation

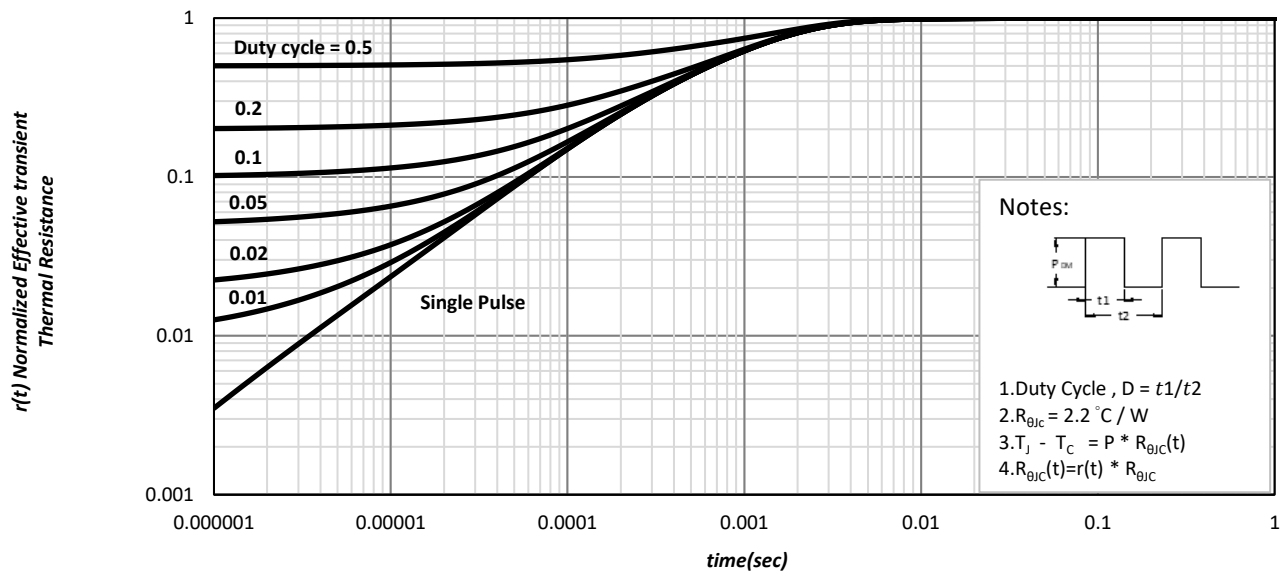


Fig.11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMB12P03V for EDFN 3x3



B12P03: Device Name

ABCDEFG: Date Code

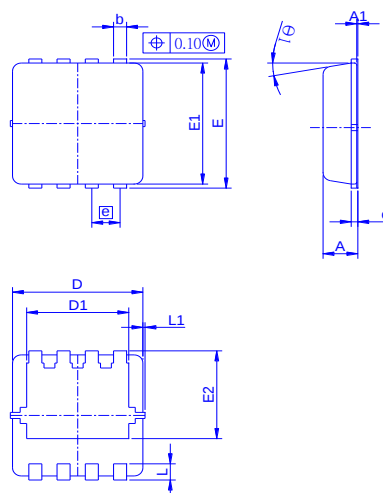
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

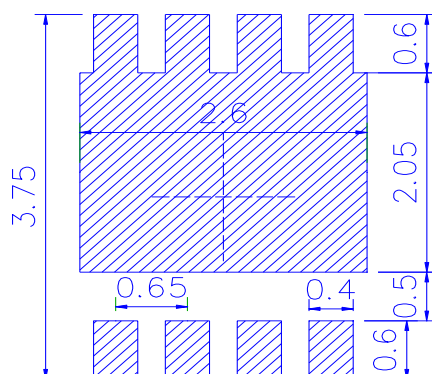
DEFG: Serial No.

Outline Drawing

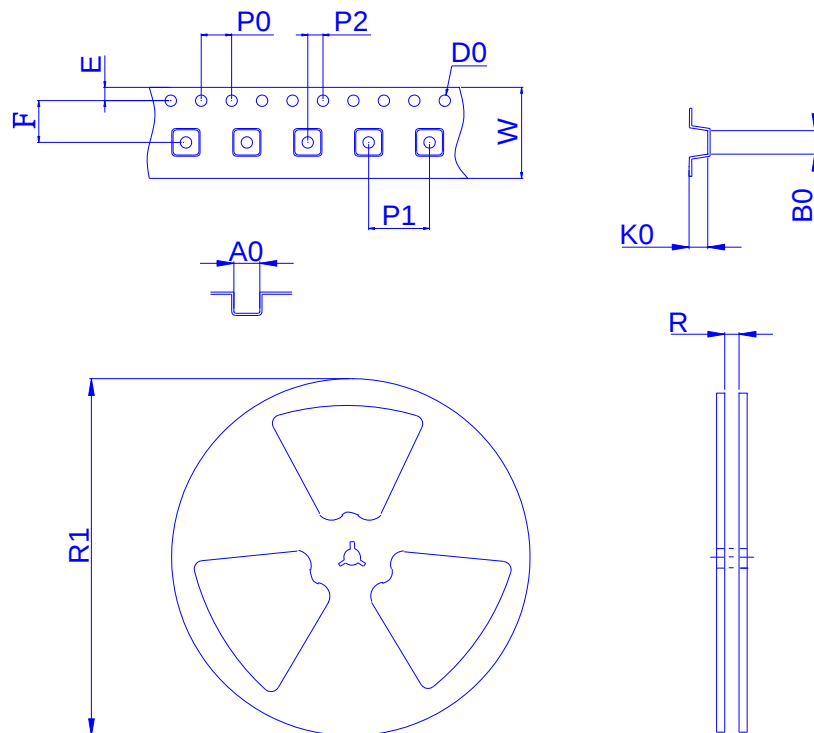


Dimension	A	A1	b	c	D	D1	E	E1	E2	e	L	L1	Θ1
Min.	0.650	0	0.200	0.100	2.900	2.150	3.100	2.900	1.530	0.550	0.250	-	0°
Typ.	0.750	-	0.300	0.150	3.000	2.450	3.200	3.000	1.970	0.650	0.400	0.075	10°
Max.	0.900	0.050	0.400	0.250	3.300	2.740	3.500	3.300	2.590	0.750	0.600	0.150	14°

Footprint



◆ Tape&Reel Information:5000pcs/Reel



Package	EDFN3X3
Reel	13"
Device orientation	FEED DIRECTION

Dimension in mm

Dimension	Carrier tape										Reel	
	A0	B0	D0	E	F	K0	P0	P1	P2	W	R	R1
Typ.	3.6	3.6	1.55	1.7	5.5	1.1	4	8	2	12	12.4	330
±	0.3	0.3	0.2	0.2	0.05	0.1	0.1	0.1	0.1	0.3	2	2