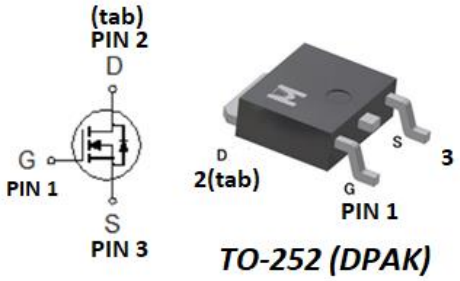
N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	100V
$R_{DSON\ (MAX.)}$	12mΩ
I_D	68A



TO-252 (DPAK)

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	68	A
	T_C = 100 °C		43	
Pulsed Drain Current[1]		I_{DM}	150	
Avalanche Current		I_{AS}	18	
Avalanche Energy	L = 0.1mH, ID=18A, RG=25Ω	E_{AS}	16.2	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	8.1	
Power Dissipation	T_C = 25 °C	P_D	89	W
	T_C = 100 °C		35	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		1.4	°C / W
Junction-to-Ambient	$R_{\theta JA}$		62.5	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

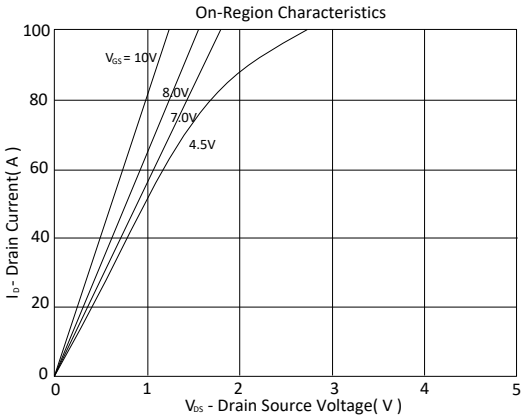
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.0	2.0	3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80V, V_{GS} = 0V			1	μA
		V_{DS} = 70V, V_{GS} = 0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 10V	68			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 12A		9.5	12	mΩ
		V_{GS} = 4.5V, I_D = 10A		11.5	15	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 12A		45		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 50V, f = 1MHz		2130		pF
Output Capacitance	C_{oss}			336		
Reverse Transfer Capacitance	C_{rss}			29		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz		1.5		Ω
Total Gate Charge[1,2]	Q_g(V_{GS}=10V)	V_{DS} = 50V, V_{GS} = 10V, I_D = 12A		38		nC
	Q_g(V_{GS}=4.5V)			23		
Gate-Source Charge[1,2]	Q_{gs}			10		
Gate-Drain Charge[1,2]	Q_{gd}			8.2		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 50V, I_D = 12A, V_{GS} = 10V, R_{GS} = 6Ω		6		nS
Rise Time[1,2]	t_r			10		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			8		
Fall Time[1,2]	t_f			25		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				68	A
Pulsed Current[3]	I_{SM}				150	
Forward Voltage[1]	V_{SD}	I_F = 12A, V_{GS} = 0V			1.2	V
Reverse Recovery Time	t_{rr}	I_F = 12A, dI_F/dt = 100A / μS		30		nS
Reverse Recovery Charge	Q_{rr}			130		nC

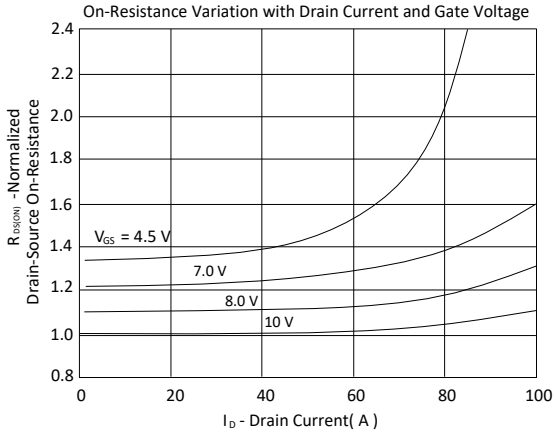
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

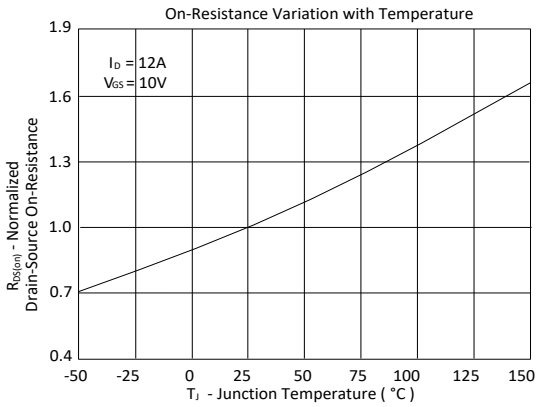
[2]Independent of operating temperature.

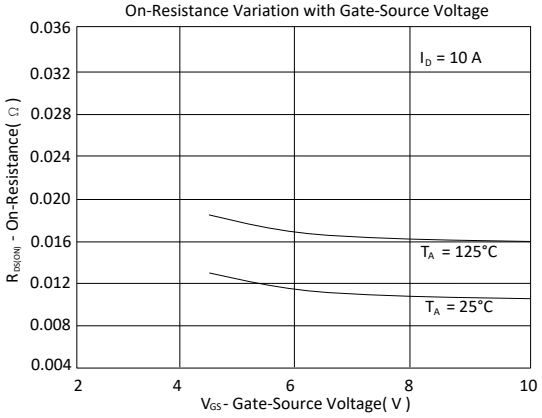
[3]Pulse width limited by maximum junction temperature.

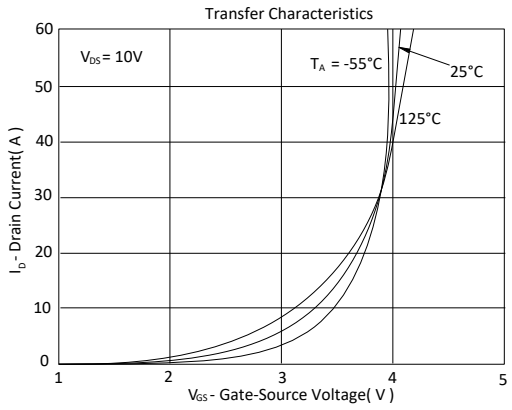
TYPICAL CHARACTERISTICS

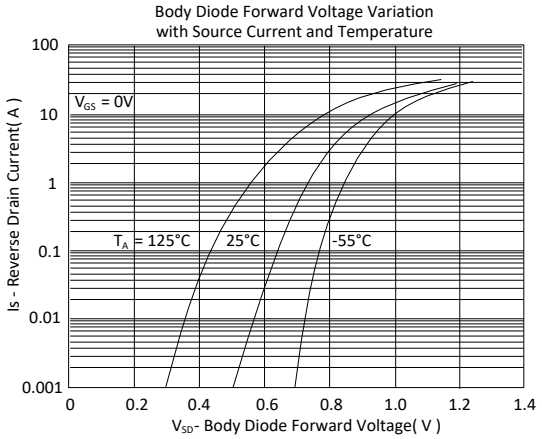




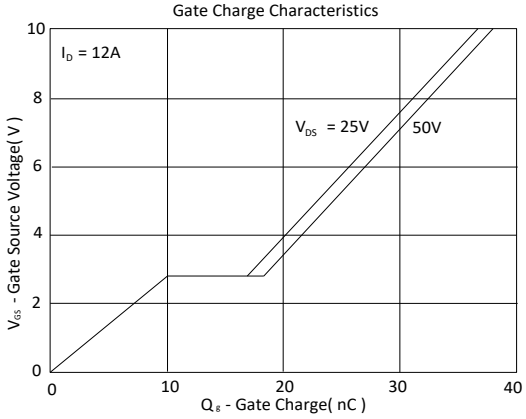




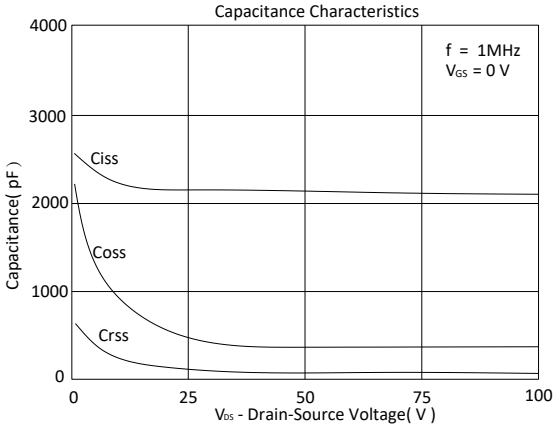




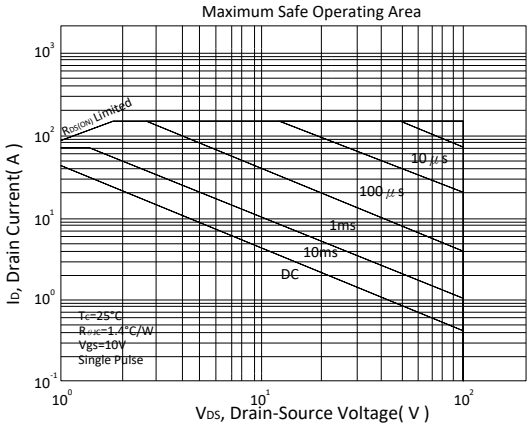
Gate Charge Characteristics



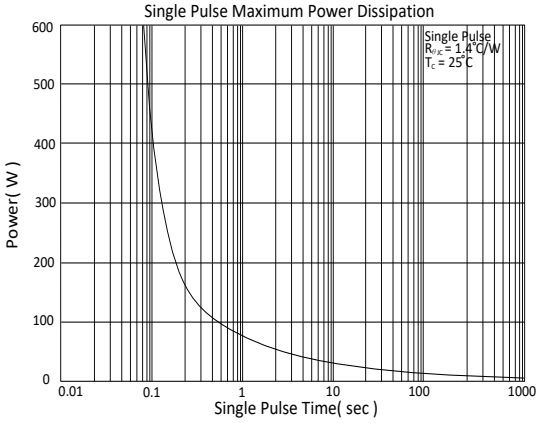
Capacitance Characteristics



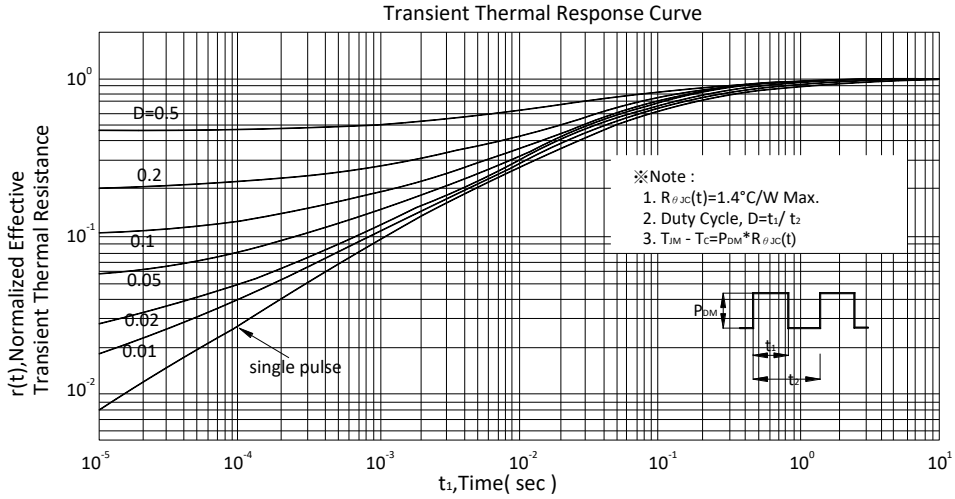
Maximum Safe Operating Area



Single Pulse Maximum Power Dissipation

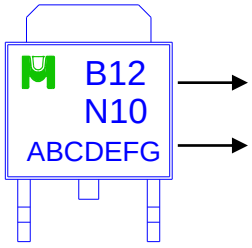


Transient Thermal Response Curve



Ordering & Marking Information:

Device Name: EMB12N10A for TO-252 [DPAK]



B12N10: Device Name

ABCDEFG: Date Code

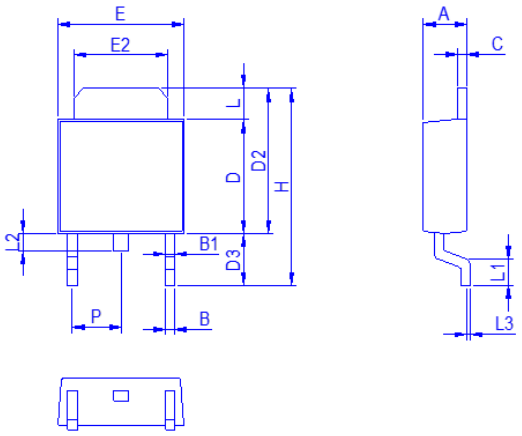
A: Assembly House

B: Year(A:2008 B:2009 C:2010….)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

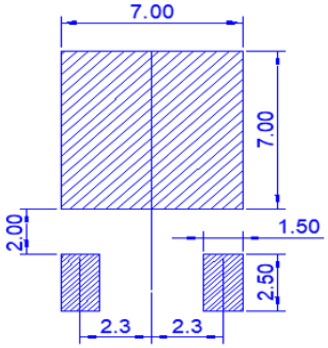
DEFG: Serial No.

Outline Drawing

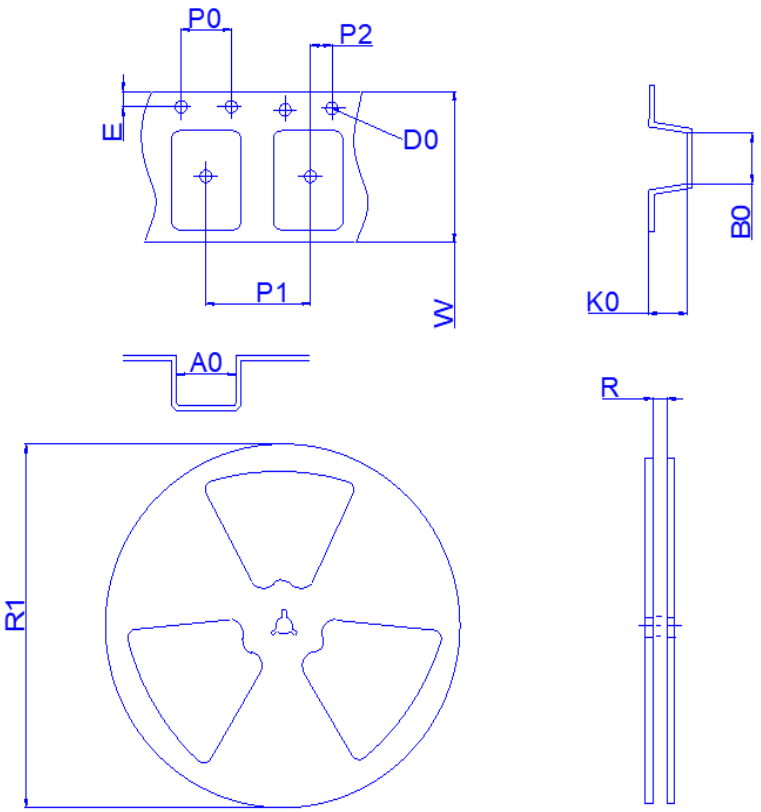


Dimension	A	B	B1	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.1	0.62	0.65	0.45	5.96	6.8	2.6	6.3	4.9	9.3	0.8	1.2	0.5	0	2.1
Typ.	2.25	0.76	0.9	0.67	6.1	7.15	2.8	6.5	5.2	9.9	1.1	1.65	0.8	0.1	2.25
Max.	2.4	0.9	1.15	0.89	6.24	7.5	3	6.7	5.5	10.5	1.4	2.1	1.1	0.2	2.4

Footprint



Tape&Reel Information:2500pcs/Reel



產品別	TO252-2
Reel尺寸	13”
編帶方式	FEED DIRECTION

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	6.9	10.5	1.55	1.75	2.7	4	8	2	16	17	330
±	1	1	0.2	0.1	0.2	0.2	0.1	0.1	0.3	2	2