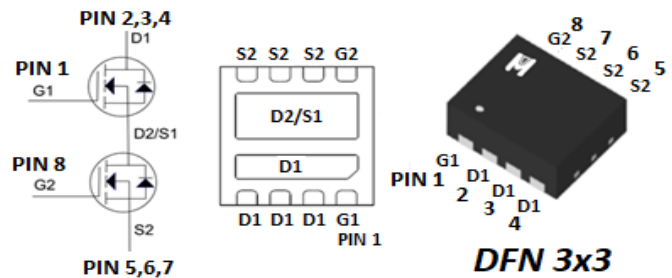


Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

•Product Summary:

	Q1	Q2
BVDSS	30V	30V
$R_{DS(on)} (MAX.) @ V_{GS}=10V$	20.0mΩ	9.0mΩ
$R_{DS(on)} (MAX.) @ V_{GS}=4.5V$	30.0mΩ	15.0mΩ
$I_D @ T_C=25^{\circ}C$	32.0A	49.0A
$I_D @ T_A=25^{\circ}C$	8.0A	13.0A

• Pin Description:



Dual N Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

•ABSOLUTE MAXIMUM RATINGS ($T_C = 25^{\circ}C$ Unless Otherwise Noted)



PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
			Q1	Q2	
Gate-Source Voltage		V_{GS}	± 20	± 20	V
Continuous Drain Current	$T_C = 25^{\circ}C$	I_D	32	49	A
	$T_C = 100^{\circ}C$		20	31	
Continuous Drain Current	$T_A = 25^{\circ}C$	I_D	8	13	
	$T_A = 70^{\circ}C$		6	10	
Pulsed Drain Current ¹		I_{DM}	85	127	
Avalanche Current		I_{AS}	16	21	
Avalanche Energy	$L = 0.1mH$	EAS	12.8	22.1	mJ
Repetitive Avalanche Energy ²	$L = 0.05mH$	EAR	6.4	11.0	
Power Dissipation	$T_C = 25^{\circ}C$	P_D	35.7	35.7	W
	$T_C = 100^{\circ}C$		14.3	14.3	
Power Dissipation	$T_A = 25^{\circ}C$	P_D	2.5	2.5	W
	$T_A = 70^{\circ}C$		1.6	1.6	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		$^{\circ}C$

•THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM		UNIT
				Q1	Q2	
Junction-to-Case		$R_{\theta JC}$		3.5	3.5	$^{\circ}C/W$
Junction-to-Ambient ³	$t \leq 10s$	$R_{\theta JA}$		50	50	
	Steady-State	$R_{\theta JA}$		90	90	

¹Pulse width limited by maximum junction temperature.

²Duty cycle < 1%

³90 $^{\circ}C$ / W when mounted on a 1 in² pad of 2 oz copper.

⁴Guarantee by Engineering test

▪ Q1_ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250uA	30			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	1	1.6	3	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 24V, V _{GS} = 0V			1	uA
		V _{DS} =20V, V _{GS} =0V, T _J =125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	32			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 8A		12.5	20	mΩ
		V _{GS} = 4.5V, I _D = 5A		18.9	30	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 5A		15		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		401		pF
Output Capacitance ⁵	C _{oss}			73		
Reverse Transfer Capacitance ⁵	C _{rss}			60		
Gate Resistance ^{4,5}	R _g	f = 1MHz		1.5		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 15V, V _{GS} = 10V, I _D = 8A		8.9		nC
	Q _g (V _{GS} =4.5V)			4.9		
Gate-Source Charge ^{1,2,5}	Q _{gs}			1.3		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			2.6		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 15V, V _{GS} = 10V, I _D = 5A , R _g = 6Ω		4.9		nS
Rise Time ^{1,2,5}	t _r			11.0		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			13.0		
Fall Time ^{1,2,5}	t _f			12.8		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				32	A
Pulsed Current ³	I _{SM}				85	
Forward Voltage ^{1,4}	V _{SD}	I _F = 10A, V _{GS} = 0V			1.3	V
Reverse Recovery Time ⁵	t _{rr}	I _F = 10A, dI _F /dt = 400A / uS		8.0		nS
Reverse Recovery Charge ⁵	Q _{rr}			9.8		nC

¹ Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

² Independent of operating temperature.

³ Pulse width limited by maximum junction temperature.

⁴ Guarantee by FT test Item

⁵ Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.



▪ Q1_TYPICAL CHARACTERISTICS

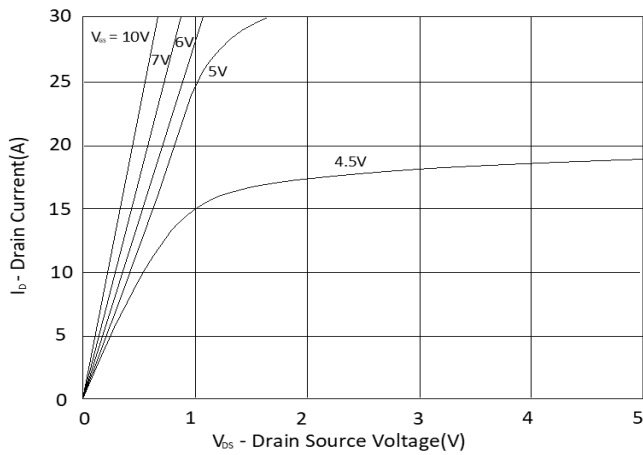


Fig.1 Typical Output Characteristics

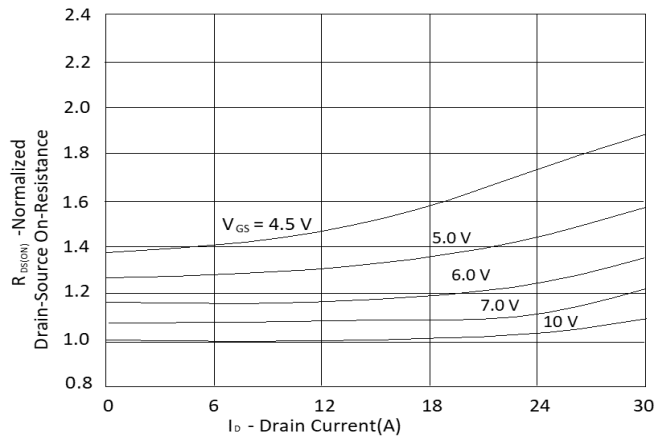


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

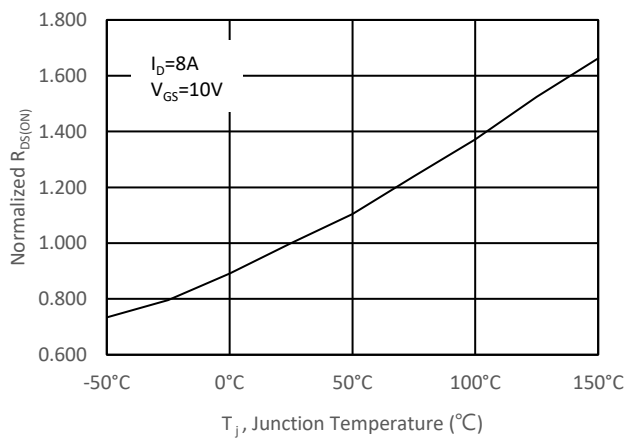


Fig.3 Normalized On-Resistance v.s. Junction Temperature

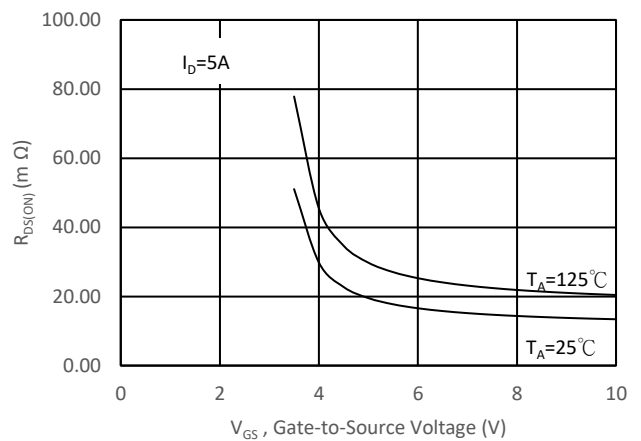


Fig.4 On-Resistance v.s. Gate Voltage

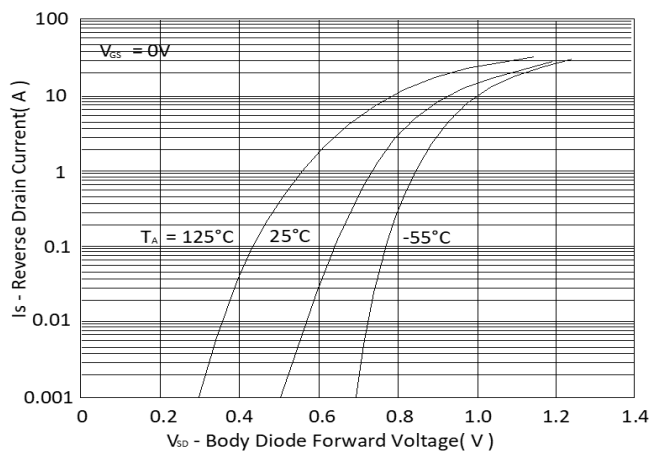


Fig.5 Forward Characteristic of Reverse Diode

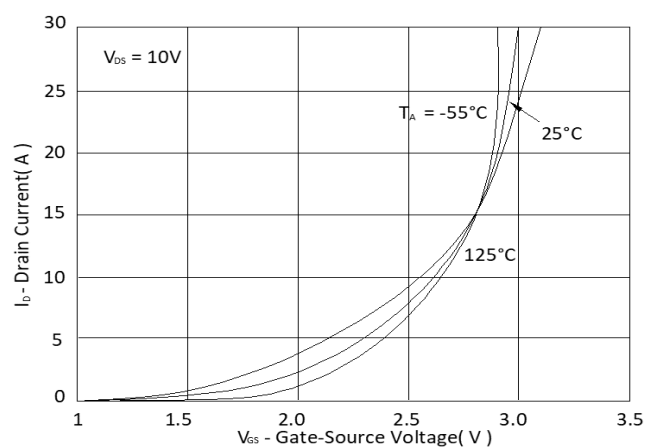


Fig.6 Transfer Characteristics

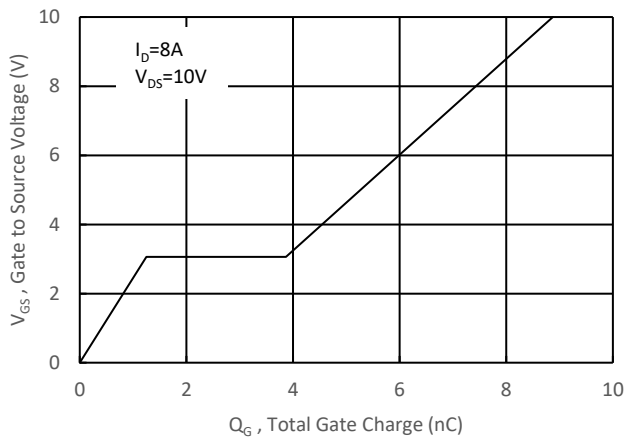


Fig.7 Gate Charge Characteristics

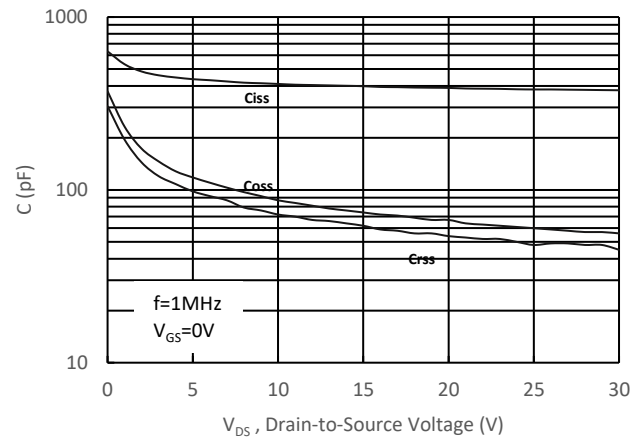


Fig.8 Typical Capacitance Characteristics

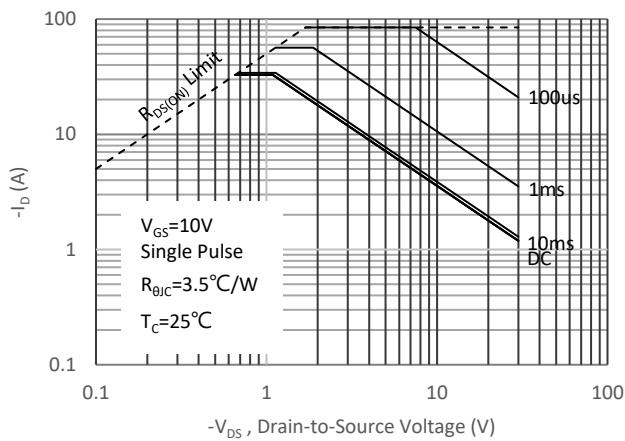


Fig 9. Maximum Safe Operating Area

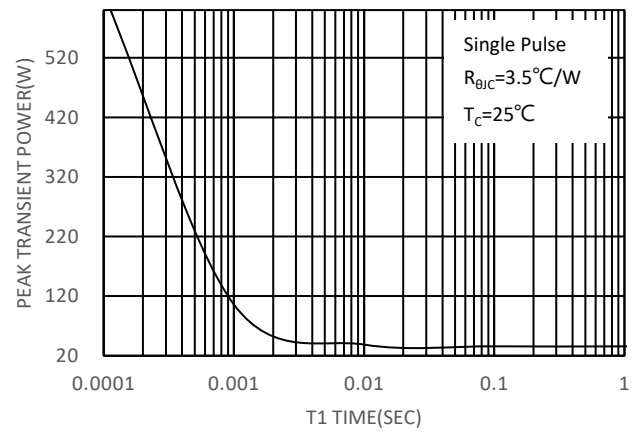


Fig 10. Single Pulse Maximum Power Dissipation

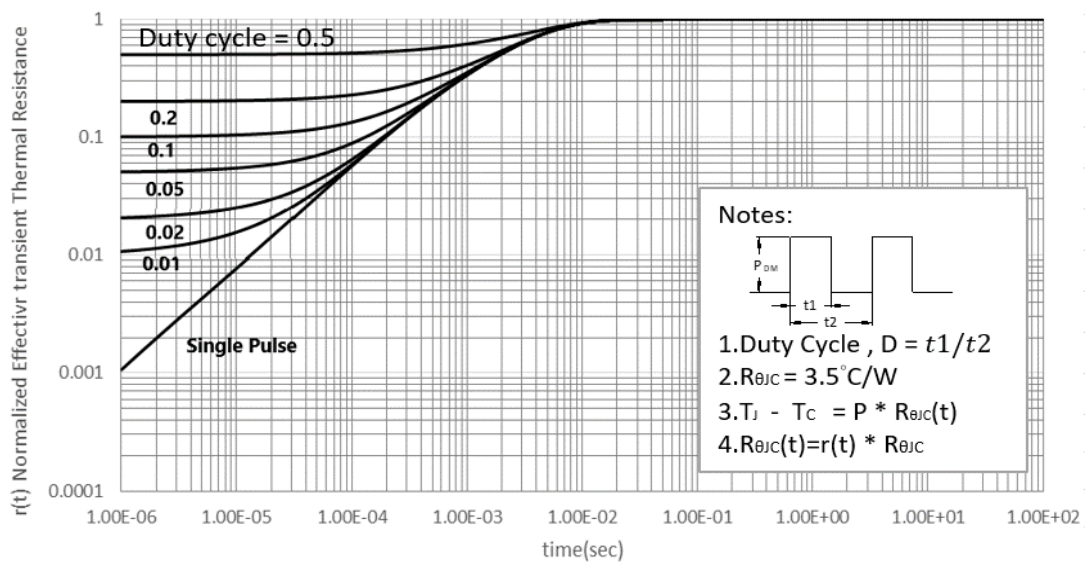


Fig 11. Effective Transient Thermal Impedance

▪ Q2_ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250uA	30			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	1	1.6	3	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 24V, V _{GS} = 0V			1	uA
		V _{DS} =20V, V _{GS} =0V, T _J =125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	49			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 10A		7	9	mΩ
		V _{GS} = 4.5V, I _D = 6A		11	15	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 6A		18		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		976		pF
Output Capacitance ⁵	C _{oss}			150		
Reverse Transfer Capacitance ⁵	C _{rss}			99		
Gate Resistance ^{4,5}	R _g	f = 1MHz		1.4		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 15V, V _{GS} = 10V, I _D = 10A		16.5		nC
	Q _g (V _{GS} =4.5V)			8.5		
Gate-Source Charge ^{1,2,5}	Q _{gs}			2.1		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			3.4		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 15V, V _{GS} = 10V, I _D = 5A , R _g = 6Ω		7.0		nS
Rise Time ^{1,2,5}	t _r			14.8		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			13.0		
Fall Time ^{1,2,5}	t _f			12.8		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				49	A
Pulsed Current ³	I _{SM}				127	
Forward Voltage ^{1,4}	V _{SD}	I _F = 15A, V _{GS} = 0V			1.3	V
Reverse Recovery Time ⁵	t _{rr}	I _F = 15A, dI _F /dt = 400A / uS		6.9		nS
Reverse Recovery Charge ⁵	Q _{rr}			6.2		nC

¹ Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

² Independent of operating temperature.

³ Pulse width limited by maximum junction temperature.

⁴ Guarantee by FT test Item

⁵ Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪ Q2_TYPICAL CHARACTERISTICS

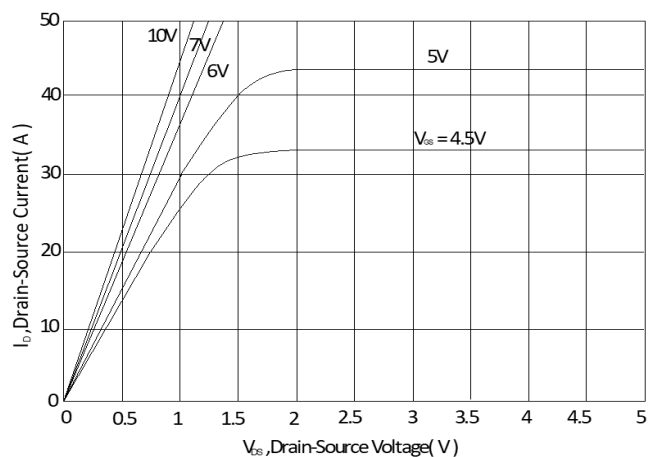


Fig.1 Typical Output Characteristics

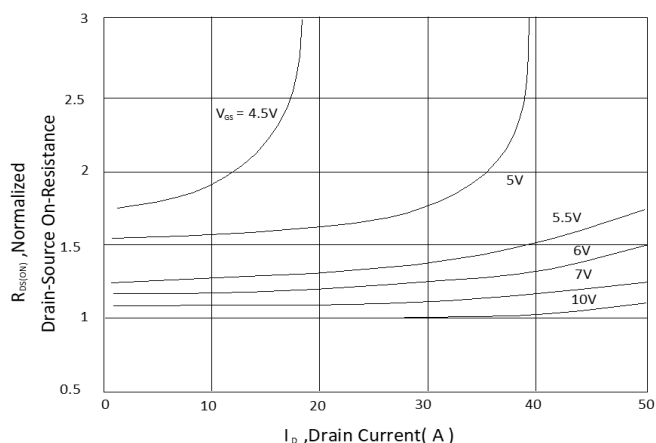


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

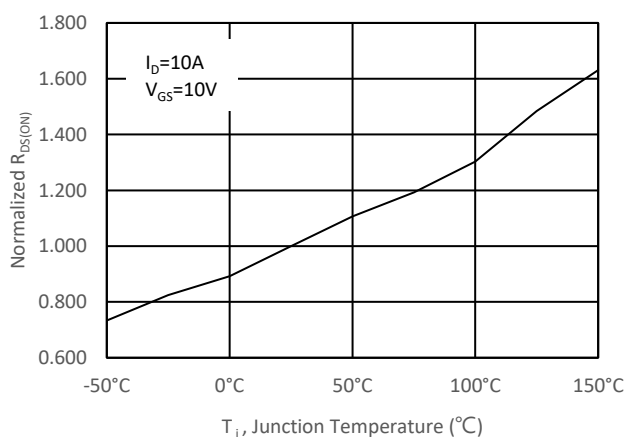


Fig.3 Normalized On-Resistance v.s. Junction Temperature

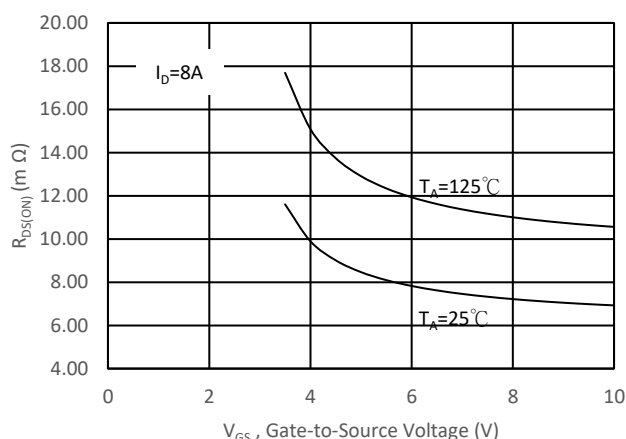


Fig.4 On-Resistance v.s. Gate Voltage

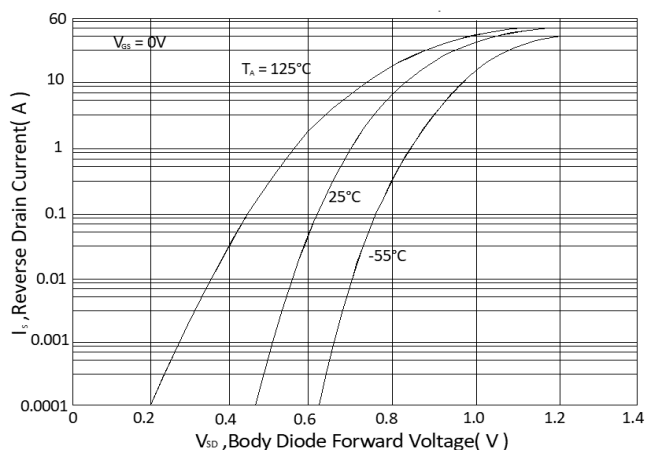


Fig.5 Forward Characteristic of Reverse Diode

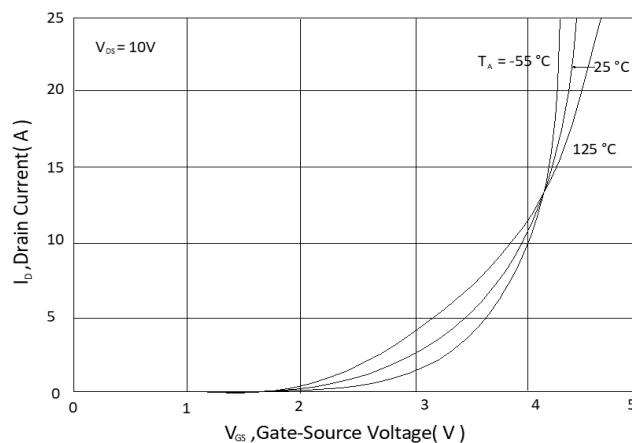


Fig.6 Transfer Characteristics

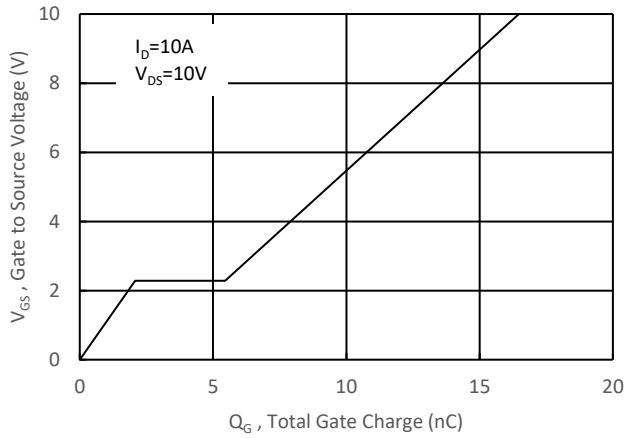


Fig.7 Gate Charge Characteristics

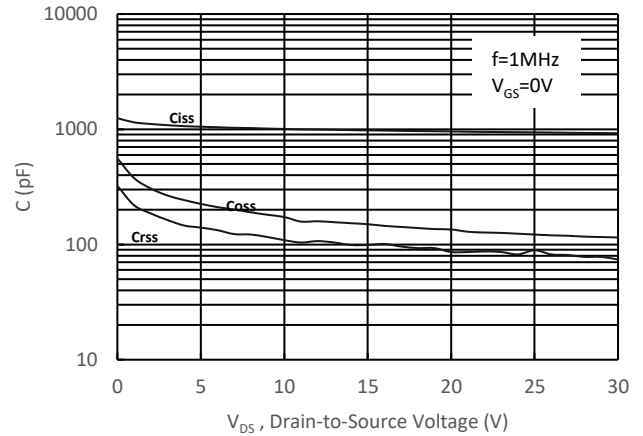


Fig.8 Typical Capacitance Characteristics

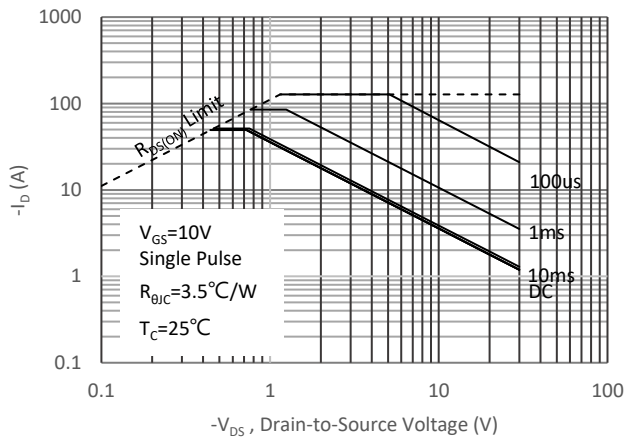


Fig 9. Maximum Safe Operating Area

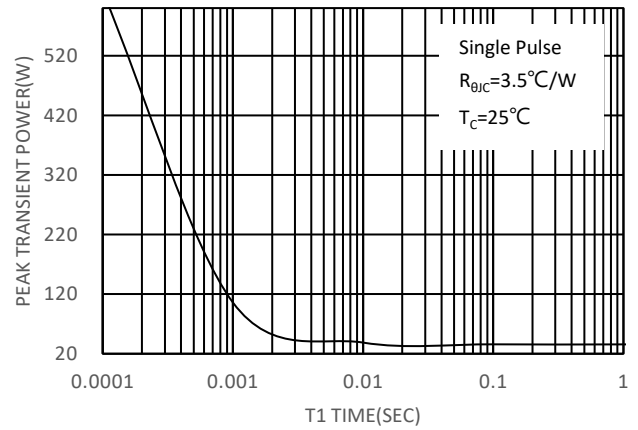


Fig 10. Single Pulse Maximum Power Dissipation

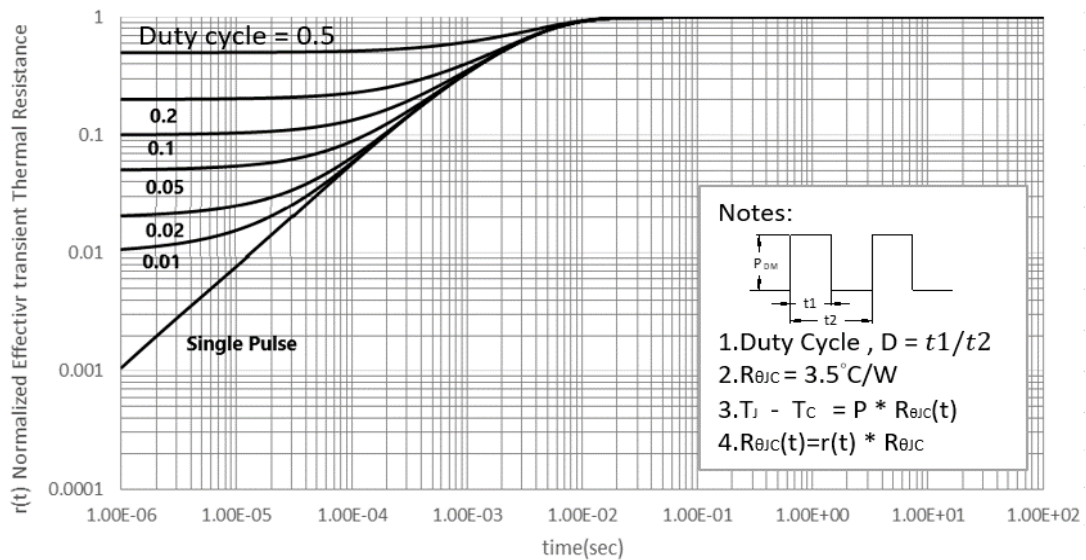


Fig 11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMB09K03VP for Asymmetric Dual DFN3X3



B09K03: Device Name

ABCDEFG: Date Code

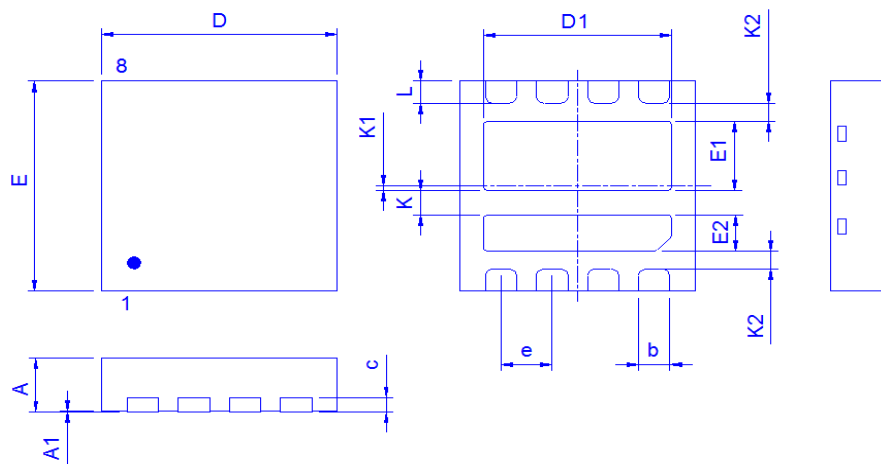
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

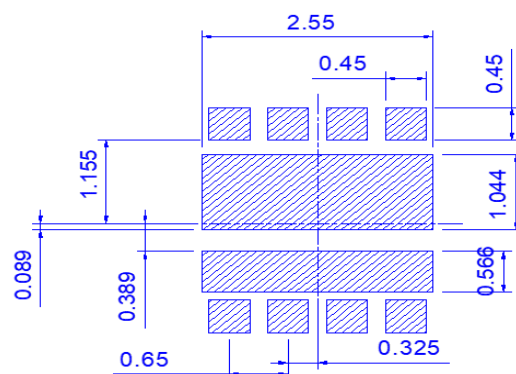
Outline Drawing



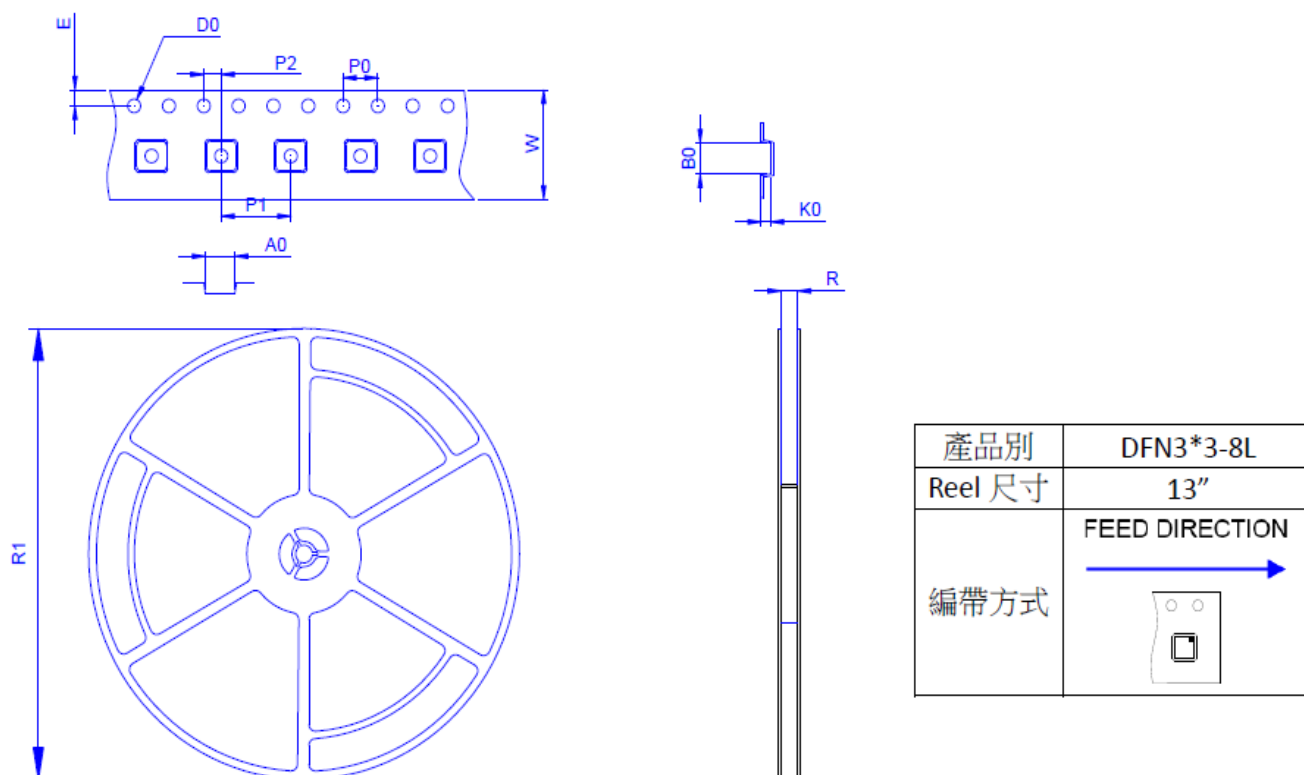
Dimension	A	A1	b	c	D	D1	E	E1	E2	e	L	K	K1
Min.	0.7	0	0.35		2.9	2.3	2.9	0.89	0.42		0.27		
Typ.	0.75		0.4	0.203	3	2.4	3	0.99	0.52	0.65	0.32	0.35	0.06
Max.	0.8	0.05	0.45		3.1	2.5	3.1	1.09	0.62		0.37		

Dimension	K2
Min.	
Typ.	0.25
Max.	

Footprint



◆ Tape&Reel Information:5000pcs/Reel



Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	3.30	3.30	1.50	1.75	1.10	4.00	8.00	2.00	12.00	12.40	330.00
±	0.30	0.20	0.20	0.20	0.40	0.20	0.20	0.20	0.50	REF	REF