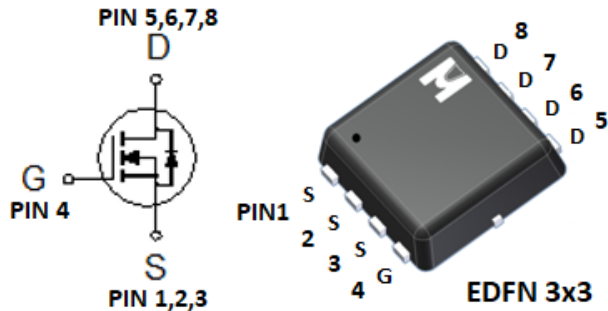


Single N-Channel Logic Level Enhancement Mode Field Effect Transistor

•Product Summary:

	N-CH
BV_{DSS}	30V
$R_{DSON (MAX.)@V_{GS}=10V}$	5.0mΩ
$R_{DSON (MAX.)@V_{GS}=4.5V}$	8.0mΩ
$I_D @T_C=25^{\circ}C$	79A
$I_D @T_A=25^{\circ}C$	16A

• Pin Description:



Single N Channel MOSFET

UIS, Rg 100% Tested

RoHS & Halogen Free & TSCA Compliant



• ABSOLUTE MAXIMUM RATINGS ($T_C = 25^{\circ}C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNIT
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D	$T_C = 25^{\circ}C$	79
		$T_C = 100^{\circ}C$	50
Continuous Drain Current	I_D	$T_A = 25^{\circ}C$	16
		$T_A = 70^{\circ}C$	13
Pulsed Drain Current ¹	I_{DM}	212	
Avalanche Current ^{1,4}	I_{AS}	60	
Avalanche Energy ^{1,4}	E_{AS}	18	mJ
Repetitive Avalanche Energy ^{2,4}	E_{AR}	90	
Power Dissipation ¹	P_D	$T_C = 25^{\circ}C$	50
		$T_C = 100^{\circ}C$	20
Power Dissipation ¹	P_D	$T_A = 25^{\circ}C$	2.1
		$T_A = 70^{\circ}C$	1.3
Operating Junction & Storage Temperature Range	T_j, T_{stg}	-55 to 150	°C

◆100% UIS testing in condition of $V_D=25V, L=0.01mH, V_G=10V, I_L=36A, R_G=25\Omega, \text{Rated } V_{DS}=30V \text{ N-CH}$

•THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		2.5	°C / W
Junction-to-Ambient ³	$t \leq 10s$	$R_{\theta JA}$	25	
	Steady-State	$R_{\theta JA}$	59	

¹Pulse width limited by maximum junction temperature.

²Duty cycle < 1%

³The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^{\circ}C$.

⁴Guarantee by Engineering test

▪ ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	30			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.2	1.7	2.5	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 30V, V _{GS} = 0V			1	μA
		V _{DS} = 30V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	79			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A		4.1	5.0	mΩ
		V _{GS} = 4.5V, I _D = 18A		6.0	8.0	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 20A		63		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		995		pF
Output Capacitance ⁵	C _{oss}			384		
Reverse Transfer Capacitance ⁵	C _{rss}			48		
Gate Resistance ^{4,5}	R _g	f = 1MHz		0.8		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 15V, V _{GS} = 10V, I _D = 20A		18		nC
	Q _g (V _{GS} =4.5V)			8.2		
Gate-Source Charge ^{1,2,5}	Q _{gs}			4.4		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			3.0		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}		V _{DS} = 15V, V _{GS} = 10V, I _D = 5A, R _g = 3Ω		5.9	
Rise Time ^{1,2,5}	t _r			6.9		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			14		
Fall Time ^{1,2,5}	t _f			3.6		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				42	A
Pulsed Current ³	I _{SM}				212	
Forward Voltage ^{1,4}	V _{SD}	I _F = 20A, V _{GS} = 0V		0.8	1.2	V
Reverse Recovery Time ⁵	t _{rr}	I _F = 20A, dI _F /dt = 400A / μS		11		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			2.0		A
Reverse Recovery Charge ⁵	Q _{rr}				12	

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.



• TYPICAL CHARACTERISTICS

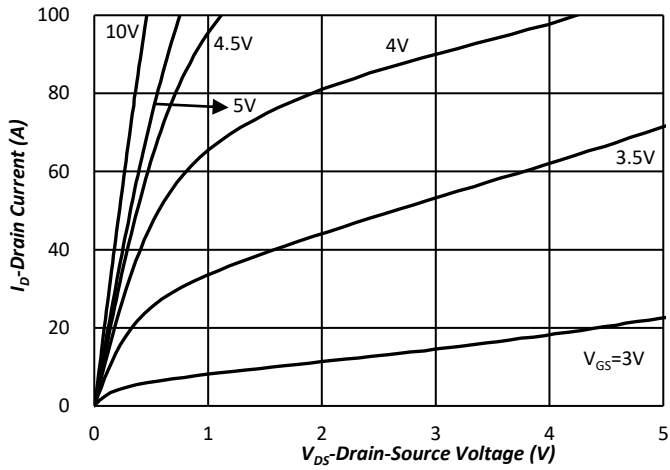


Fig.1 Typical Output Characteristics

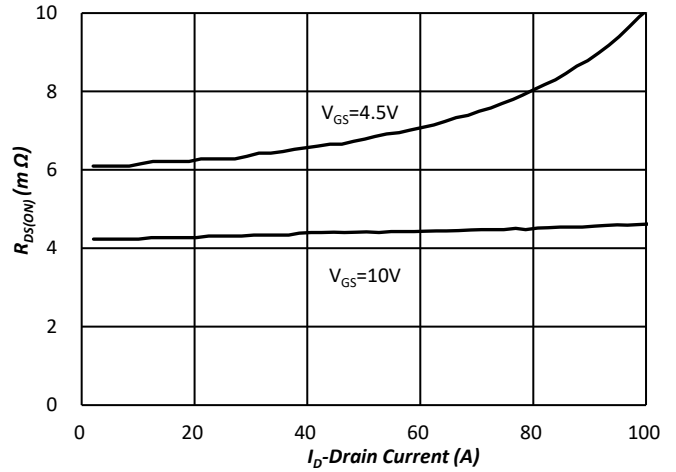


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

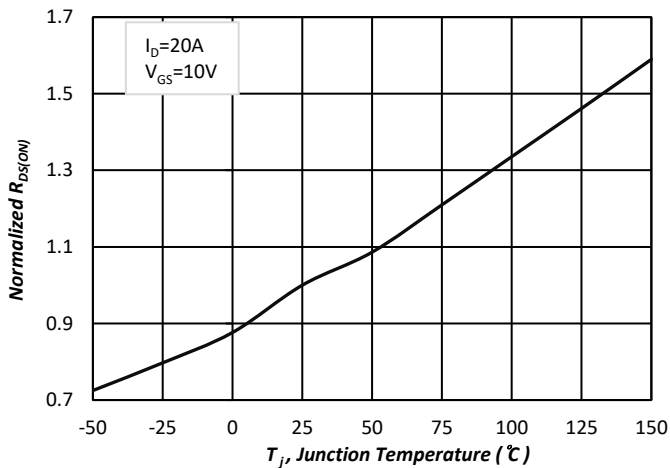


Fig.3 Normalized On-Resistance v.s. Junction Temperature

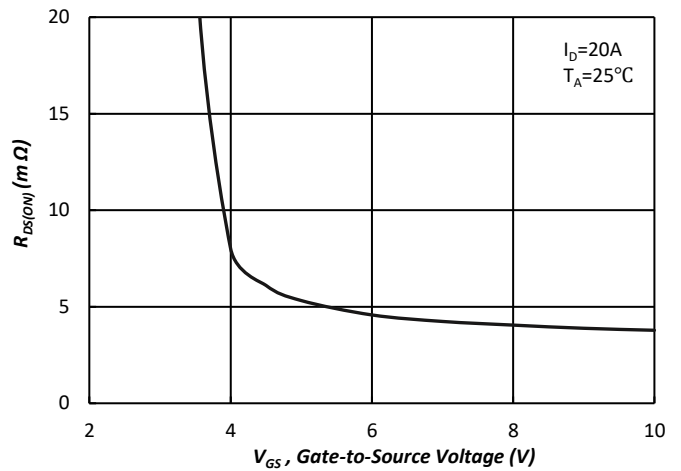


Fig.4 On-Resistance v.s. Gate Voltage

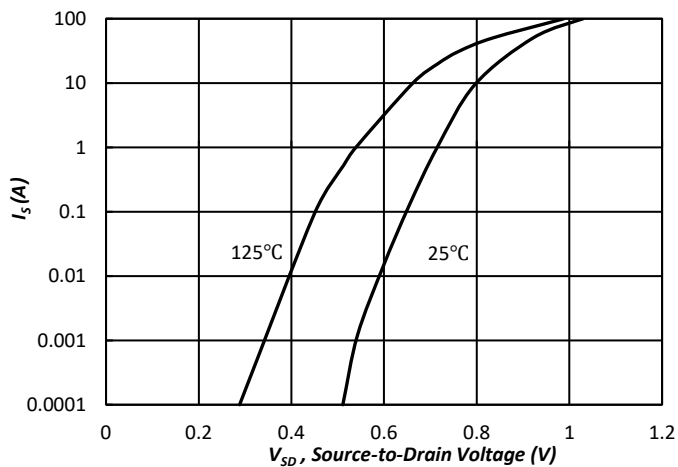


Fig.5 Forward Characteristic of Reverse Diode

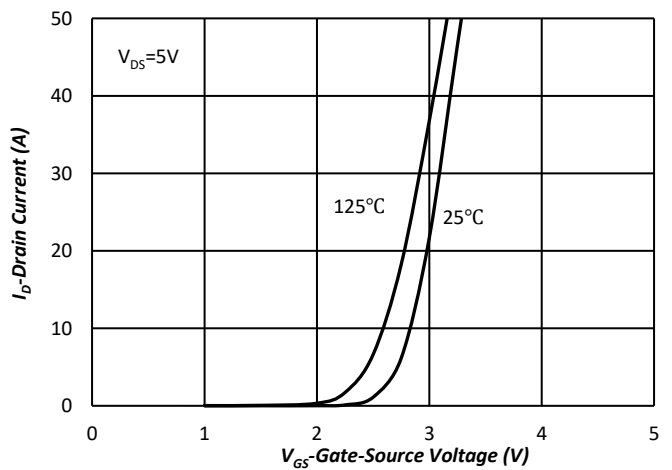


Fig.6 Transfer Characteristics

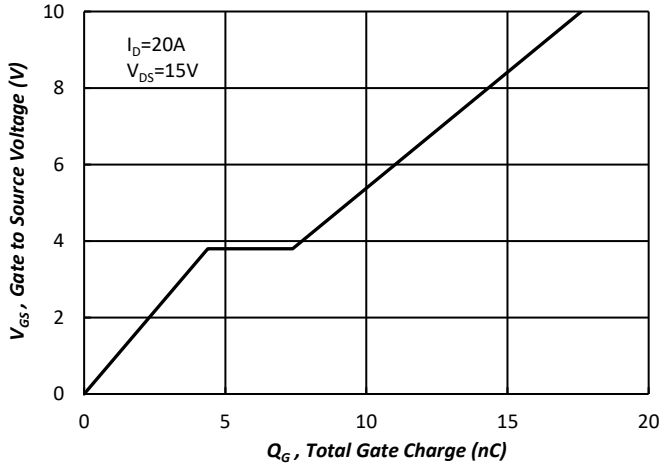


Fig.7 Gate Charge Characteristics

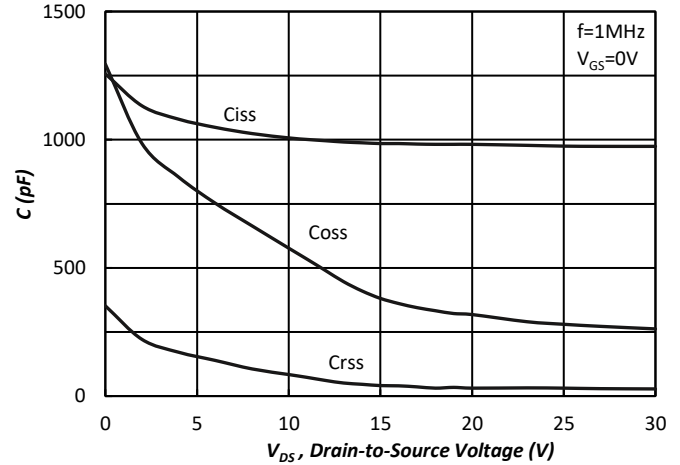


Fig.8 Typical Capacitance Characteristics

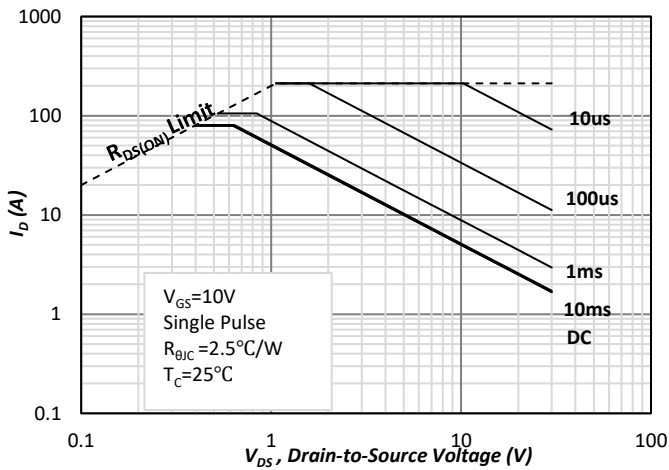


Fig.9. Maximum Safe Operating Area

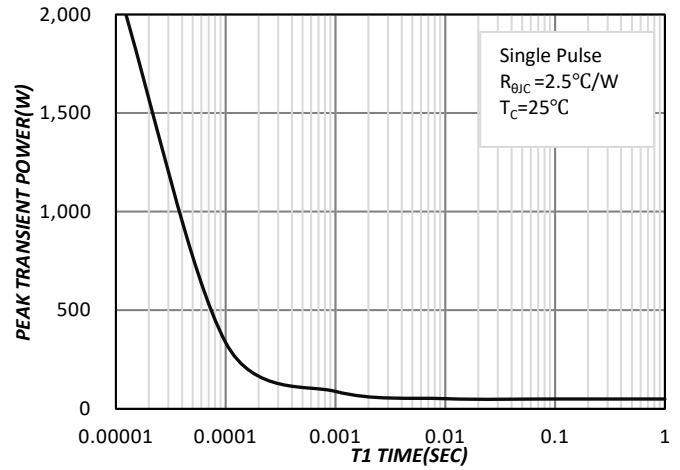


Fig.10. Single Pulse Maximum Power Dissipation

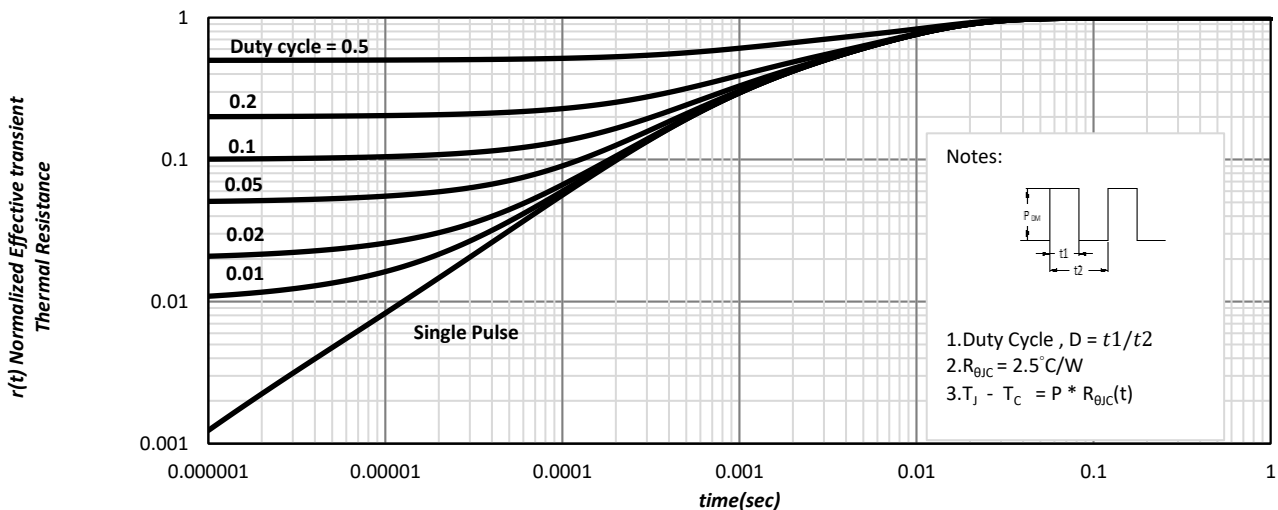


Fig.11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMB04N03VS for EDFN 3x3



B04N03S: Device Name

ABCDEFGH: Date Code

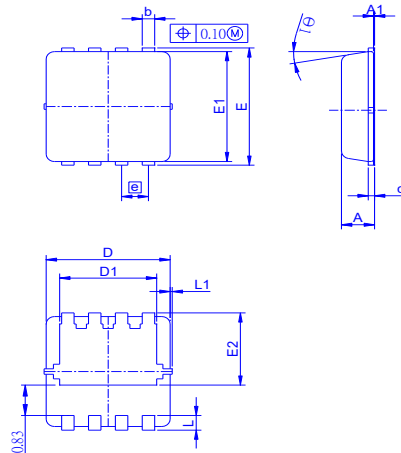
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

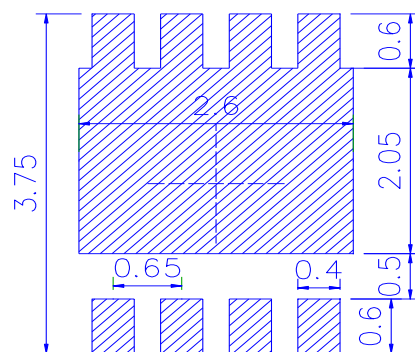
DEFG: Serial No.

Outline Drawing

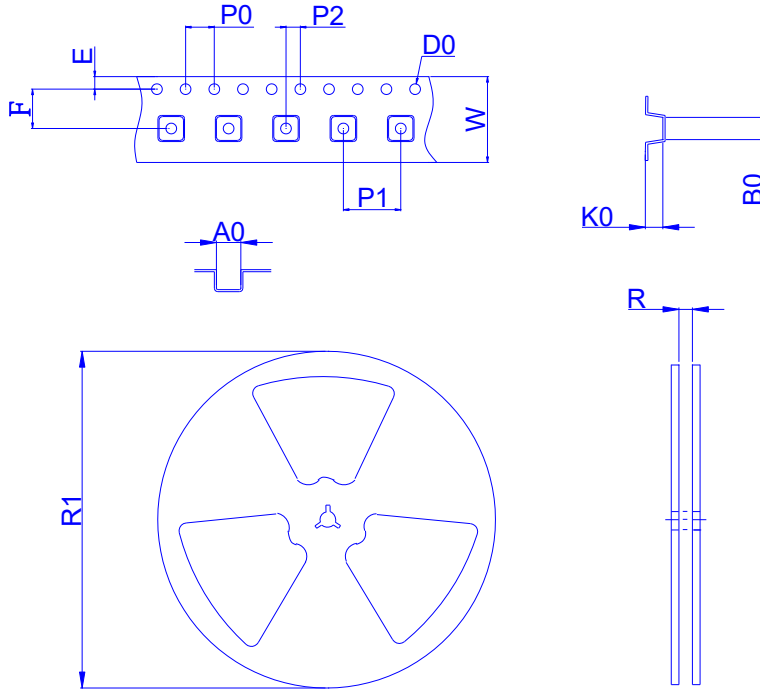


Dimension	A	A1	b	c	D	D1	E	E1	E2	e	L	L1	Θ1
Min.	0.65	0	0.2	0.1	2.9	2.15	3.1	2.9	1.53	0.55	0.25	-	0°
Typ.	0.75	-	0.3	0.15	3	2.45	3.2	3	1.97	0.65	0.4	0.075	10°
Max.	0.9	0.05	0.4	0.25	3.3	2.74	3.5	3.3	2.59	0.75	0.6	0.15	14°

Footprint



◆ Tape&Reel Information:5000pcs/Reel



Package	EDFN3X3
Reel	13"
Device orientation	<p>FEED DIRECTION</p> <p>→</p>

Dimension in mm

Dimension	Carrier tape										Reel	
	A0	B0	D0	E	F	K0	P0	P1	P2	W	R	R1
Typ.	3.60	3.60	1.55	1.70	5.50	1.10	4.00	8.00	2.00	12.0	12.4	330
±	0.30	0.30	0.20	0.20	0.05	0.10	0.10	0.10	0.10	0.30	2	2