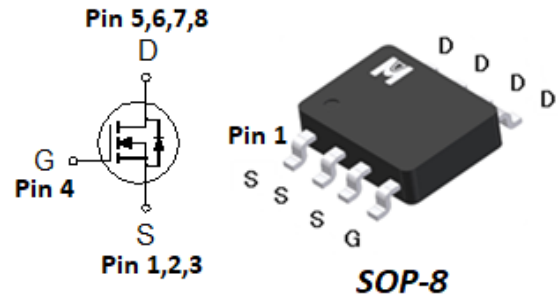


Single N-Channel Logic Level Enhancement Mode Field Effect Transistor

• Product Summary:

	N-CH
BVDSS	30 V
$R_{DS(on) (MAX.)}@V_{GS}=10V$	4.5 mΩ
$R_{DS(on) (MAX.)}@V_{GS}=4.5V$	6.0 mΩ
$I_D @T_A=25^{\circ}C$	23 A

• Pin Description:



Single N Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



• ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current ¹	T _A = 25 °C	I _D	23	
	T _A = 70 °C		14	
Pulsed Drain Current ¹		I _{DM}	92	
Avalanche Current ^{1,4}		I _{AS}	50	
Avalanche Energy ^{1,4}	L = 0.1mH	EAS	125	mJ
Repetitive Avalanche Energy ^{2,4}	L = 0.05mH	EAR	62.5	
Power Dissipation ¹	T _A = 25 °C	P _D	3.1	W
	T _A = 70 °C		1.3	
Operating Junction & Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C

• 100% UIS testing in condition of $V_D=30V$, $L=0.1mH$, $V_G=10V$, $I_L=30A$, Rated $V_{DS}=30V$ N-CH

• THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case		$R_{\theta JC}$		25	$^{\circ}C/W$
Junction-to-Ambient ³	$t \leq 10s$	$R_{\theta JA}$		40	
	Steady-State	$R_{\theta JA}$		75	

¹ Pulse width limited by maximum junction temperature.

² Duty cycle < 1%

³ $75^{\circ}C / W$ when mounted on a 1 in² pad of 2 oz copper.

⁴ Guarantee by Engineering test

▪ CH-1_ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250uA	30			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	1.2	1.7	2.5	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 30V, V _{GS} = 0V			1	uA
		V _{DS} = 30V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	23			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A		3.8	4.5	mΩ
		V _{GS} = 4.5V, I _D = 20A		4.8	6	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 20A		25		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		2298		pF
Output Capacitance ⁵	C _{oss}			314		
Reverse Transfer Capacitance ⁵	C _{rss}			169		
Gate Resistance ^{4,5}	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		1.9	3.8	Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 15V, V _{GS} = 10V, I _D = 20A		36.9		nC
	Q _g (V _{GS} =4.5V)			18.1		
Gate-Source Charge ^{1,2,5}	Q _{gs}			5.0		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			6.6		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 15V, V _{GS} = 10V, I _D = 1A , R _g = 6Ω		7.8		nS
Rise Time ^{1,2,5}	t _r			3.6		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			54.7		
Fall Time ^{1,2,5}	t _f			26.1		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				23	A
Pulsed Current ³	I _{SM}				92	
Forward Voltage ^{1,4}	V _{SD}	I _F = I _S , V _{GS} = 0V			1.2	V
Reverse Recovery Time ⁵	t _{rr}	I _F = I _S , dI _F /dt = 400A / uS		14.7		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			2.67		A
Reverse Recovery Charge ⁵	Q _{rr}			18.9		nC

¹ Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

² Independent of operating temperature.

³ Pulse width limited by maximum junction temperature.

⁴ Guarantee by FT test item

⁵ Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪TYPICAL CHARACTERISTICS

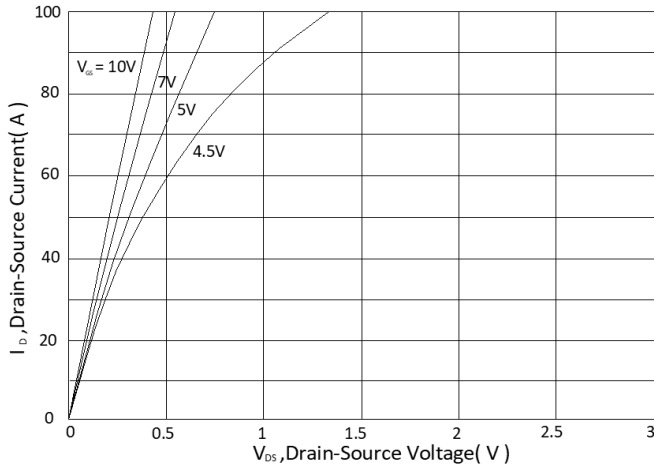


Fig.1 Typical Output Characteristics

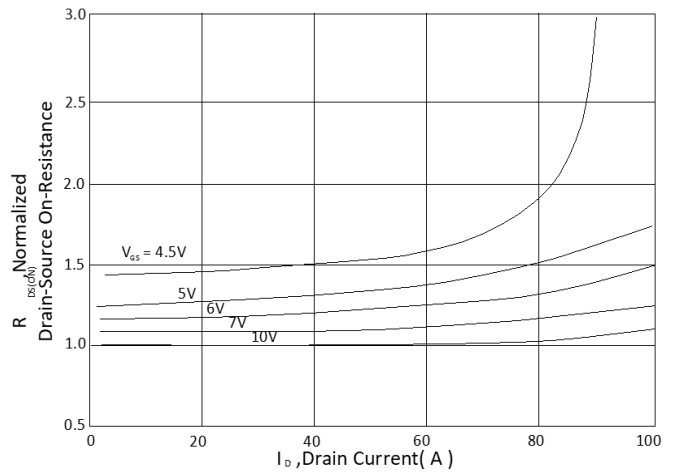


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

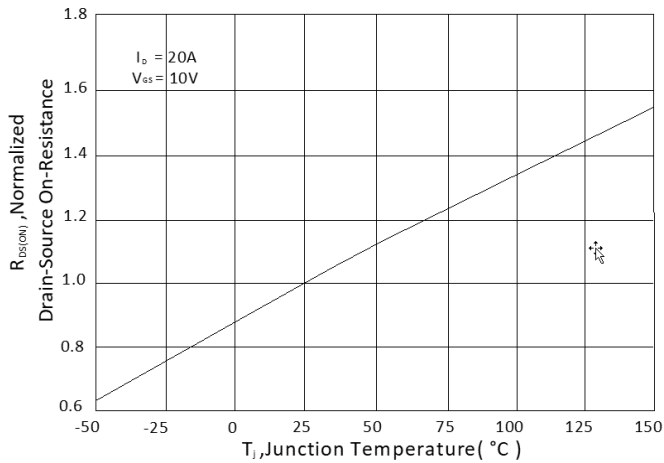


Fig.3 Normalized On-Resistance v.s. Junction Temperature

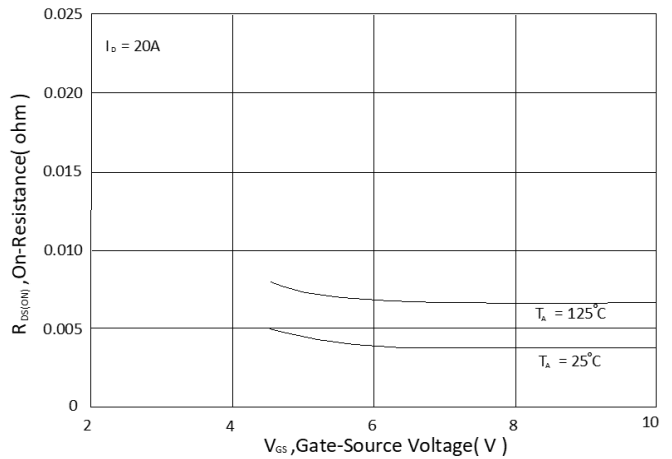


Fig.4 On-Resistance v.s. Gate Voltage

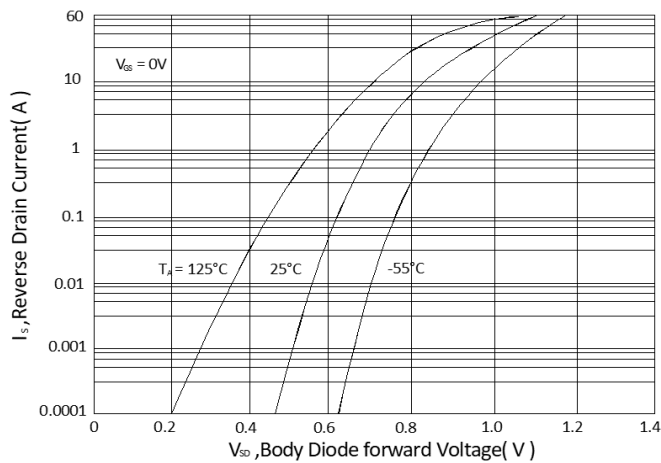


Fig.5 Forward Characteristic of Reverse Diode

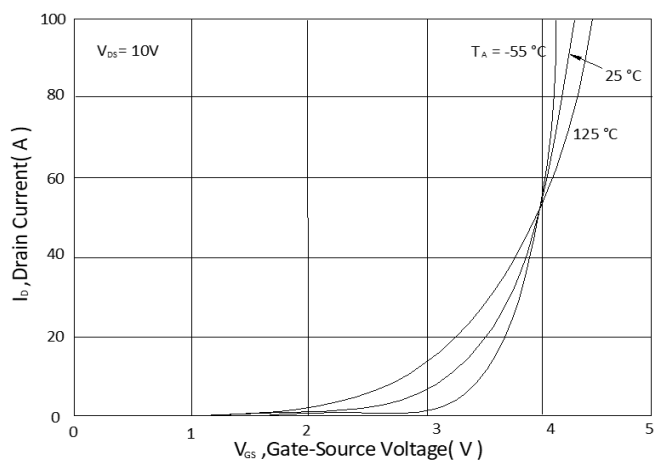


Fig.6 Transfer Characteristics

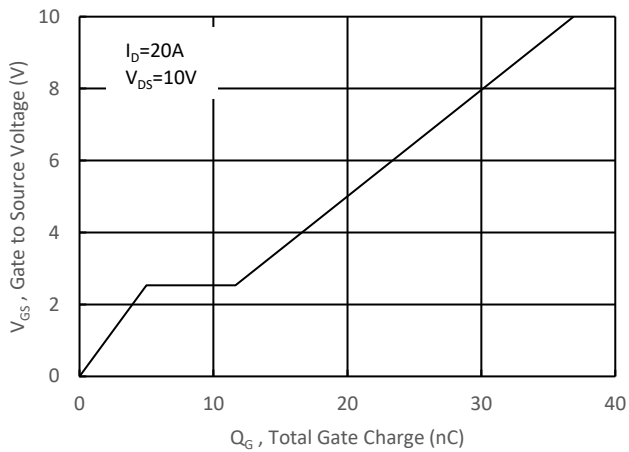


Fig.7 Gate Charge Characteristics

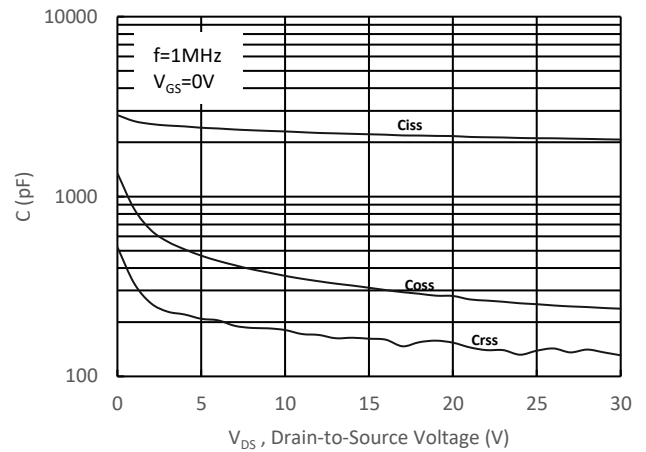


Fig.8 Typical Capacitance Characteristics

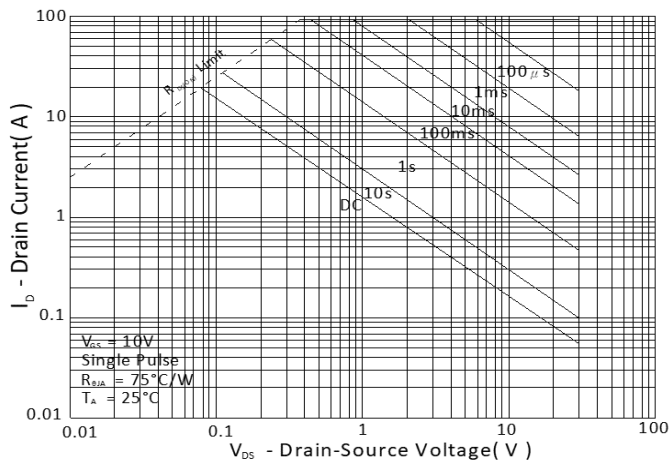


Fig 9. Maximum Safe Operating Area

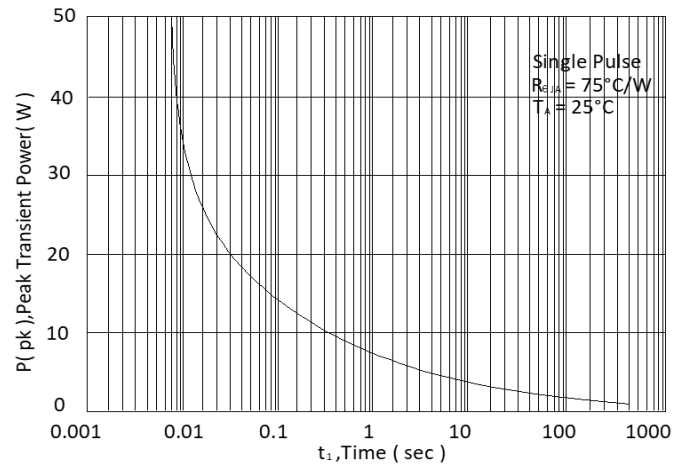


Fig 10. Single Pulse Maximum Power Dissipation

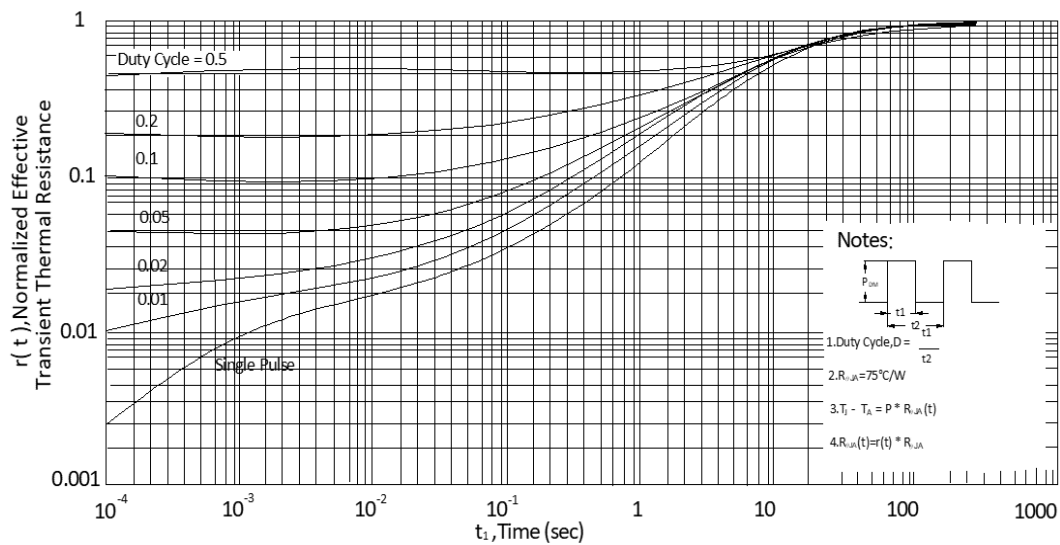
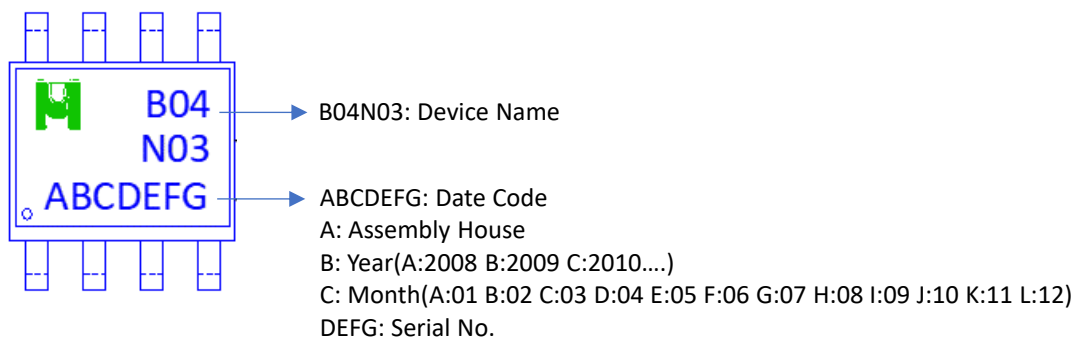


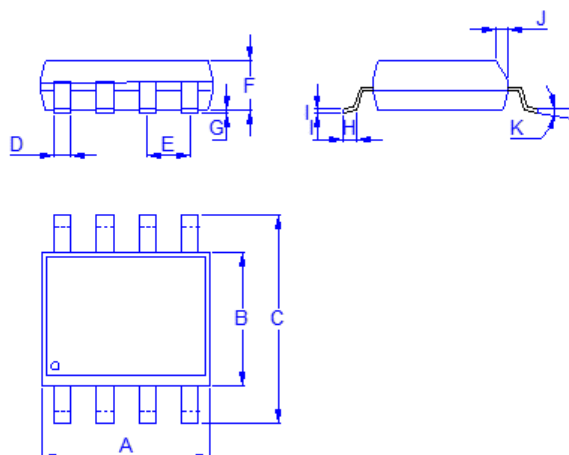
Fig 11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMB04N03G for SOP-8

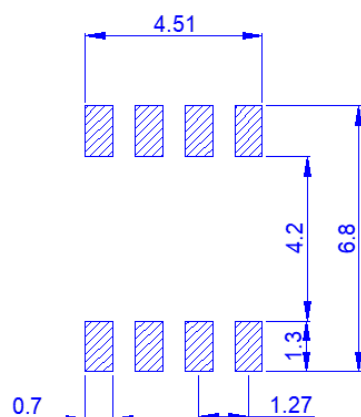


Outline Drawing

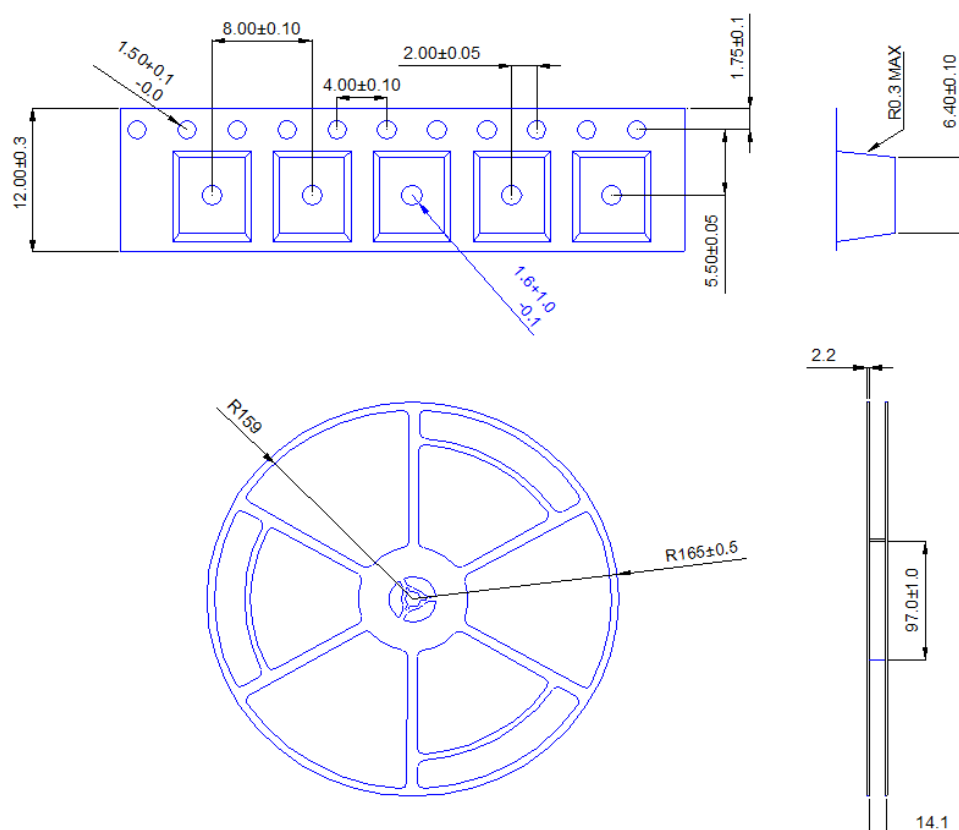


Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.7	3.8	5.8	0.31		1.35	0.01	0.4	0.1	0.25	0°
Typ.	4.9	3.9	6	0.41	1.27	1.55	0.18	0.6	0.2	0.3	
Max.	5.1	4	6.2	0.51		1.75	0.25	1.27	0.25	0.5	8°

Footprint



◆ Tape&Reel Information:2500pcs/Reel(Dimension in millimeter)



產品別	SOP-8
Reel尺寸	13"
編帶方式	FEED DIRECTION
前空格	25
後空格	50
裝箱數	
滿捲數量	2.5K
捲/內盒比	01:01
內盒滿箱數	2.5K
內/外箱比	10:01
外箱滿箱數	25K