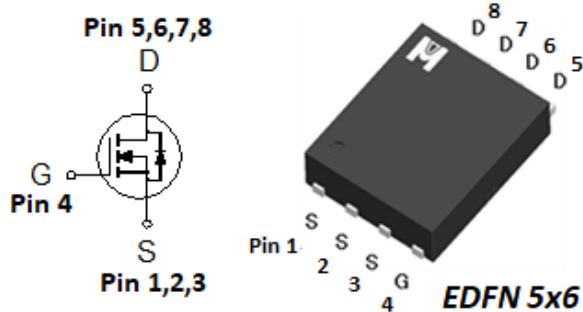


Single N-Channel Logic Level Enhancement Mode Field Effect Transistor

•Product Summary:

	N-CH
BVDSS	60V
$R_{DS(on) (MAX.)}@V_{GS}=10V$	3.0mΩ
$R_{DS(on) (MAX.)}@V_{GS}=4.5V$	4.5mΩ
$I_D @T_C=25^{\circ}C$	166A
$I_D @T_A=25^{\circ}C$	22A

• Pin Description:



Single N Channel MOSFET

UIS, Rg 100% Tested

RoHS & Halogen Free & TSCA Compliant



•ABSOLUTE MAXIMUM RATINGS ($T_C = 25^{\circ}C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^{\circ}C$	I_D	166	A
	$T_C = 100^{\circ}C$		104	
Continuous Drain Current	$T_A = 25^{\circ}C$	I_D	22	
	$T_A = 70^{\circ}C$		17	
Pulsed Drain Current ¹		I_{DM}	269	mJ
Avalanche Current		I_{AS}	65	
Avalanche Energy	$L = 0.1mH$	EAS	211.3	
Repetitive Avalanche Energy ²	$L = 0.05mH$	EAR	105.6	W
Power Dissipation	$T_C = 25^{\circ}C$	P_D	138.9	
	$T_C = 100^{\circ}C$		55.6	W
Power Dissipation	$T_A = 25^{\circ}C$	P_D	2.5	
	$T_A = 70^{\circ}C$		1.6	°C
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	

• 100% UIS testing in condition of $V_D=30V$, $L=0.1mH$, $V_G=10V$, $I_L=39A$, Rated $V_{DS}=60V$ N-CH

•THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		0.9	°C/W
Junction-to-Ambient ³	$R_{\theta JA}$		50	

¹Pulse width limited by maximum junction temperature.

²Duty cycle < 1%

³The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}C$.

⁴Guarantee by Engineering test

▪ ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250uA	60			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	1.2	1.6	2.5	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 48V, V _{GS} = 0V			1	uA
		V _{DS} =42V, V _{GS} =0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	166			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A		2.3	3	mΩ
		V _{GS} = 4.5V, I _D = 20A		3.1	4.5	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 20A		56		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 30V, f = 1MHz		4393		pF
Output Capacitance ⁵	C _{oss}			665		
Reverse Transfer Capacitance ⁵	C _{rss}			29		
Gate Resistance ^{4,5}	R _g	f = 1MHz		1.5		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 30V, V _{GS} = 10V, I _D = 20A		91.5		nC
	Q _g (V _{GS} =4.5V)			47.3		
Gate-Source Charge ^{1,2,5}	Q _{gs}			10.1		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			21.9		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 30V, V _{GS} = 10V, I _D = 5A , R _g = 6Ω		10.7		nS
Rise Time ^{1,2,5}	t _r			11.6		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			48.2		
Fall Time ^{1,2,5}	t _f			20.4		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				166	A
Pulsed Current ³	I _{SM}				269	
Forward Voltage ^{1,4}	V _{SD}	I _F = I _S , V _{GS} = 0V			1.2	V
▪ 100% UIS testing in condition of V _D =20V, L=0.1mH, V _G =10V, I _L =20A	t _{rr}	I _F =30A, di _F /dt = 400A / uS		31.2		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			3.77		A
Reverse Recovery Charge ⁵	Q _{rr}			68.6		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.



▪ TYPICAL CHARACTERISTICS

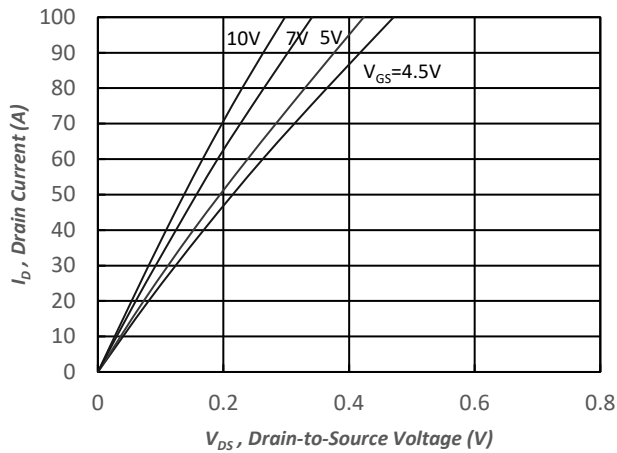


Fig.1 Typical Output Characteristics

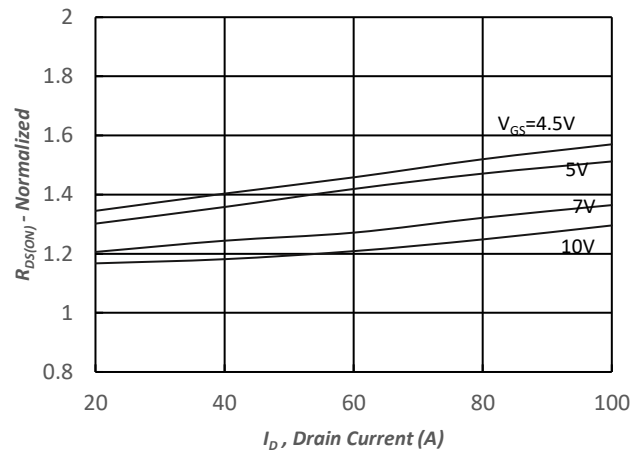


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

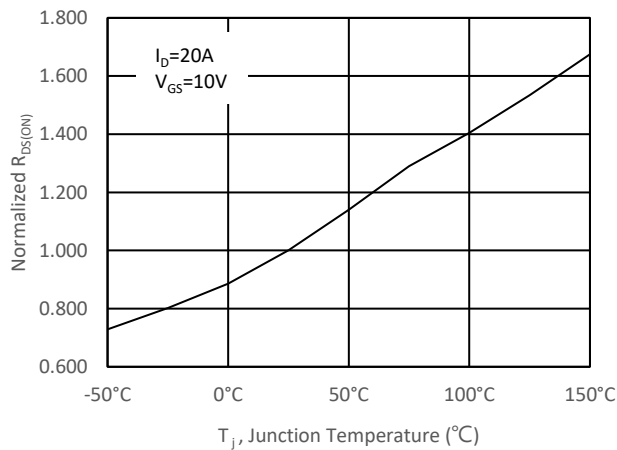


Fig.3 Normalized On-Resistance v.s. Junction Temperature

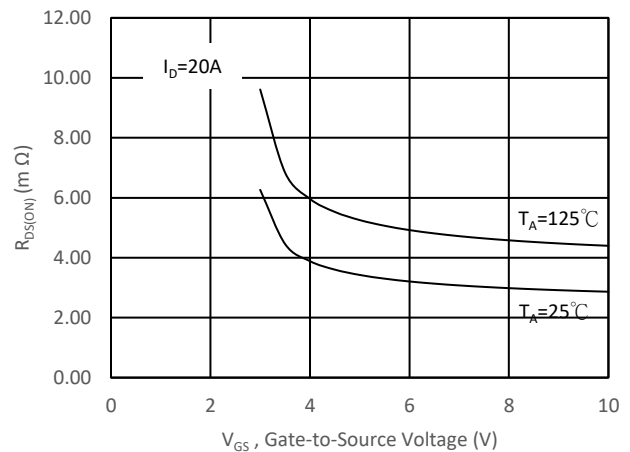


Fig.4 On-Resistance v.s. Gate Voltage

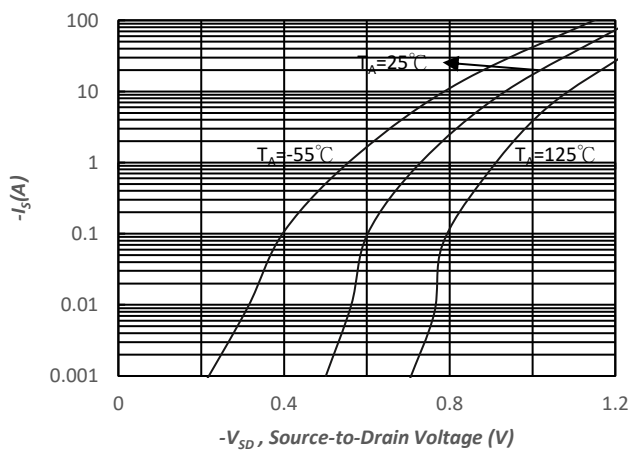


Fig.5 Forward Characteristic of Reverse Diode

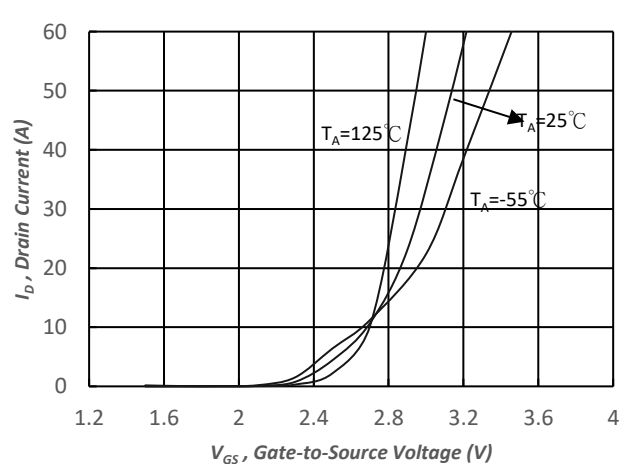


Fig.6 Transfer Characteristics

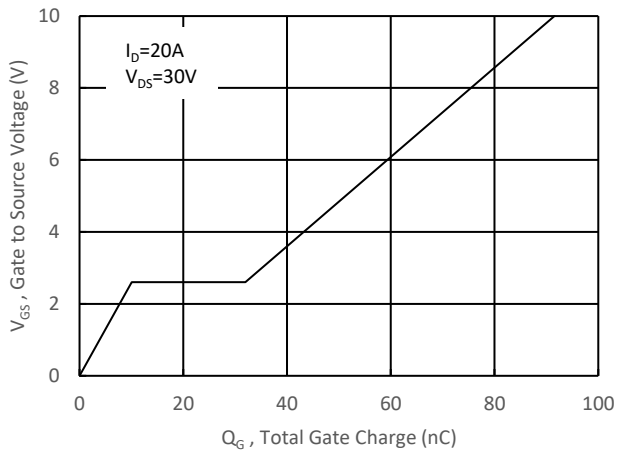


Fig.7 Gate Charge Characteristics

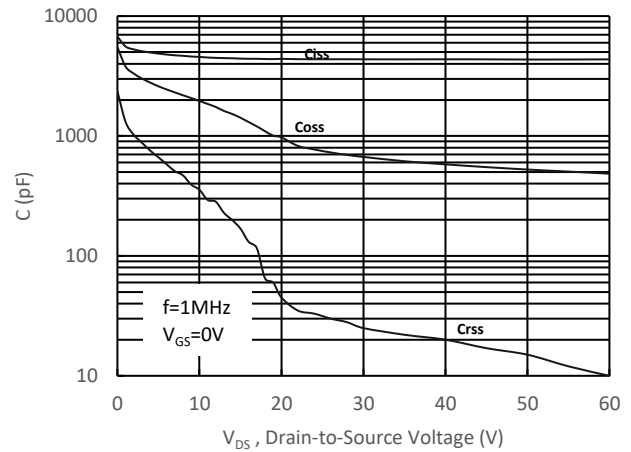


Fig.8 Typical Capacitance Characteristics

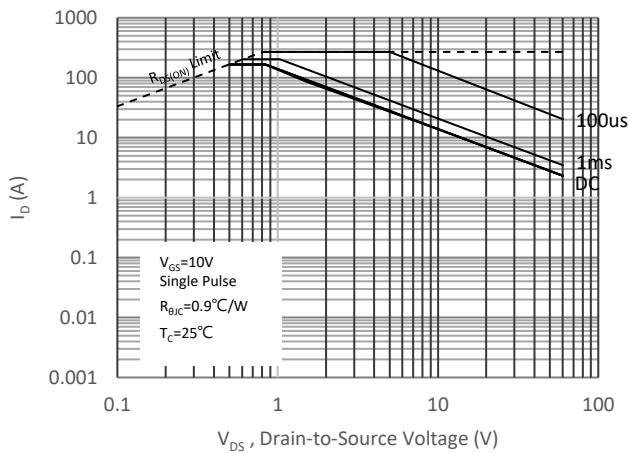


Fig.9. Maximum Safe Operating Area

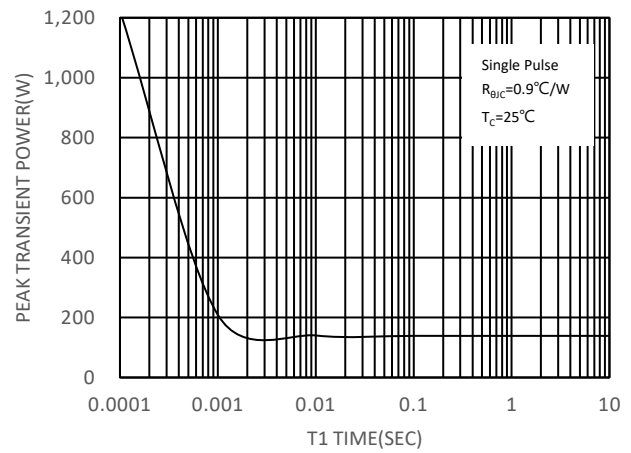


Fig.10. Single Pulse Maximum Power Dissipation

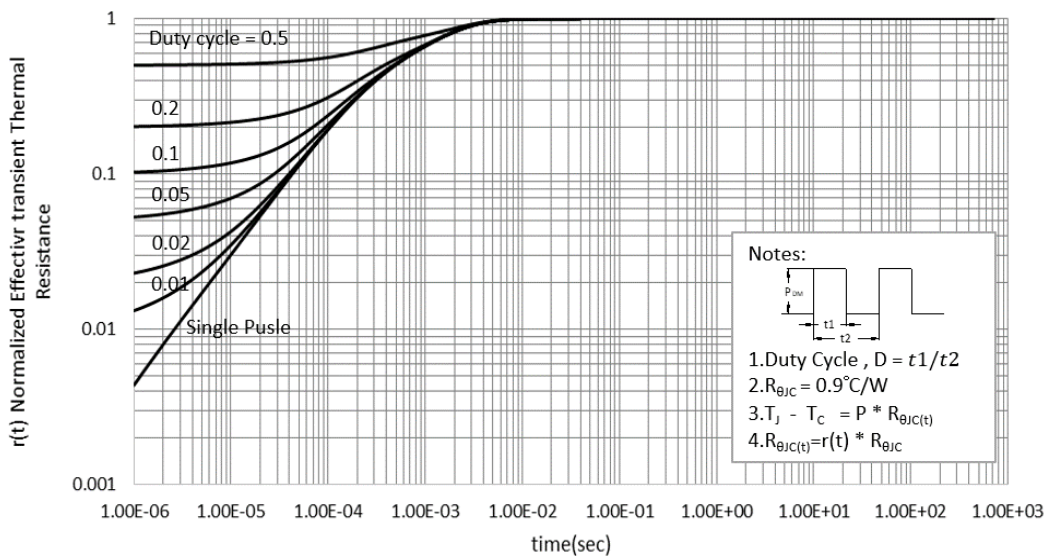


Fig.11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMB03N06HS for EDFN 5x6



B03N06S: Device Name

ABCDEFG: Date Code

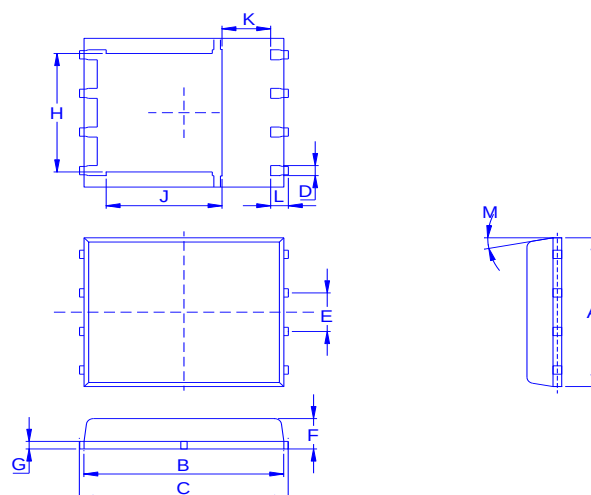
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

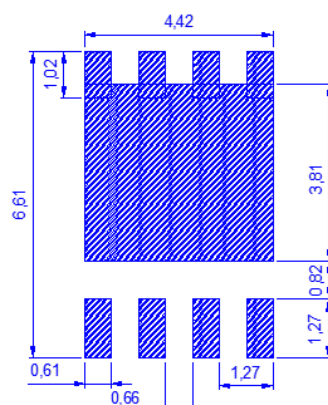
DEFG: Serial No.

Outline Drawing

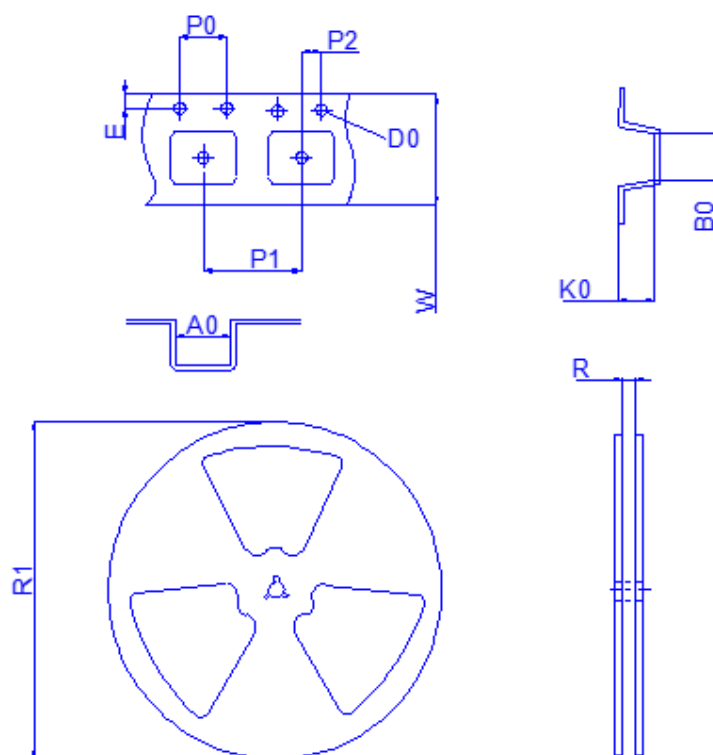


Dimension	A	B	C	D	E	F	G	H	J	K	L	M
Min	4.8	5.55	5.9	0.3	1.17	0.85	0.15	3.61	3.18	1	0.38	0°
Typ.	4.9	5.7	6	0.4	1.27	0.95	0.2	3.87	3.44	1.2	0.4	
Max	5.4	5.85	6.15	0.51	1.37	1.17	0.34	4.31	3.78	1.39	0.71	12°

Footprint



◆ Tape&Reel Information:2500pcs/Reel
(Dimension in millimeter)



Package	EDFN5X6
Reel	13"
Device orientation	FEED DIRECTION

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	6.4	5.3	1.5	1.8	1.6	4	8	2	12	12.4	330
±	0.2	0.2	0.1	0.1	0.6	0.1	0.1	0.1	0.3	2	2