杰力科技股份有限公司
Excelliance MOS Corporation

EMB03N03HCS

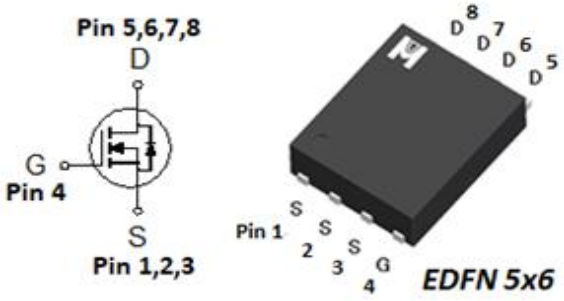
Single N-Channel Logic Level Enhancement Mode Field Effect Transistor

▪Product Summary:

	N-CH
BV_{DSS}	30V
$R_{DSON(MAX)}V_{GS}$=10V	3.0mΩ
$R_{DSON(MAX)}V_{GS}$=4.5V	4.0mΩ
I_D @T_C=25°C	116A
I_D @T_A=25°C	38A

Single N Channel MOSFET
UIS, Rg 100% Tested
RoHS & Halogen Free & TSCA Compliant

▪ Pin Description:



▪ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_C = 25 °C	I_D	116	A
	T_C = 100 °C		73	
Continuous Drain Current	T_A = 25 °C	I_D	38	
	T_A = 70 °C		30	
Pulsed Drain Current[1]		I_{DM}	234	
Avalanche Current		I_{AS}	105	
Avalanche Energy	L = 0.01mH	EAS	55	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	EAR	28	
Power Dissipation	T_C = 25 °C	P_D	63	W
	T_C = 100 °C		25	
Power Dissipation	T_A = 25 °C	P_D	6.8	W
	T_A = 70 °C		4	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

▪ 100% UIS testing in condition of VD=25V, L=0.01mH, VG=10V, IL= 60A,RG=25Ω,Rated VDS=30V N-CH

▪THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case		$R_{\theta JC}$		2.0	°C/W
Junction-to-Ambient[3,4]	t≦10s	$R_{\theta JA}$		18	
	Steady-State	$R_{\theta JA}$		52	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle < 1%

[3]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C.

[4]Guarantee by Engineering test

▪ ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage[4]	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250uA	30			V
Gate Threshold Voltage[4]	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.2	1.6	2.2	
Gate-Body Leakage[4]	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current[4]	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V			1	μA
		V_{DS} =30V, V_{GS} =0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	116			A
Drain-Source On-State Resistance[1,4]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 20A		2.5	3	mΩ
Drain-Source On-State Resistance[1,4]	$R_{DS(ON)}$	V_{GS} = 4.5V, I_D = 20A		3.3	4	mΩ
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 20A		122		S
DYNAMIC						
Input Capacitance[5]	C_{iss}	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		1608		pF
Output Capacitance[5]	C_{oss}			639		
Reverse Transfer Capacitance[5]	C_{rss}			45		
Gate Resistance[4,5]	R_g	f = 1MHz		1.3		Ω
Total Gate Charge[1,2,5]	Q_g(V_{GS}=10V)	V_{DS} = 15V, V_{GS} = 10V, I_D = 20A		28		nC
Total Gate Charge[1,2,5]	Q_g(V_{GS}=4.5V)			12		
Gate-Source Charge[1,2,5]	Q_{gs}			6		
Gate-Drain Charge[1,2,5]	Q_{gd}			3		
Turn-On Delay Time[1,2,5]	$t_{d(on)}$	V_{DS} = 15V, V_{GS} = 10V, I_D = 5A , Rg = 3Ω		7		nS
Rise Time[1,2,5]	t_r			7.4		
Turn-Off Delay Time[1,2,5]	$t_{d(off)}$			22		
Fall Time[1,2,5]	t_f			5.8		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				52	A
Pulsed Current[3]	I_{SM}				234	
Forward Voltage[1,4]	V_{SD}	I_F = 20A, V_{GS} = 0V			1.2	V
Reverse Recovery Time[5]	t_{rr}	I_F = 20A, dI_F/dt = 400A / μS		17		nS
Peak Reverse Recovery Current[5]	$I_{RM(REC)}$			3		A
Reverse Recovery Charge[5]	Q_{rr}			25		nC

[1]Pulse test : Pulse Width ≦ 300 usec, Duty Cycle ≦ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

[4]Guarantee by FT test Item

[5]Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪ N-CH_TYPICAL CHARACTERISTICS

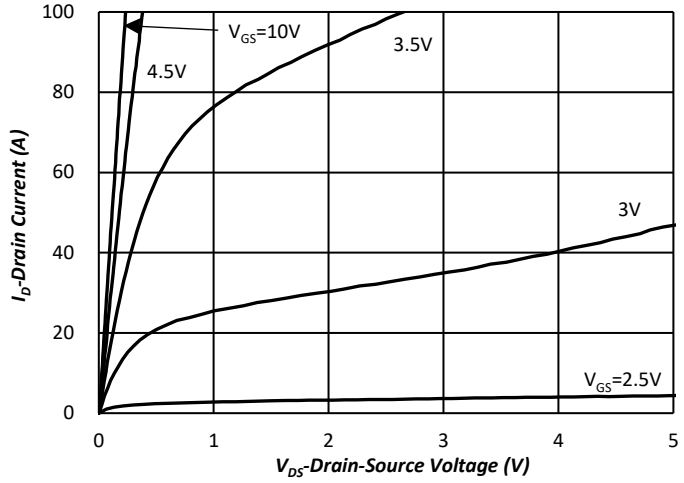


Fig.1 Typical Output Characteristics

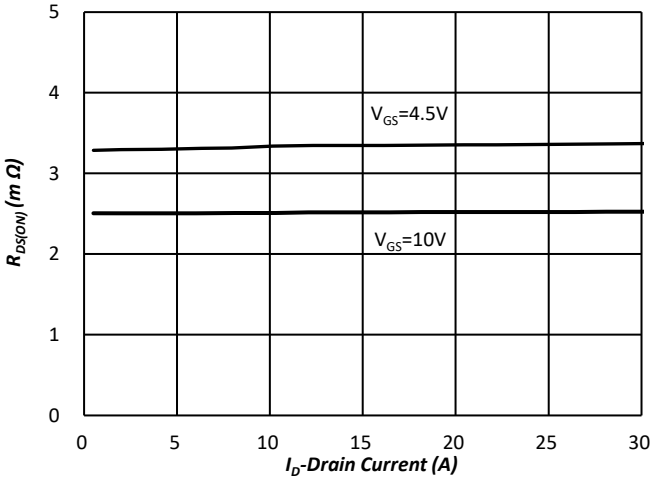


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

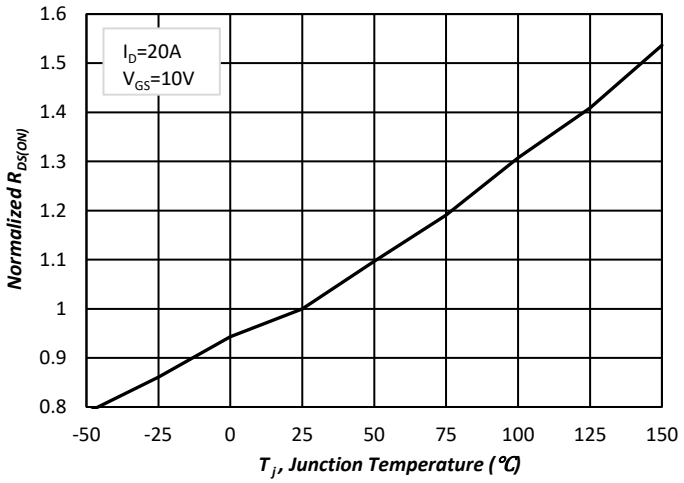


Fig.3 Normalized On-Resistance v.s. Junction Temperature

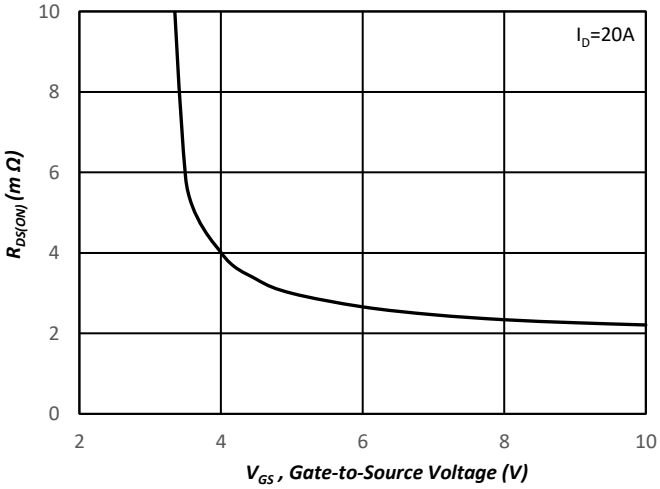


Fig.4 On-Resistance v.s. Gate Voltage

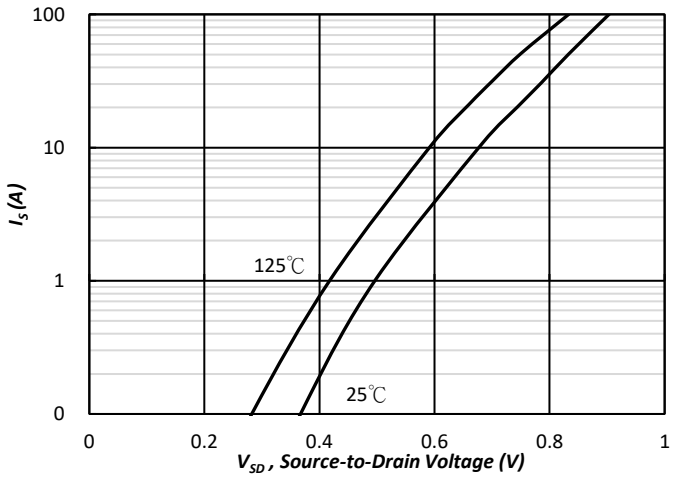


Fig.5 Forward Characteristic of Reverse Diode

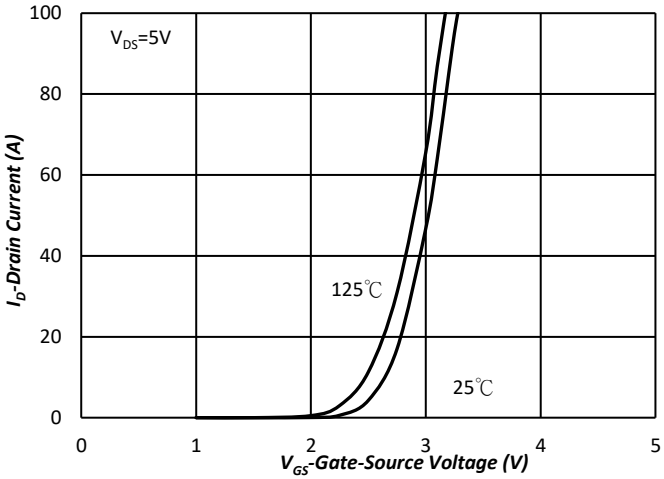


Fig.6 Transfer Characteristics

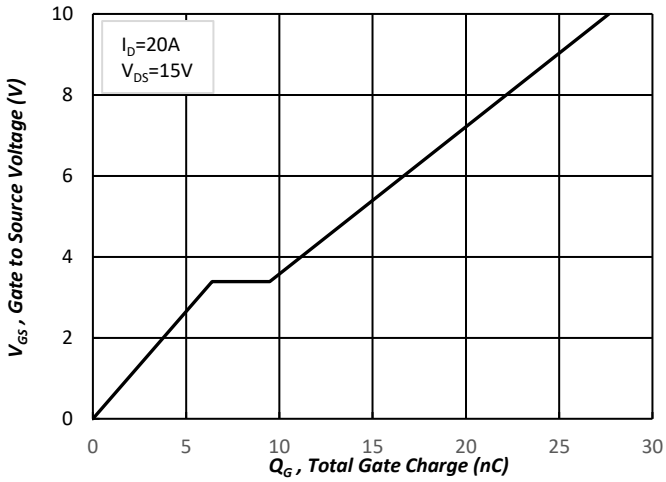


Fig.7 Gate Charge Characteristics

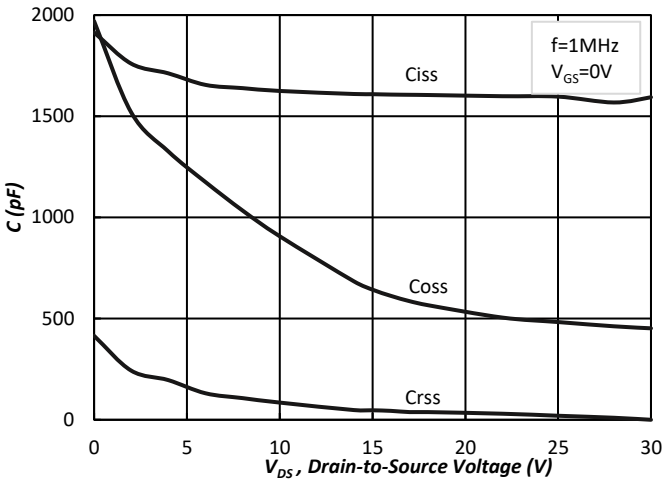


Fig.8 Typical Capacitance Characteristics

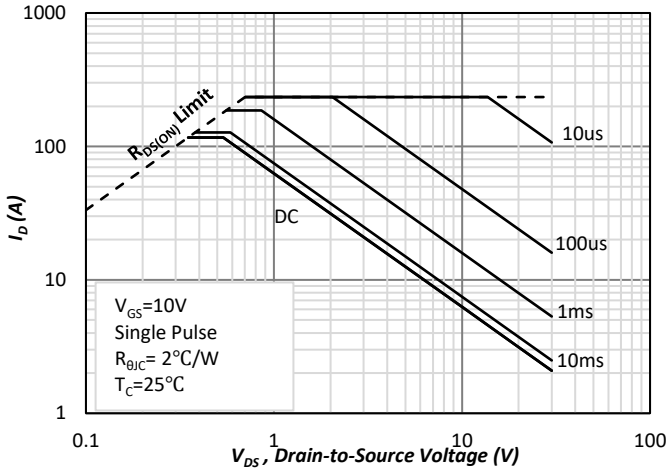


Fig 9. Maximum Safe Operating Area

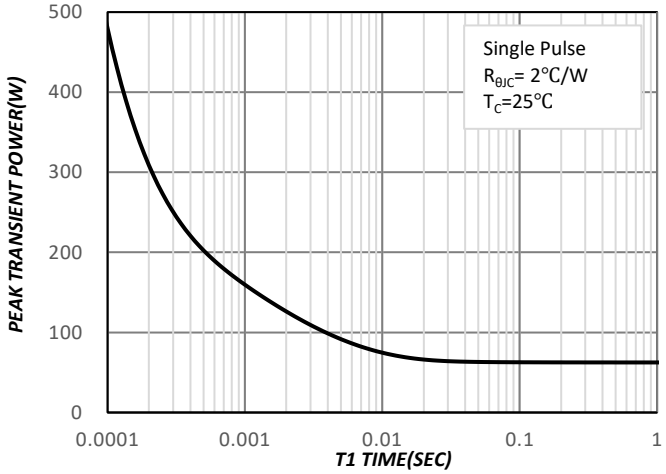


Fig 10. Single Pulse Maximum Power Dissipation

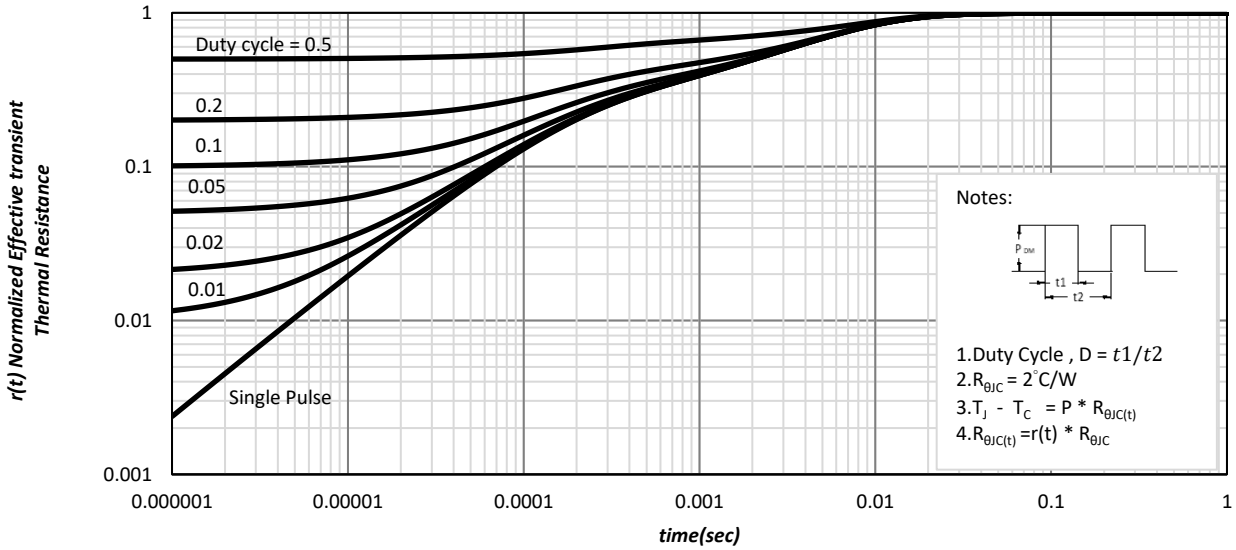
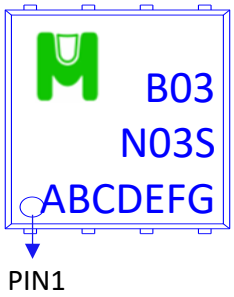


Fig 11. Effective Transient Thermal Impedance

Ordering & Marking Information:

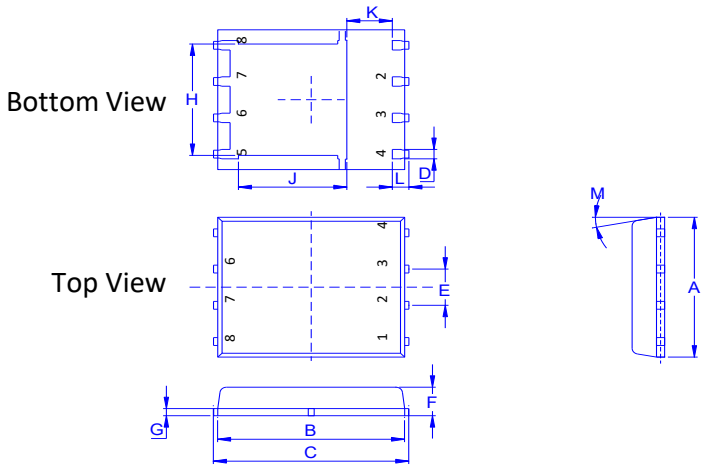
Device Name: EMB03N03HCS for EDFN 5x6



B03N03S: Device Name

ABCDEFG: Date Code
A: Assembly House
B: Year(A:2008 B:2009 C:2010….)
C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)
DEFG: Serial No.

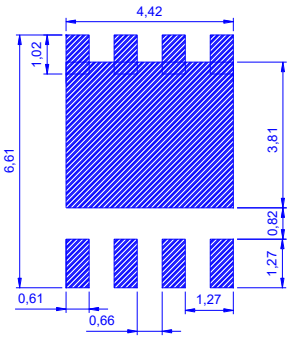
Outline Drawing



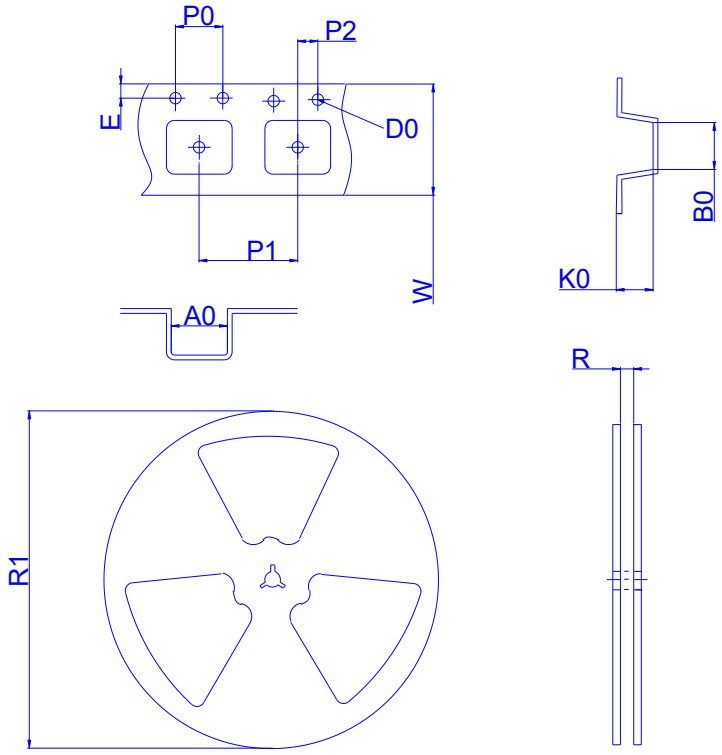
Dimension in mm

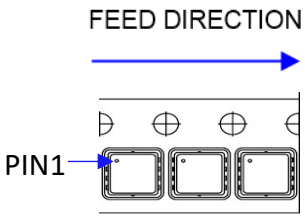
Dimension	A	B	C	D	E	F	G	H	J	K	L	M
Min	4.80	5.70	5.90	0.33	1.17	0.90	0.20	3.67	3.38	1.10	0.51	0°
Typ.	4.90	5.75	6.00	0.40	1.27	0.95	0.25	3.87	3.48	-	0.61	-
Max	5.00	5.80	6.10	0.51	1.37	1.10	0.34	4.02	3.78	-	0.71	12°

Footprint



◆ Tape&Reel Information:2500pcs/Reel



Package	EDFN5X6-A
Reel	13”
Device orientation	

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	6.4	5.3	1.5	1.8	1.3	4	8	2	12	12.4	330
±	0.2	0.2	0.1	0.1	0.2	0.1	0.1	0.1	0.3	2	2