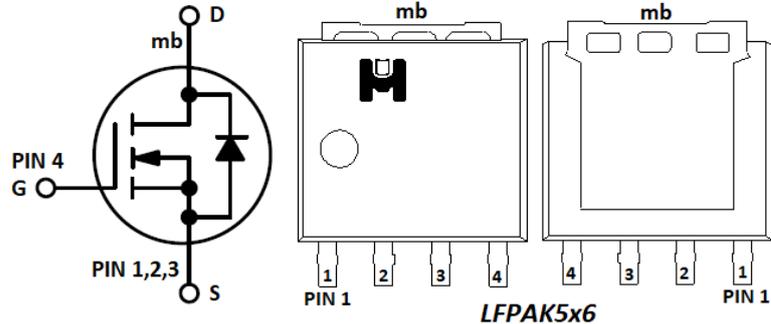


Single N-Channel Logic Level Enhancement Mode Field Effect Transistor

▪Product Summary:

	N-CH
BV_{DSS}	30V
$R_{DSON (MAX.)}@V_{GS}=10V$	0.99m Ω
$I_D @T_C=25^\circ C$	519A
$I_D @T_A=25^\circ C$	37A

▪ Pin Description:



Single N Channel MOSFET

UIS, Rg 100% Tested

RoHS & Halogen Free & TSCA Compliant



▪ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNIT	
Gate-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current ¹	I_D	$T_C = 25^\circ C$	519	
		$T_C = 100^\circ C$	328	
Continuous Drain Current ¹	I_D	$T_A = 25^\circ C$	37	
		$T_A = 70^\circ C$	29	
Pulsed Drain Current ¹	I_{DM}	783	A	
Avalanche Current ^{1,4}	I_{AS}	133		
Avalanche Energy ^{1,4}	E_{AS}	884		mJ
Repetitive Avalanche Energy ^{2,4}	E_{AR}	442		
Power Dissipation ¹	P_D	$T_C = 25^\circ C$	481	
		$T_C = 100^\circ C$	192	
Power Dissipation ¹	P_D	$T_A = 25^\circ C$	2.5	
		$T_A = 70^\circ C$	1.6	
Operating Junction & Storage Temperature Range	T_{jv}, T_{stg}	-55 to 150	$^\circ C$	

▪ 100% UIS testing in condition of $V_D=25V, L=0.1mH, V_G=10V, I_L=80A, R_G=25\Omega, \text{Rated } V_{DS}=30V \text{ N-CH}$

▪THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		0.26	$^\circ C/W$
Junction-to-Ambient ³	$t \leq 10s$	$R_{\theta JA}$	17	
	Steady-State	$R_{\theta JA}$	50	

¹Pulse width limited by maximum junction temperature.

²Duty cycle < 1%

³The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ C$.

⁴Guarantee by Engineering test

▪ ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	30			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.2	2.0	2.5	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 30V, V _{GS} = 0V			1	μA
		V _{DS} = 30V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	519			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 25A		0.75	0.99	mΩ
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 25A		50		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		7350		pF
Output Capacitance ⁵	C _{oss}			1150		
Reverse Transfer Capacitance ⁵	C _{rss}			435		
Gate Resistance ^{4,5}	R _g	f = 1MHz		1.0		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 15V, V _{GS} = 10V, I _D = 25A		125		nC
	Q _g (V _{GS} =4.5V)			57		
Gate-Source Charge ^{1,2,5}	Q _{gs}			31		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			22		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}		V _{DS} = 15V, V _{GS} = 10V, I _D = 5A, R _g = 3Ω		16	
Rise Time ^{1,2,5}	t _r			18		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			70		
Fall Time ^{1,2,5}	t _f			38		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				401	A
Pulsed Current ³	I _{SM}				783	
Forward Voltage ^{1,4}	V _{SD}	I _F = 25A, V _{GS} = 0V			1.2	V
Reverse Recovery Time ⁵	t _{rr}	I _F = 25A, di _F /dt = 100A / μS		29		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			1.3		A
Reverse Recovery Charge ⁵	Q _{rr}			22		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.



•TYPICAL CHARACTERISTICS

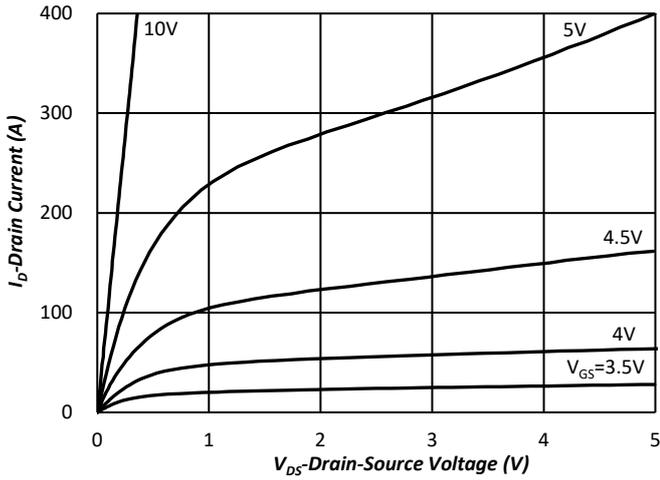


Fig.1 Typical Output Characteristics

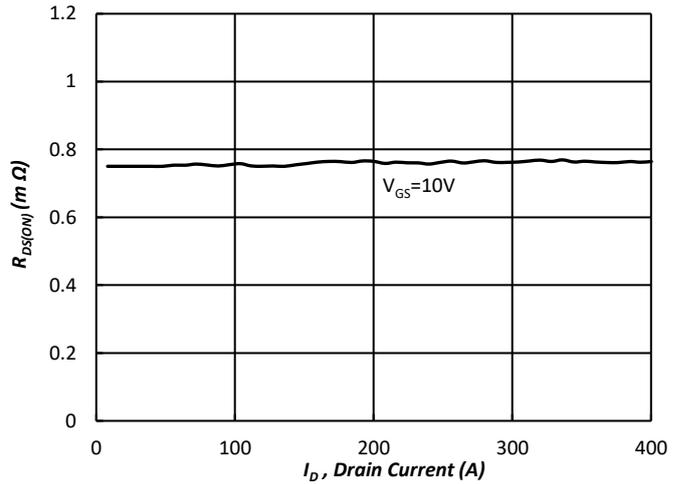


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

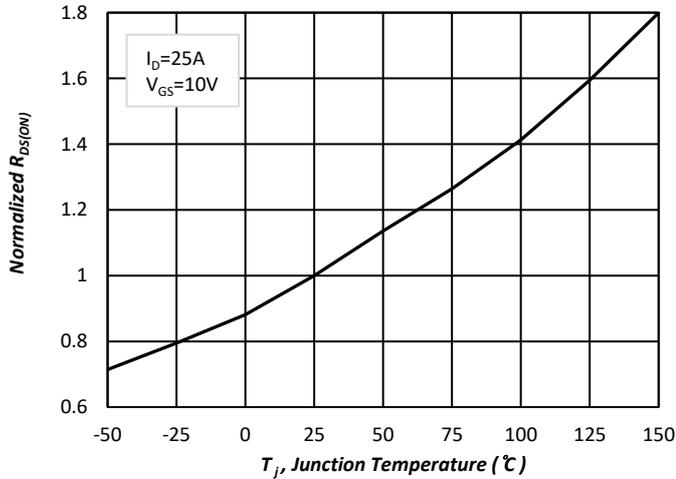


Fig.3 Normalized On-Resistance v.s. Junction Temperature

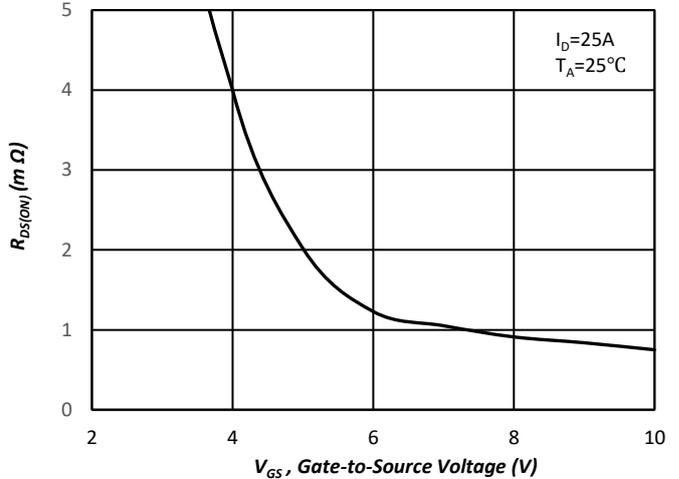


Fig.4 On-Resistance v.s. Gate Voltage

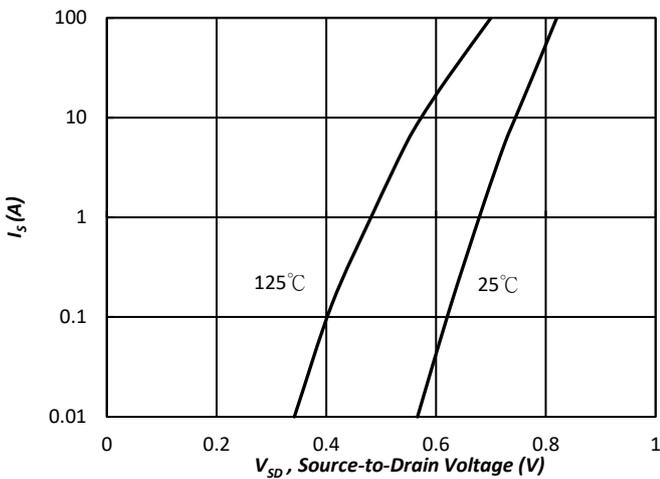


Fig.5 Forward Characteristic of Reverse Diode

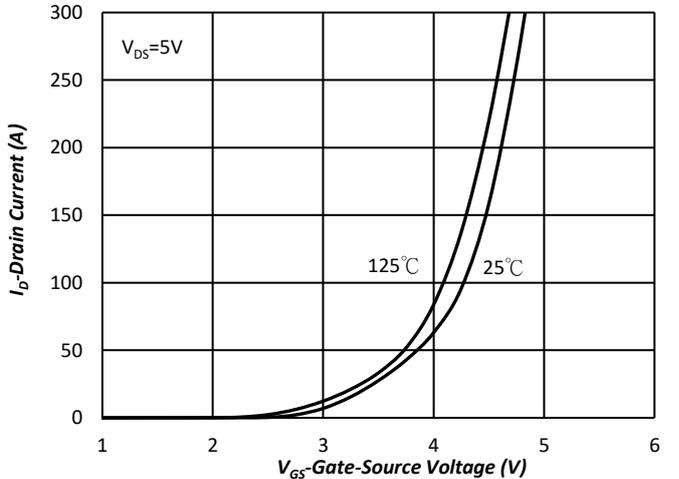


Fig.6 Transfer Characteristics

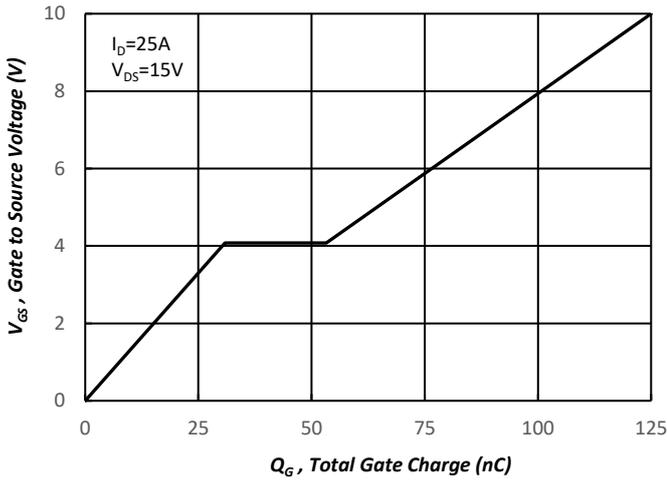


Fig.7 Gate Charge Characteristics

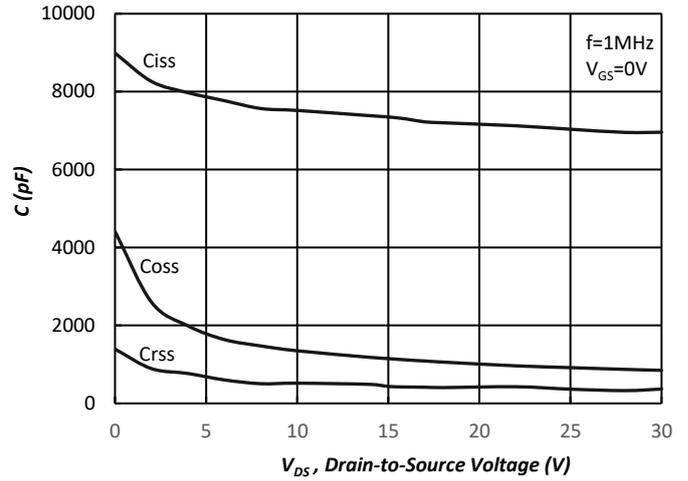


Fig.8 Typical Capacitance Characteristics

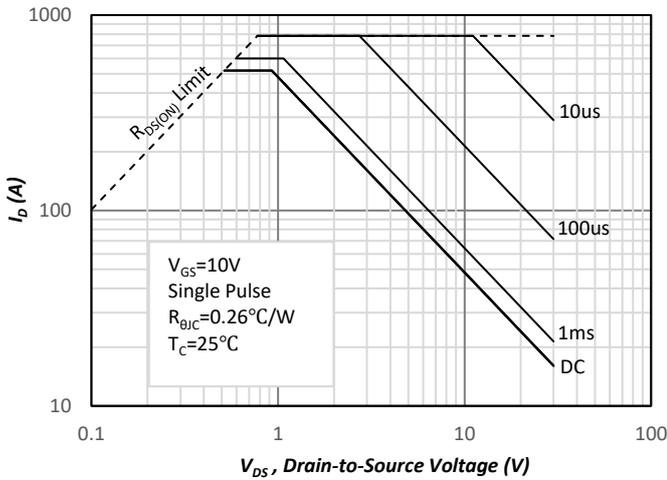


Fig.9. Maximum Safe Operating Area

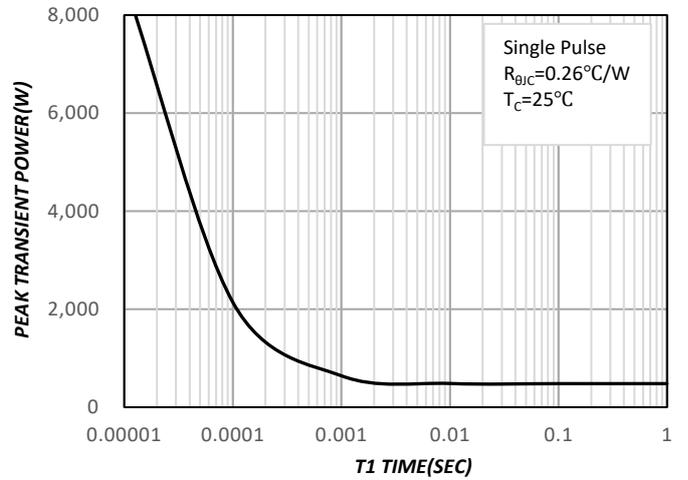


Fig.10. Single Pulse Maximum Power Dissipation

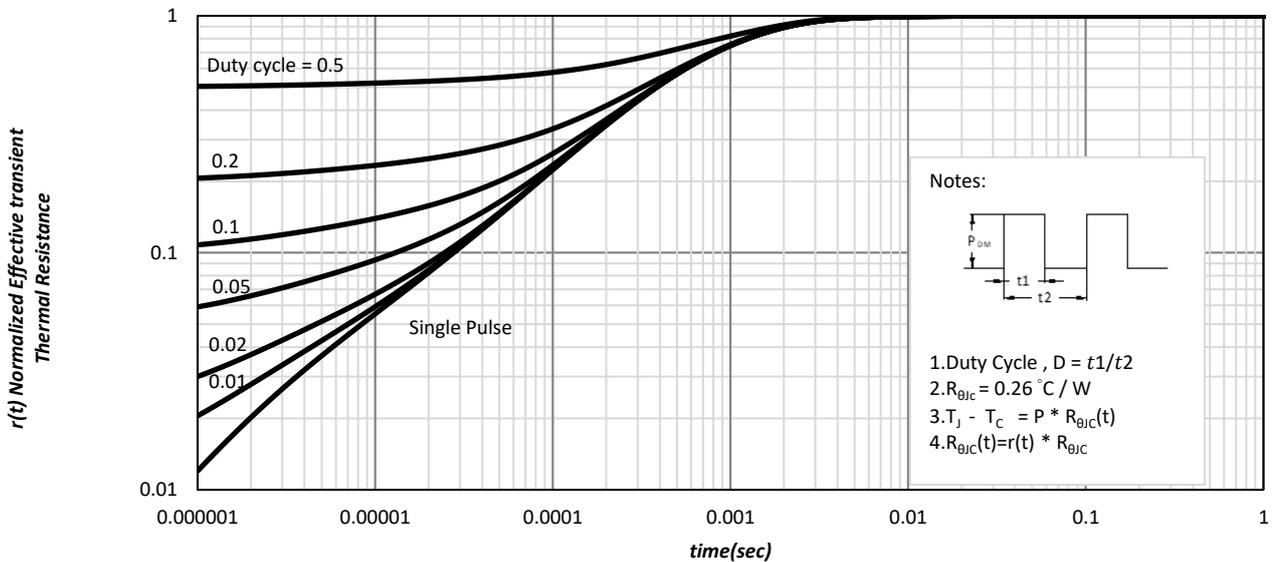
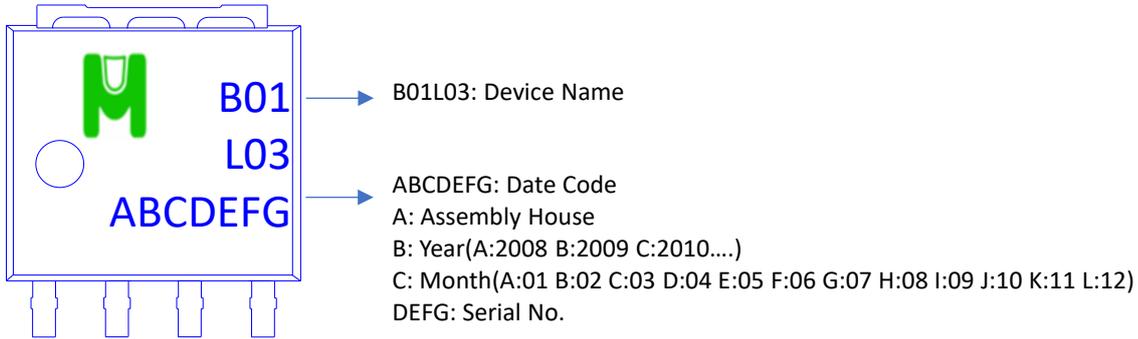


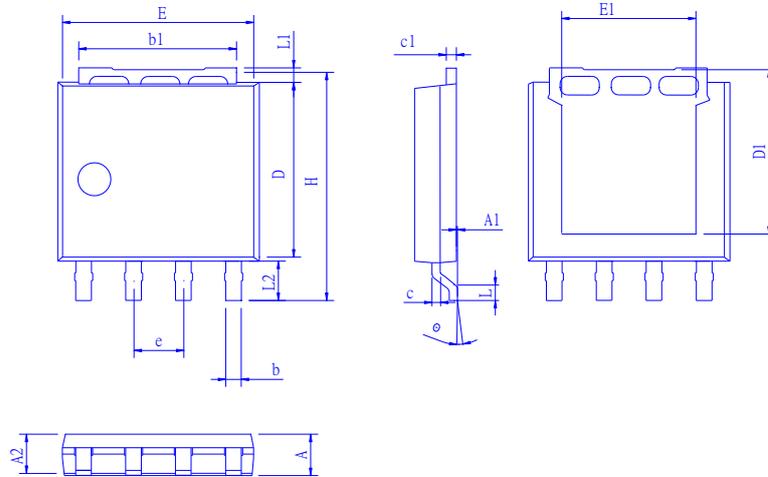
Fig.11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name:EMB01L03RHC for LFPAK5X6

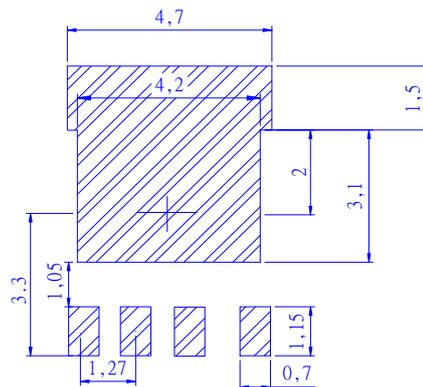


Outline Drawing

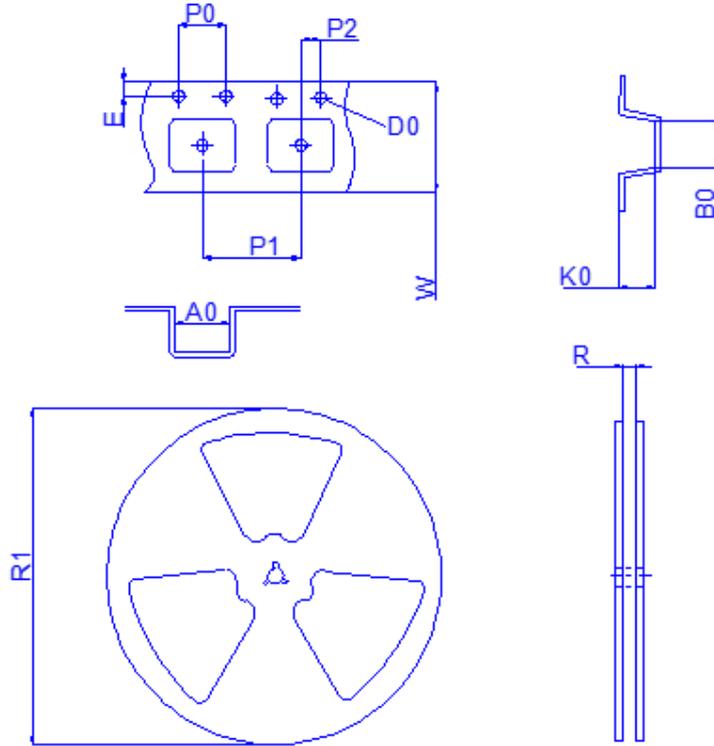


Dimension	A	A1	A2	b	b1	c	c1	D	D1	E	E1	e	H	L	L1	L2	Θ
Min	1.000	-	0.980	0.350	4.020	0.190	0.240	4.450	-	4.950	3.500	-	5.950	0.400	0.270	0.800	0°
Typ.	-	0.075	1.050	0.420	4.230	0.220	0.270		-	-	-	1.270	-	-	-		-
Max	1.300	0.150	1.120	0.500	4.410	0.250	0.300	4.700	4.450	5.300	3.700	-	6.250	0.850	0.570	1.300	8°

Footprint



◆ Tape&Reel Information:2500pcs/Reel



Package	LPAK5X6
Reel	13"
Device orientation	<p>FEEED DIRECTION</p>

Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	6.58	5.50	1.50	1.75	1.45	4	8	2	12	12.4	330
±	0.3	0.3	0.1	0.1	0.1	0.1	0.1	0.1	0.3	2	2