# High Voltage USB PD Power Switch

## General Description

The EM5232A is an advanced high voltage USB PD power switch. The Integrated back-to-back NFETs can support up to 5.5A unidirectional current making the device well suited for system with multiple power charging sour ces. It includes under voltage lockout, input over voltage protection, reverse voltage protection, over current protection during start up and over temperature protection. This part is available in DFN3312 package.

## Ordering Information

| Part Number | OCP Type | $R_{DS(ON)}$ | Package |
|---|---|---|---|
| EM5232AVQC-**0L** | Latch Off | 30mΩ | DFN3.0x3.0-12 |
| EM5232AVQC-**0A** | Auto Restart | 30mΩ | DFN3.0x3.0-12 |

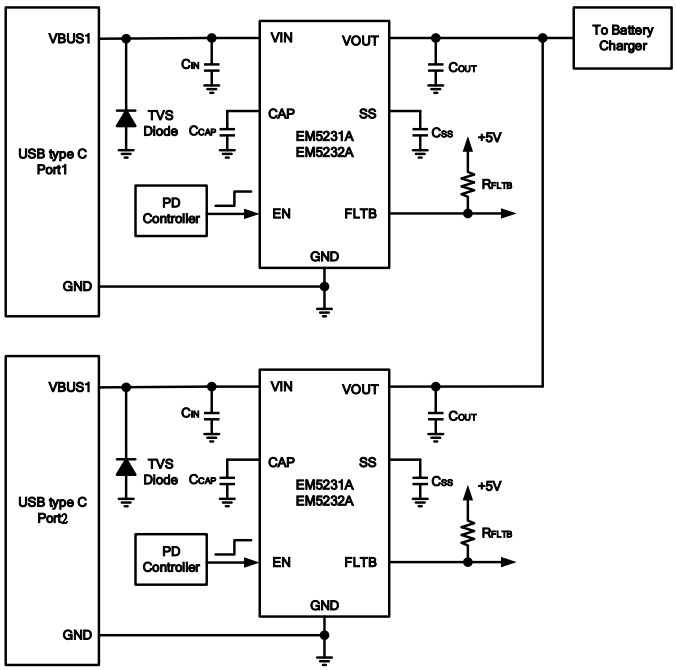
## Features

- Wide input range 3.4V to 22V
- Low 30mΩ (Typ.) MOSFET on resistance
- Maximum 5.5A continue current
- Input over voltage protection
- Input under voltage protection
- 28V Rating on VIN and VOUT pin
- Ideal Diode True Reverse Current Blocking
- Active open drain power ready indicator
- Internal Slew Rate Control for Inrush Current Limit
- True reverse current blocking
- Protection Circuitry:
  UVLO/OVLO/RVP/OTP/OCP
- Robust ESD capability:
  2kV HBM all pins
- RoHS & Halogen Free & TSCA Compliant

## Applications

- Input Power Path Management
- USB PD
- High Side Power Protection Switches

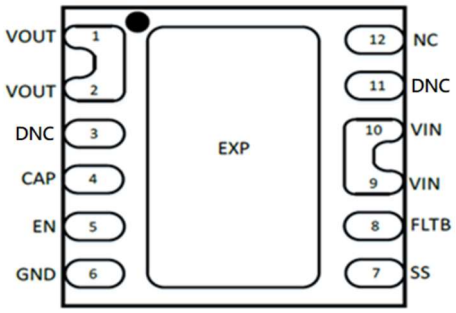
## Typical Application Circuit



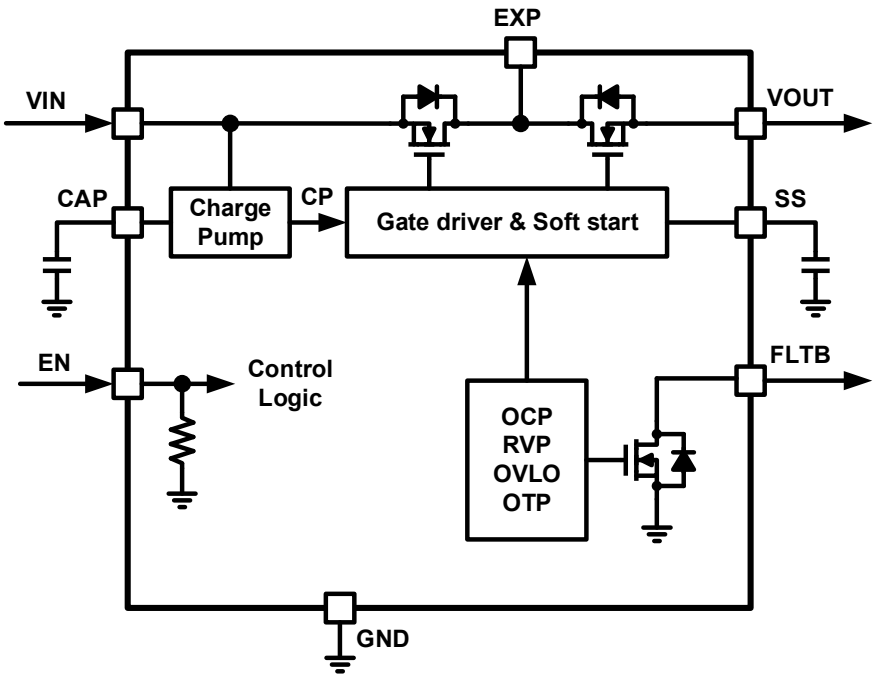

USB PD Application with multiple charging input

## Pin Configuration

**TOP VIEW**



## Function Block




## Pin Assignment

| Pin Name | DFN3312 Pin No. | Pin Function |
|---|---|---|
| VIN | 9/10 | **Input Voltage.** Input Power Supply |
| CAP | 4 | **CAP.** Connect a 1nF capacitor to GND for internal charge pump circuit |
| EN | 5 | **Enable/Disable.** Enable Active High. |
| VOUT | 1/2 | **Output.** Output voltage |
| FLTB | 8 | **Fault Indicator.** Open drain output, tie to GND or floating if not used. |
| GND | 6 | **GND.** Ground |
| SS | 7 | **Soft Start.** Connect a capacitor $C_{SS}$ from SS to GND to set the soft-start time |
| EXP | EXP | **Exposed Thermal Pad.** It is the common drain node for the power switch and it must be electrically isolated. Don't be connected to ground. |
| DNC | 3 | **Do Not Connect.** Internally connected to EXP. |
| DNC | 11 | **Do Not Connect.** Internally connected to VIN. |
| NC | 12 | **No Connect.** |

## Absolute Maximum Rating (Note1)

- VIN, VOUT ---------- -0.5V to +28V
- EN, SS, FLTB ---------- -0.3V to +6V
- CAP to VIN ---------- -0.3V to +6V
- Package Thermal Resistance, $\theta_{JC}$, DFN3.0X3.0-12 (Note 2) ---------- 2.8°C/W
- Package Thermal Resistance, $\theta_{JA}$, DFN3.0X3.0-12 (Note 2) ---------- 36°C/W
- Junction Temperature, $T_J$ ---------- +150°C
- Storage Temperature ---------- -65°C to +150°C
- ESD susceptibility (Note3)
  HBM (Human Body Mode) ---------- 2kV

## Recommended Operating Conditions (Note4)

- VIN, VOUT ---------- 3.4V to +22V
- EN, SS, FLTB ---------- 0V to +5.5V
- CAP to VIN ---------- 0V to +5.5V
- Continuous Switch Current---------- 0A to 5.5A
- Peak Switch Current ($I_{SW}$) for 10 ms @ 2% Duty Cycle ---------- 15A
- Junction Temperature, $T_J$ ---------- -40°C to 125°C
- Ambient Temperature, $T_A$ ---------- -40°C to 85°C

## Electrical Characteristics

$V_{IN}$ = 20V, $V_{EN}$ = 5V, $C_{IN}$ = 10µF, $C_{OUT}$ = 10µF, $C_{SS}$ = 5.6nF, $C_{CAP}$ = 1nF, $T_A$ = 25°C, unless otherwise specified.

| Parameter | Symbol | Test Conditions | Min | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| **Input Section** | | | | | | |
| Input Supply Voltage | $V_{IN}$ | | 3.4 | | 22 | V |
| $V_{IN}$ POR Threshold | $V_{PORTH}$ | Internal $V_{IN}$ POR | 2.8 | 3 | 3.3 | V |
| POR Hysteresis | $V_{PORHYS}$ | | | 200 | | mV |
| $V_{IN}$ Quiescent Current | $I_Q$ | $V_{IN}$=20V, EN=5V, $I_{OUT}$=0A | | 300 | 750 | µA |
| $V_{IN}$ Shutdown Current | $I_{SD}$ | $V_{IN}$=20V, EN=0V, $I_{OUT}$=0A | | 30 | 100 | µA |
| Output Leakage Current | $I_{VO\_OFF}$ | $V_{OUT}$=20V, $V_{IN}$=0V, EN=0V | | 20 | 50 | µA |
| **EN Section** | | | | | | |
| Enable High Level | $V_{ENH}$ | | 1.2 | | | V |
| Disable Low Level | $V_{ENL}$ | | | | 0.4 | V |
| EN pull down resistance | $R_{EN\_LO}$ | | | 1 | | MΩ |
| **VIN OVLO Section** | | | | | | |
| Over voltage Lockout | $V_{OVLO}$ | $V_{IN}$ Rising. System latch off. | 22.8 | 24 | 25.2 | V |
| Over Voltage Protection Debounce Time | $T_{OVD}$ | | | 512 | | µs |
| **Switch Section** | | | | | | |
| On Resistance | $R_{ON}$ | $I_{LOAD}$=1A, $V_{IN}$=4.5V to 22V, EM5232A | | 30 | | mΩ |
| **Power ON/OFF Section** | | | | | | |
| Output Turn-on De-bounce Time | $T_{EN}$ | EN active to $V_{OU}$=10% of $V_{IN}$, $R_L$=100Ω, $C_{SS}$=5.6nF | | 8 | | ms |
| Output Turn off Time | $T_{DIS}$ | Disable from EN to $V_{OUT}$=90% of $V_{IN}$, $C_O$=NC, $R_L$=100Ω, $C_{SS}$=5.6nF | | 32 | | µs |
| Output Rising Time | $T_{SS}$ | $V_{OUT}$ from 10% to 90% of $V_{IN}$, $C_O$=68µF, $R_L$=100Ω, $V_{IN}$=20V, $C_{SS}$=5.6nF | | 1.9 | | ms |
| **Reverse Voltage Protection** | | | | | | |
| Ideal Diode TRCB Regulation Voltage | $V_{IDRCB}$ | $V_{IN}$-$V_{OUT}$ for EM5232A | | 50 | | mV |
| Output Reverse Protection | $V_{RVP}$ | Reverse Protection trip point ($V_{OUT}$>$V_{IN}$+$V_{RVP}$) for EM5232A | | 50 | | mV |
| RVP Delay Time (Guaranteed by design) | $T_{RVD}$ | From $V_{OUT}$>$V_{IN}$+$V_{RVP}$ to switch turn off | 0.5 | 1 | 1.5 | µs |
| **Fault Indicator** | | | | | | |
| Fault Flag Level | $I_{FS}$ | Sink 4mA | | | 0.4 | V |
| **Over Temperature Protection** | | | | | | |
| Over Temperature Protection | $T_{SD}$ | Temperature rising. System latch off. | | 150 | | °C |

**Note 1.** The "Absolute Maximum Ratings" listed above may cause permanent damage to the device. These are for stress ratings only. The functional operation of the device under these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Prolonged exposure to conditions exceeding the absolute maximum ratings may affect the device's reliability.

**Note 2.** $\theta_{JA}$ is measured in the natural convection at $T_A$=25°C on a low effective thermal conductivity test board (Single layout, 1S) of JEDEC 51-3 thermal measurement standard.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

## Timing Diagrams

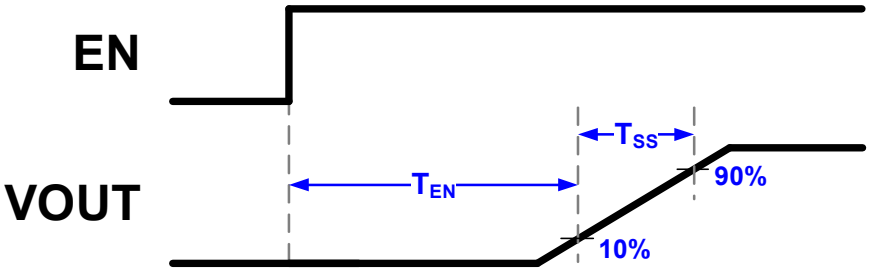



Figure. 1 Turn-on delay and output rising time

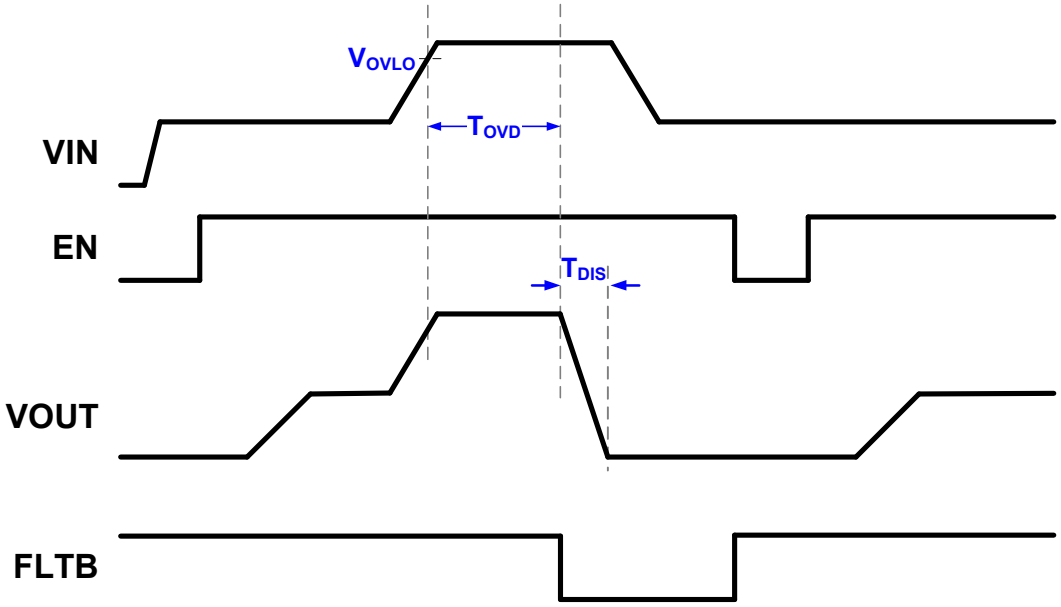



Figure. 2 Over Voltage Lockout

## Timing Diagrams

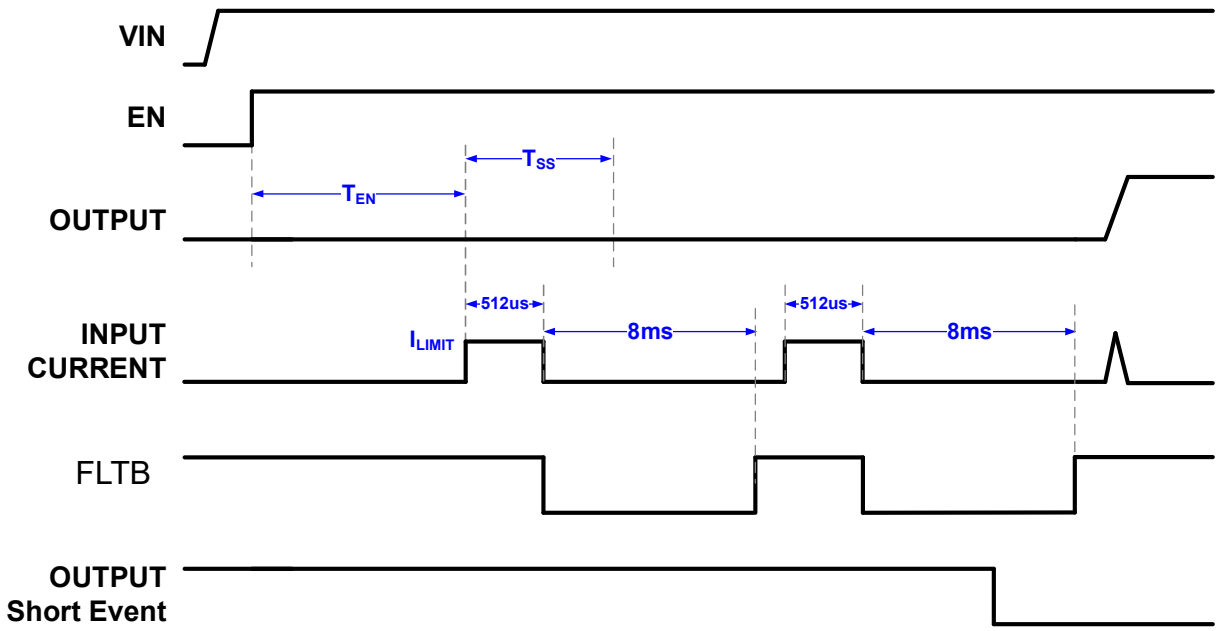



Figure. 3 OUTPUT shorted to GND with OCP

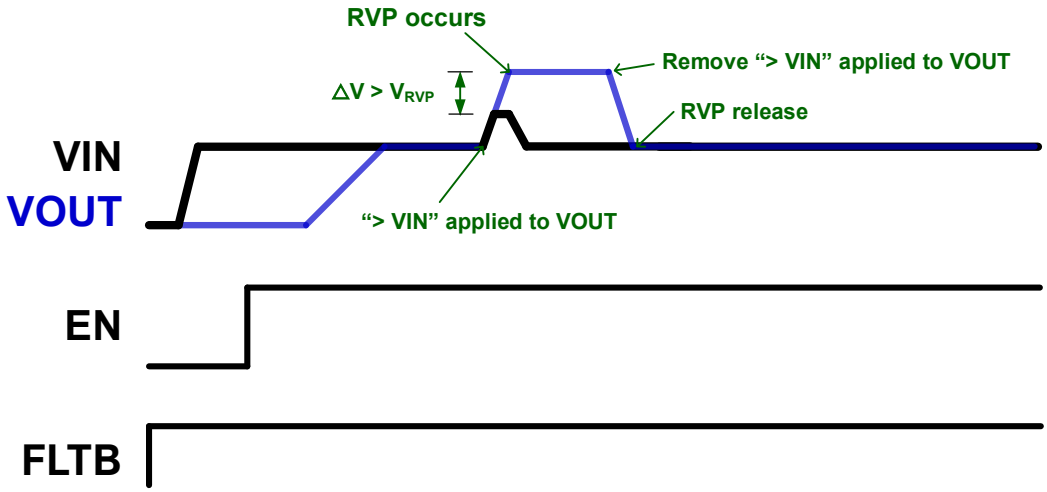
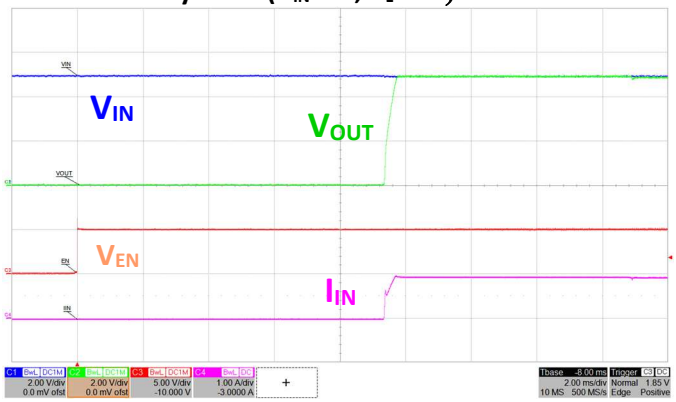



Figure. 4 Output Reverse Voltage Protection

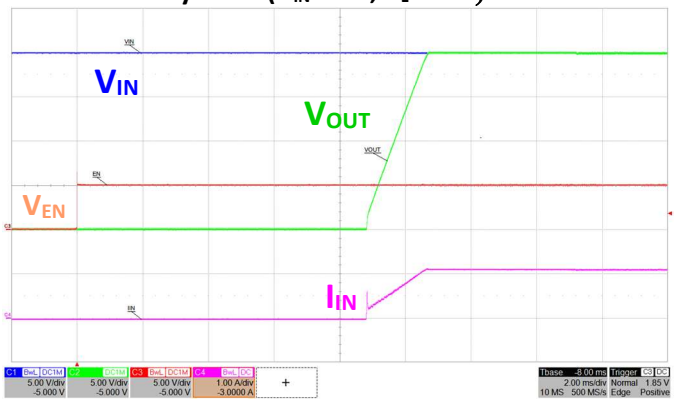
## Typical Operating Characteristics

$V_{IN}$ = 20V, $V_{EN}$ = 5V, $C_{IN}$ = 10µF, $C_{OUT}$ = 10µF, $C_{SS}$ = 5.6nF, $C_{CAP}$ = 1nF, $T_A$ = 25°C, unless otherwise specified.

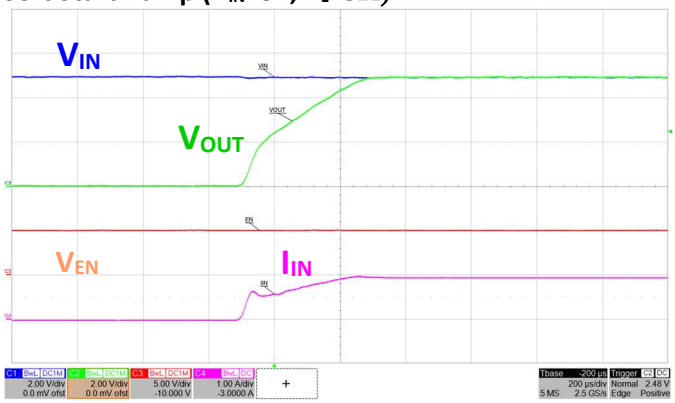
**Soft Start Delay Time ($V_{IN}$=5V, $R_L$=5Ω)**



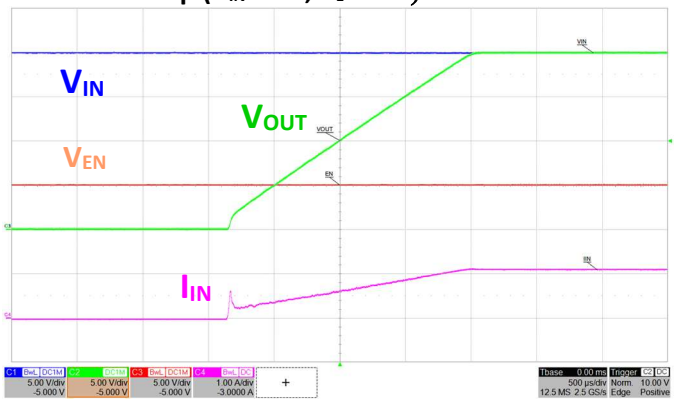

**Soft Start Delay Time ($V_{IN}$=20V, $R_L$=18Ω)**



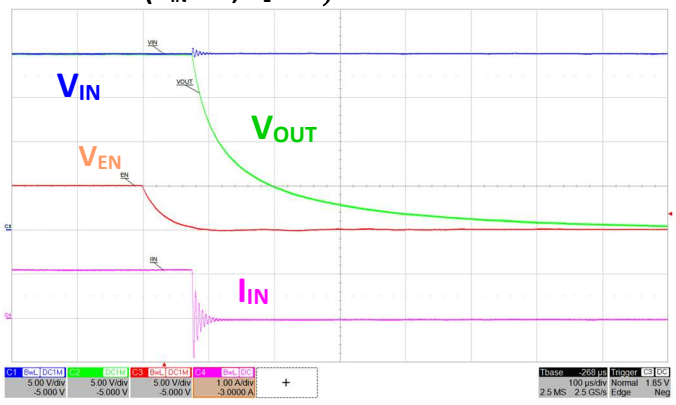

**Soft Start Ramp ($V_{IN}$=5V, $R_L$=5Ω)**



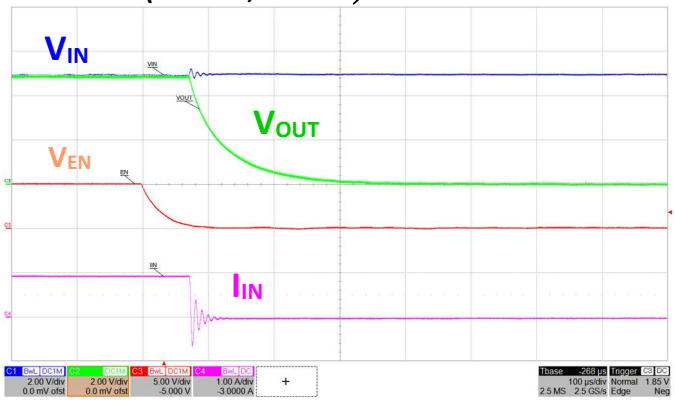

**Soft Start Ramp ($V_{IN}$=20V, $R_L$=18Ω)**



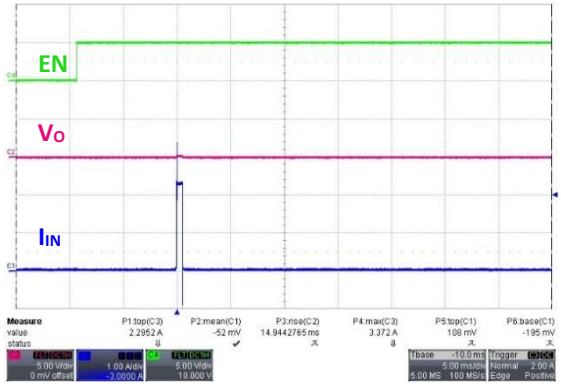

**Shut Down ($V_{IN}$=5V, $R_L$=5Ω)**



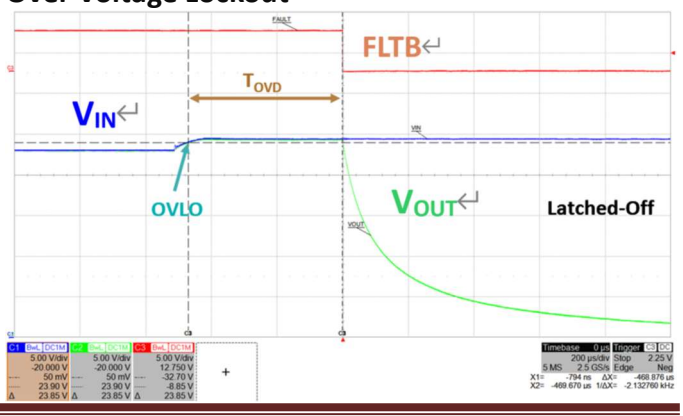

**Shut Down ($V_{IN}$=20V, $R_L$=18Ω)**




**Over Current Protection** (Latch-off Version)

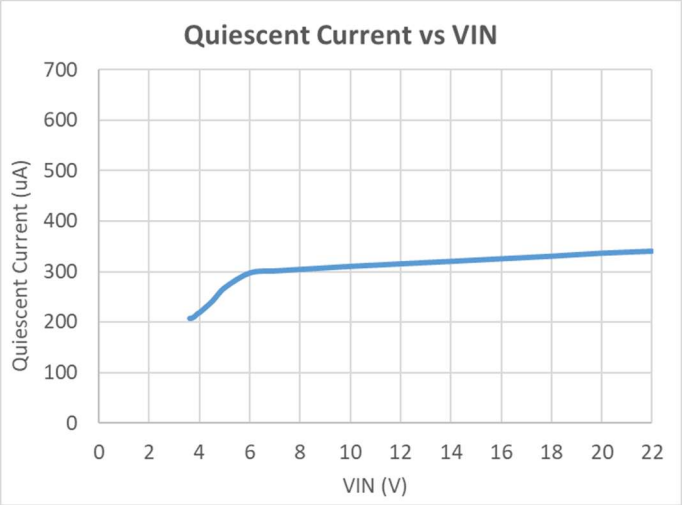


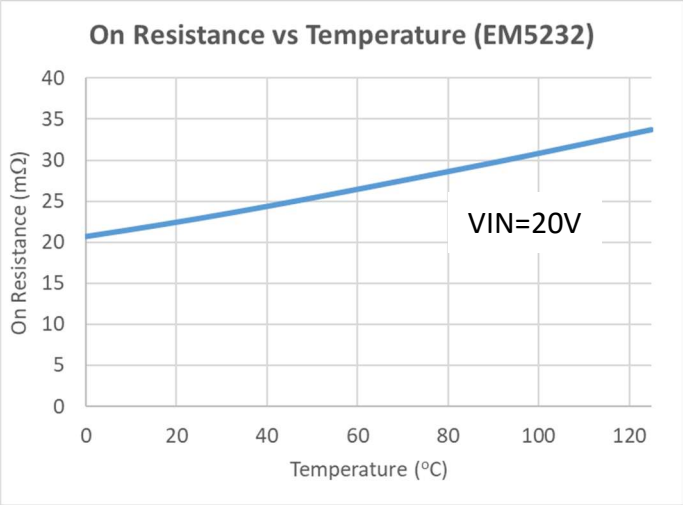

**Over Voltage Lockout**

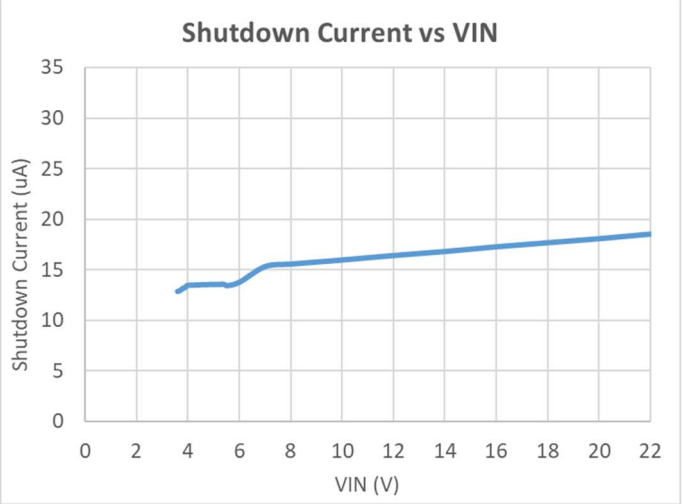


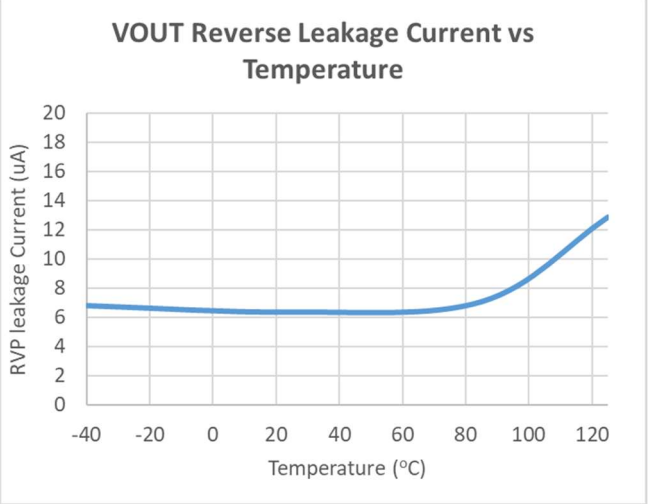
## Typical Operating Characteristics

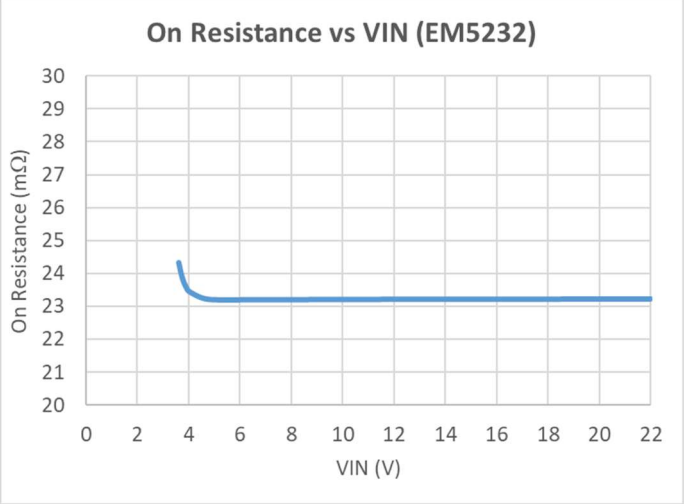
$T_A$ = 25°C, unless otherwise specified.

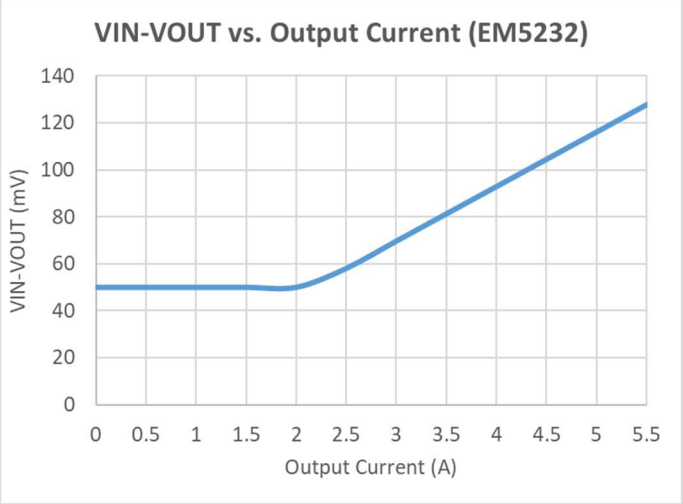


## Functional Description

### Input Under-Voltage Lockout (UVLO)

The under-voltage lockout circuit shut-down the power switch until the input voltage reaches the UVLO turn on threshold.

### Enable

EM5232A is enabled if the voltage of the EN pin is greater than logic high level. If the voltage of the EN pin is less than logic low level, the device will be disabled.

### Over Voltage Lockout (OVLO)

The Over Voltage Lockout shut-down the power switch if the input voltage exceeds 24V(typ.). When the Over Voltage Lockout is triggered, the FLTB is pulled low to report the fault warning, the device will be latched-up until re-toggle EN Pin or cycling the input power supply.

### Over Current Protection (OCP)

The OCP function limits the input current at 1.5A (Min.) during the soft-start period. If the current limit duration exceeds 512µs, the internal power MOSFET shuts off until an automatic restart after 8ms.

### Ideal Diode Mode

When the device is active with no load or light load conditions, it is operating ideal diode mode. it regulates VOUT to be $V_{IDRCB}$(50mV) below VIN in ideal diode mode. As the load current is increasing or decreasing, the device adjusts the gate voltage to keep the $V_{IDRCB}$(50mV) drop from VIN to VOUT. As the load current increases, the device increases the gate voltage until the power MOSFET is fully turned on. It means the device has left the ideal diode mode. VIN to VOUT drop is determined by the product of current through the MOSFET and $R_{DS(ON)}$.

### Reverse Voltage Protection

When the output voltage exceeds the input voltage by 50mV, the reverse voltage circuitry will turn off the internal Power MOS after 1µs in order to protect the input power supply. This protection circuit remains active until the output voltage drops below the input voltage, at which point the device will return to its ideal diode mode.

### Fault Protection

The EM5232A has multiple protections. When OVLO, OTP is triggered, the device will be shut down and the FLTB pin will be pulled low. Re-toggle EN pin to release latch state. When the OCP is triggered, the internal power MOSFET turns off and the FLTB will be pulled low until retry after about 8ms. When RVP is triggered, FLTB does not act.

| Protection | Fault Response | FLTB Status |
|---|---|---|
| OVLO | Latch off | Low |
| OTP | Latch off | Low |
| RVP | Protection remains active until VOUT drops below VIN | High |
| OCP | **EM5232A-0A**: Limit the input current at 1.5A(Min). If exceeds 512µs, the device will be shut off and auto-restart after 8ms<br>**EM5232A-0L**: Limit the input current at 1.5A(Min). If exceeds 512µs, the device will latch-off. | Pulled low if exceeds 512µs |

### Soft-Start Slew-Rate Control

The EM5232A has a soft-start function that ramps up the output voltage with programmable slew rate by adjusting $C_{SS}$ value to avoid input inrush current and output overshooting at start-up. The following formula provides the estimate rise time from 10% to 90% for typical $C_{SS}$ values between 1nF to 10nF.

$$t_{ON} = \frac{V_{IN}}{24} \times \left( \frac{C_{SS}}{0.0023} - 100 \right)$$

Where $C_{SS}$ is in nF and $t_{ON}$ is in µs.

### Input Capacitor

In order to limit the voltage drop on the input supply caused by transient inrush current, an input bypass capacitor is recommended. A 10µF ceramic capacitor should be placed as closed as possible to the VIN pin. The USB specification limits the capacitance on VBUS to a maximum of 10µF. Use this maximum value for noise immunity due to the system and cable plug/unplug transients.

### Over Temperature Protection

Over temperature protection prevent the IC damage when the junction temperature over the 150 degrees, the internal thermal sense turns the power switch off and the FLTB output is pulled low, thus preventing the power switch from damage.

## Layout Guidelines

EM5232A is a protection switch designed to deliver high current. To remove the heat generated by this current, connect as much copper as possible to the exposed pad. The exposed pad is the common drain of the power switch, which must be electrically isolated. On the top layer, expand the exposed pad pad as much as possible for optimal thermal performance. See example in Figure 5.

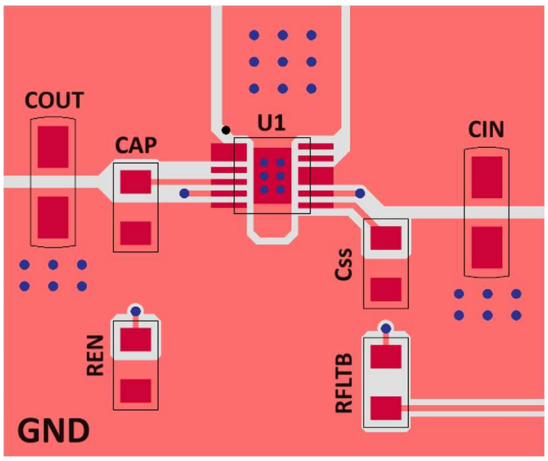



**Figure 5. Top layer layout. Maximum number of VIAs from top layer exposed pad to inner layer.**

There are two ways to create thermal pads on the inner layers as showed in Figure 6. The more layers that have these electrically isolated thermal heat sink pads the better the thermal performance will be. Connect all isolated thermal pad (top, inner layers and bottom) together with as many VIAs as possible for optimal thermal performance.

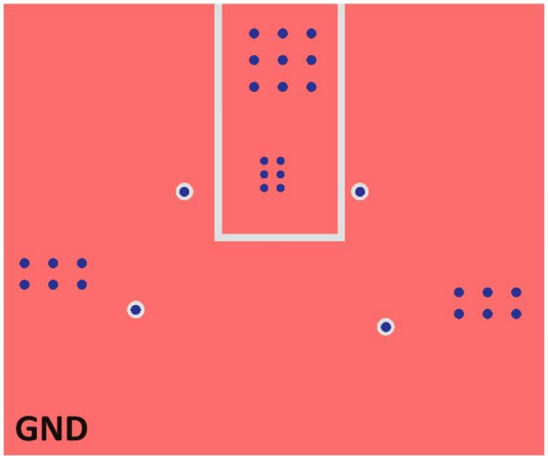



**Figure 6. Inner layer layout. Create electrically isolated thermal pad with flooded plane.**

On the bottom layer, similar to the inner layers, create an isolated thermal pad. Typically, there is more area available on the bottom area for a larger thermal pad. The top and bottom layers have better thermal performance than the inner layers because they are exposed to the ambient. See example in Figure 7.

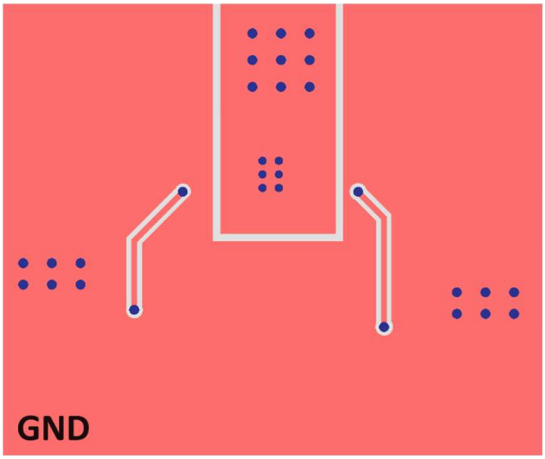
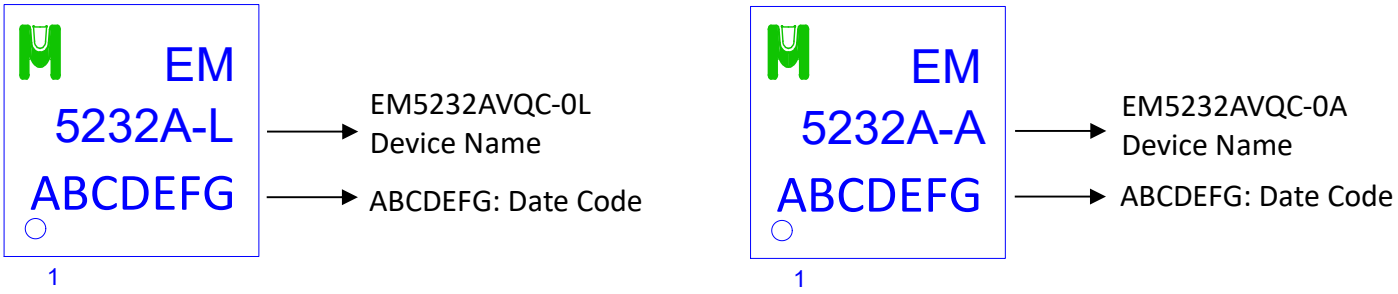



**Figure 7. Bottom layer layout. Create a large electrically isolated thermal pad.**

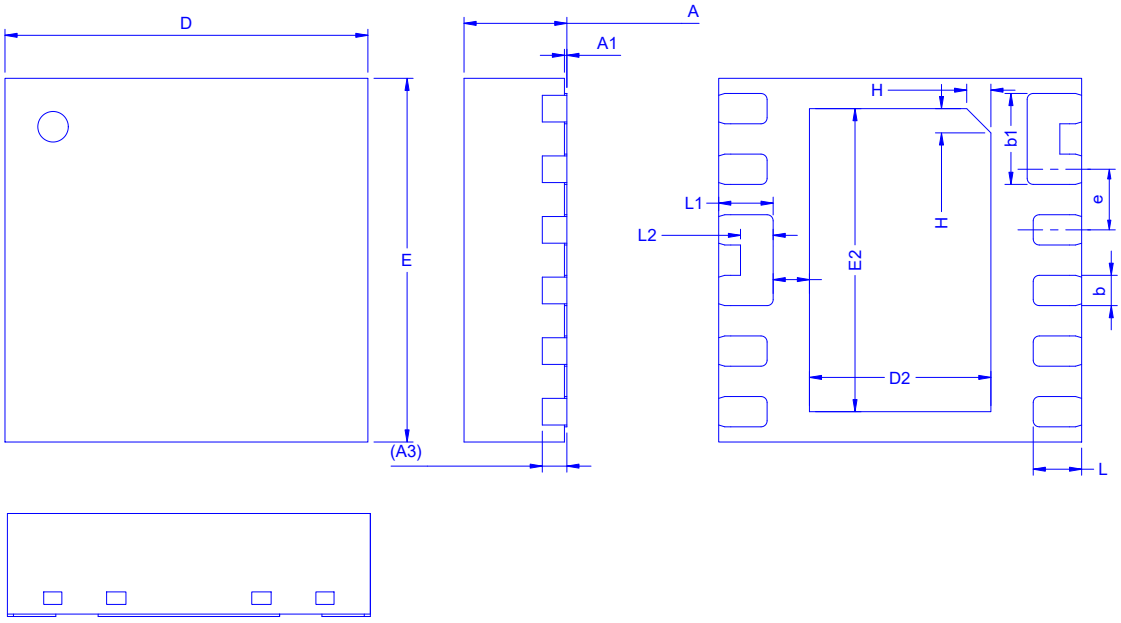
## Ordering & Marking Information

Device Name: EM5232AVQC-0L & EM5232AVQC-0A for DFN3.0X3.0-12




## Outline Drawing

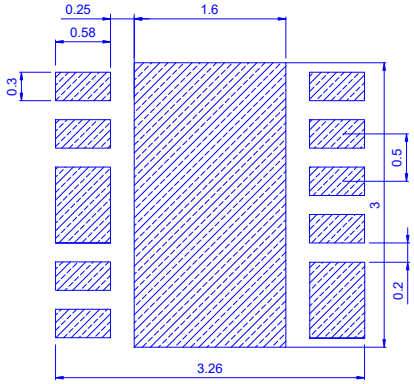
DFN3.0X3.0-12



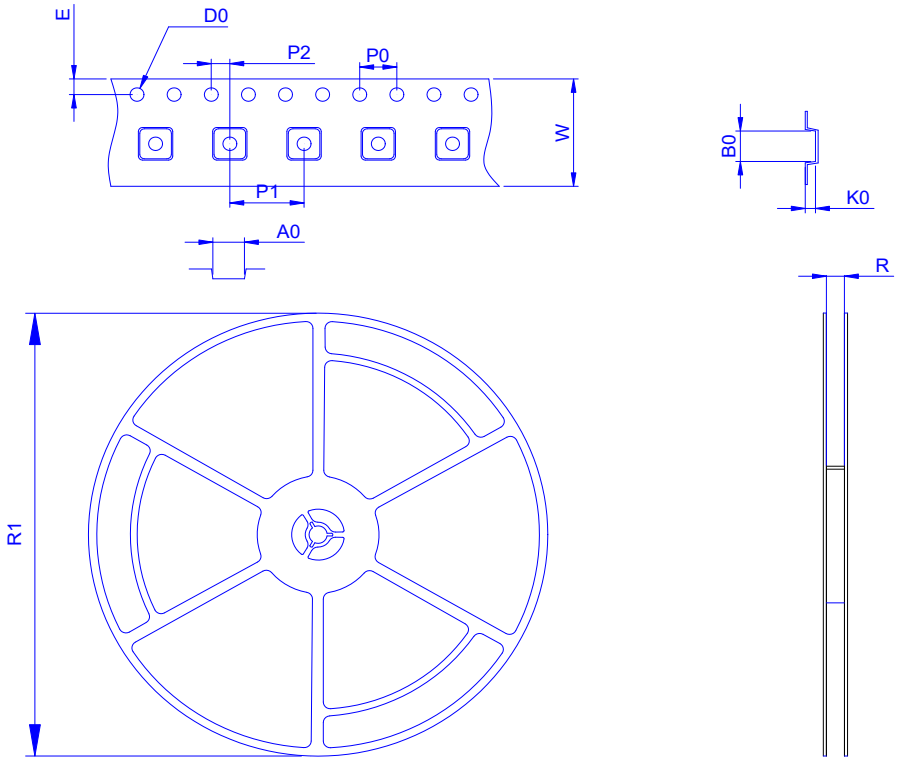

Dimension in mm

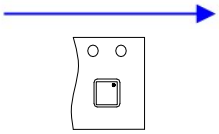
| Dimension | A | A1 | A3 | b | b1 | D | E | D2 | E2 | e | L | L1 | L2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Min. | 0.80 | 0.00 | | 0.20 | 0.70 | 2.90 | 2.90 | 1.40 | 2.40 | 0.40 | 0.35 | 0.40 | 0.22 |
| Typ. | 0.85 | 0.02 | 0.20 | 0.25 | 0.75 | 3.00 | 3.00 | 1.50 | 2.50 | 0.50 | 0.40 | 0.45 | 0.27 |
| Max. | 0.9 | 0.05 | | 0.30 | 0.80 | 3.10 | 3.10 | 1.60 | 2.60 | 0.60 | 0.45 | 0.50 | 0.32 |

## Footprint



◆ Tape&Reel Information: 5000pcs/Reel




| Package | DFN3.0X3.0-12 |
|---|---|
| Reel | 13” |
| Device orientation | FEED DIRECTION  |

Dimension in mm

| Dimension | Carrier tape | | | | | | | | | Reel | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | A0 | B0 | D0 | E | K0 | P0 | P1 | P2 | W | R | R1 |
| Typ. | 3.30 | 3.30 | 1.50 | 1.75 | 1.10 | 4.00 | 8.00 | 2.00 | 12.00 | 12.40 | 330.00 |
| ± | 0.30 | 0.20 | 0.20 | 0.20 | 0.40 | 0.20 | 0.10 | 0.20 | 0.30 | REF | REF |